SE681512

Advance Information

5 V PCM Codec-Filter

The SE681512 is a general purpose per channel PCM Codec–Filter with pin selectable Mu–Law or A–Law companding, and is offered in 20–pin DIP, SOG, and SSOP packages. This device performs the voice digitization and reconstruction as well as the band limiting and smoothing required for PCM systems. This device is designed to operate in both synchronous and asynchronous applications and contains an on–chip precision reference voltage.

This device has an input operational amplifier whose output is the input to the encoder section. The encoder section immediately low–pass filters the analog signal with an active R–C filter to eliminate very high frequency noise from being modulated down to the passband by the switched capacitor filter. From the active R–C filter, the analog signal is converted to a differential signal. From this point, all analog signal processing is done differentially. This allows processing of an analog signal that is twice the amplitude allowed by a single–ended design, which reduces the significance of noise to both the inverted and non–inverted signal paths. Another advantage of this differential design is that noise injected via the power supplies is a common–mode signal that is cancelled when the inverted and non–inverted signals are recombined. This dramatically improves the power supply rejection ratio.

After the differential converter, a differential switched capacitor filter band–passes the analog signal from 200 Hz to 3400 Hz before the signal is digitized by the differential compressing A/D converter.

The decoder accepts PCM data and expands it using a differential D/A converter. The output of the D/A is low–pass filtered at 3400 Hz and sinX/X compensated by a differential switched capacitor filter. The signal is then filtered by an active R–C filter to eliminate the out–of–band energy of the switched capacitor filter.

The SE681512 PCM Codec–Filter utilizes CMOS due to its reliable low–power performance and proven capability for complex analog/digital VLSI functions.

- Pin for Pin Replacement for the SE681512
- Single 5 V Power Supply
- Typical Power Dissipation of 15 mW, Power–Down of 0.01 mW
- Fully–Differential Analog Circuit Design for Lowest Noise
- Transmit Band–Pass and Receive Low–Pass Filters On–Chip
- Active R–C Pre–Filtering and Post–Filtering
- Mu–Law and A–Law Companding by Pin Selection
- On–Chip Precision Reference Voltage (1.575 V)

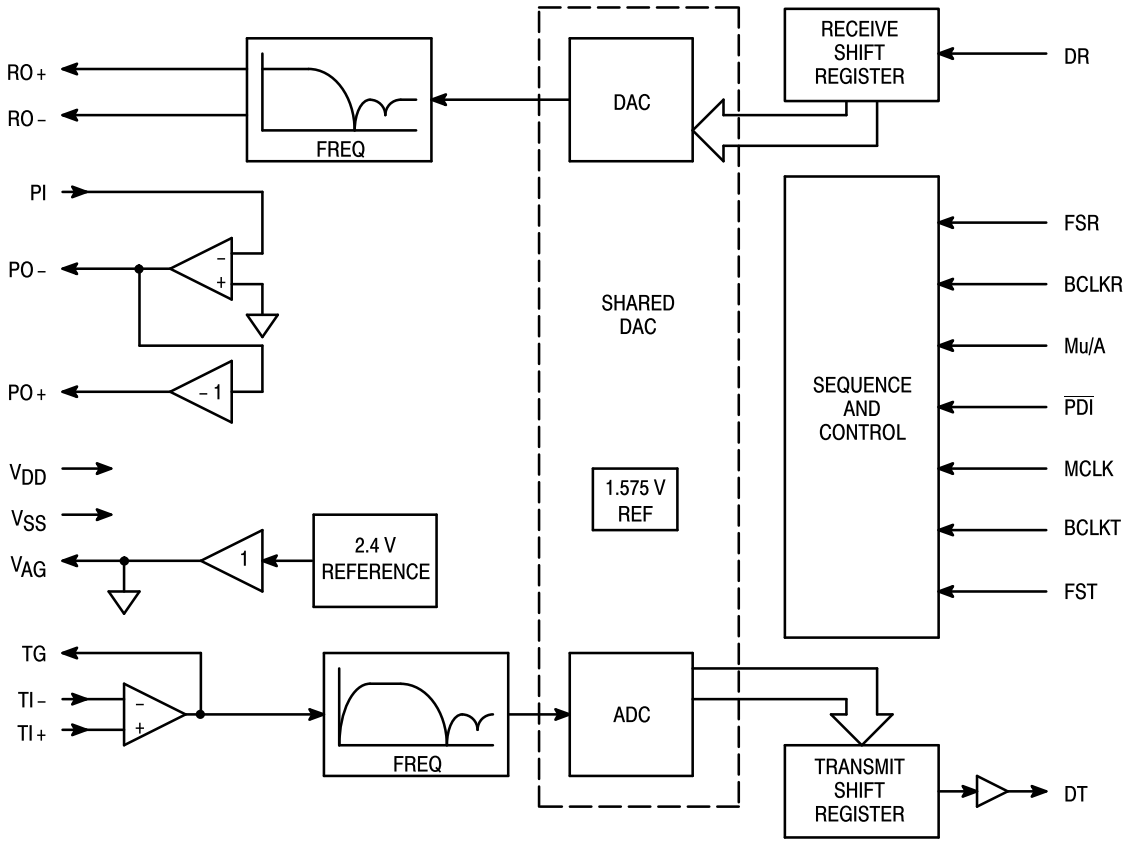


Figure 1. SE681512 PCM Codec–Filter Block Diagram

DEVICE DESCRIPTION

A PCM Codec–Filter is used for digitizing and reconstructing the human voice. These devices are used primarily for the telephone network to facilitate voice switching and transmission. Once the voice is digitized, it may be switched by digital switching methods or transmitted long distance (T1, microwave, satellites, etc.) without degradation. The name codec is an acronym from "COder" for the analog–to–digital converter (ADC) used to digitize voice, and "DECoder" for the digital–to–analog converter (DAC) used for reconstructing voice. A codec is a single device that does both the ADC and DAC conversions.

To digitize intelligible voice requires a signal–to–distortion ratio of about 30 dB over a dynamic range of about 40 dB. This may be accomplished with a linear 13–bit ADC and DAC, but will far exceed the required signal–to–distortion ratio at larger amplitudes than 40 dB below the peak amplitude. This excess performance is at the expense of data per sample. Two methods of data reduction are implemented by compressing the 13–bit linear scheme to companded pseudo–logarithmic 8–bit schemes. The two companding schemes are: Mu–255 Law, primarily in North America and Japan; and A–Law, primarily used in Europe. These companding schemes are accepted world wide. These companding schemes follow a segmented or "piecewise–linear" curve formatted as sign bit, three chord bits, and four step bits. For a given chord, all sixteen of the steps have the same voltage weighting. As the voltage of the analog input increases, the four step bits increment and carry to the three chord bits which increment. When the chord bits increment, the step bits double their voltage weighting. This results in an effective resolution of six bits (sign + chord + four step bits) across a 42 dB dynamic range (seven chords above 0, by 6 dB per chord).

In a sampling environment, Nyquist theory says that to properly sample a continuous signal, it must be sampled at a frequency higher than twice the signal's highest frequency component. Voice contains spectral energy above 3 kHz, but its absence is not detrimental to intelligibility. To reduce the digital data rate, which is proportional to the sampling rate, a sample rate of 8 kHz was adopted, consistent with a bandwidth of 3 kHz. This sampling requires a low–pass filter to limit the high frequency energy above 3 kHz from distorting the in–band signal. The telephone line is also subject to 50/60 Hz power line coupling, which must be attenuated from the signal by a high–pass filter before the analog–to–digital converter.

The digital–to–analog conversion process reconstructs a staircase version of the desired in–band signal, which has spectral images of the in–band signal modulated about the sample frequency and its harmonics. These spectral images are called aliasing components, which need to be attenuated to obtain the desired signal. The low–pass filter used to attenuate these aliasing components is typically called a reconstruction or smoothing filter.

The SE681512 PCM Codec–Filter has the codec, both presampling and reconstruction filters, a precision voltage reference on–chip, and requires no external components.

PIN DESCRIPTIONS

POWER SUPPLY

V_{DD}
Positive Power Supply (Pin 6)

This is the most positive power supply and is typically connected to + 5 V. This pin should be decoupled to V_{SS} with a 0.1 μF ceramic capacitor.

V_{SS}
Negative Power Supply (Pin 15)

This is the most negative power supply and is typically connected to 0 V.

V_{AG}
Analog Ground Output (Pin 20)

This output pin provides a mid–supply analog ground regulated to 2.4 V. This pin should be decoupled to V_{SS} with a 0.01 μF to 0.1 μF ceramic capacitor. All analog signal processing within this device is referenced to this pin. If the audio signals to be processed are referenced to V_{SS}, then special precautions must be utilized to avoid noise between V_{SS} and the V_{AG} pin. Refer to the applications information in this document for more information. The V_{AG} pin becomes high impedance when this device is in the powered down mode.

CONTROL

Mu/A
Mu/A Law Select (Pin 16)

This pin controls the compression for the encoder and the expansion for the decoder. Mu–Law companding is selected when this pin is connected to V_{DD} and A–Law companding is selected when this pin is connected to V_{SS}.

$\overline{PDI}$
Power–Down Input (Pin 10)

This pin puts the device into a low power dissipation mode when a logic 0 is applied. When this device is powered down, all of the clocks are gated off and all bias currents are turned off, which causes RO+, RO–, PO–, PO+, TG, V_{AG}, and DT to become high impedance. The device will operate normally when a logic 1 is applied to this pin. The device goes through a power–up sequence when this pin is taken to a logic 1 state, which prevents the DT PCM output from going low impedance for at least two FST cycles. The filters must settle out before the DT PCM output or the RO+ or RO– receive analog outputs will represent a valid analog signal.

ANALOG INTERFACE

TI+
Transmit Analog Input (Non–Inverting) (Pin 19)

This is the non–inverting input of the transmit input gain setting operational amplifier. This pin accommodates a differential to single–ended circuit for the input gain setting op amp. This allows input signals that are referenced to the V_{SS} pin to be level shifted to the V_{AG} pin with minimum noise. This pin may be connected to the V_{AG} pin for an inverting amplifier configuration if the input signal is already referenced to the V_{AG} pin. The common mode range of the TI+ and TI– pins is from 1.2 V, to V_{DD} minus 2 V. This is an FET gate input. Connecting the TI+ pin to V_{DD} will place this amplifier's output (TG) into a high–impedance state, thus allowing the TG pin to serve as a high–impedance input to the transmit filter.

TI–
Transmit Analog Input (Inverting) (Pin 18)

This is the inverting input of the transmit gain setting operational amplifier. Gain setting resistors are usually connected from this pin to TG and from this pin to the analog signal source. The common mode range of the TI+ and TI– pins is from 1.2 V to V_{DD} – 2 V. This is an FET gate input. Connecting the TI+ pin to V_{DD} will place this amplifier's output (TG) into a high–impedance state, thus allowing the TG pin to serve as a high–impedance input to the transmit filter.

TG
Transmit Gain (Pin 17)

This is the output of the transmit gain setting operational amplifier and the input to the transmit band–pass filter. This op amp is capable of driving a 2 kΩ load. Connecting the TI+ pin to V_{DD} will place this amplifier's output (TG) into a high–impedance state, thus allowing the TG pin to serve as a high–impedance input to the transmit filter. All signals at this pin are referenced to the V_{AG} pin. This pin is high impedance when the device is in the powered down mode.

RO+
Receive Analog Output (Non–Inverting) (Pin 1)

This is the non–inverting output of the receive smoothing filter from the digital–to–analog converter. This output is capable of driving a 2 kΩ load to 1.575 V peak referenced to the V_{AG} pin. This pin is high impedance when the device is in the powered down mode.

RO–
Receive Analog Output (Inverting) (Pin 2)

This is the inverting output of the receive smoothing filter from the digital–to–analog converter. This output is capable of driving a 2 kΩ load to 1.575 V peak referenced to the V_{AG} pin. This pin is high impedance when the device is in the powered down mode.

PI
Power Amplifier Input (Pin 3)

This is the inverting input to the PO– amplifier. The non–inverting input to the PO– amplifier is internally tied to the V_{AG} pin. The PI and PO– pins are used with external resistors in an inverting op amp gain circuit to set the gain of the PO+ and PO– push–pull power amplifier outputs. Connecting PI to V_{DD} will power down the power driver amplifiers and the PO+ and PO– outputs will be high impedance.

PO–
Power Amplifier Output (Inverting) (Pin 4)

This is the inverting power amplifier output, which is used to provide a feedback signal to the PI pin to set the gain of the push–pull power amplifier outputs. This pin is capable of driving a 300 Ω load to PO+. The PO+ and PO– outputs are differential (push–pull) and capable of driving a 300 Ω load to 3.15 V peak, which is 6.3 V peak–to–peak. The bias voltage and signal reference of this output is the V_{AG} pin. The V_{AG} pin cannot source or sink as much current as this pin, and

therefore low impedance loads must be between PO+ and PO–. Connecting PI to V_{DD} will power down the power driver amplifiers and the PO+ and PO– outputs will be high impedance. This pin is also high impedance when the device is powered down by the $\overline{PDI}$ pin.

PO+
Power Amplifier Output (Non–Inverting) (Pin 5)

This is the non–inverting power amplifier output, which is an inverted version of the signal at PO–. This pin is capable of driving a 300 Ω load to PO–. Connecting PI to V_{DD} will power down the power driver amplifiers and the PO+ and PO– outputs will be high impedance. This pin is also high impedance when the device is powered down by the $\overline{PDI}$ pin. See PI and PO– for more information.

DIGITAL INTERFACE

MCLK
Master Clock (Pin 11)

This is the master clock input pin. The clock signal applied to this pin is used to generate the internal 256 kHz clock and sequencing signals for the switched–capacitor filters, ADC, and DAC. The internal prescaler logic compares the clock on this pin to the clock at FST (8 kHz) and will automatically accept 256, 512, 1536, 1544, 2048, 2560, or 4096 kHz. For MCLK frequencies of 256 and 512 kHz, MCLK must be synchronous and approximately rising edge aligned to FST. For optimum performance at frequencies of 1.536 MHz and higher, MCLK should be synchronous and approximately rising edge aligned to the rising edge of FST. In many applications, MCLK may be tied to the BCLKT pin.

FST
Frame Sync, Transmit (Pin 14)

This pin accepts an 8 kHz clock that synchronizes the output of the serial PCM data at the DT pin. This input is compatible with various standards including IDL, Long Frame Sync, Short Frame Sync, and GCI formats. If both FST and FSR are held low for several 8 kHz frames, the device will power down.

BCLKT
Bit Clock, Transmit (Pin 12)

This pin controls the transfer rate of transmit PCM data. In the IDL and GCI modes it also controls the transfer rate of the receive PCM data. This pin can accept any bit clock frequency from 64 to 4096 kHz for Long Frame Sync and Short Frame Sync timing. This pin can accept clock frequencies from 256 kHz to 4.096 MHz in IDL mode, and from 512 kHz to 6.176 MHz for GCI timing mode.

DT
Data, Transmit (Pin 13)

This pin is controlled by FST and BCLKT and is high impedance except when outputting PCM data. When operating in the IDL or GCI mode, data is output in either the B1 or B2 channel as selected by FSR. This pin is high impedance when the device is in the powered down mode.

FSR
Frame Sync, Receive (Pin 7)

When used in the Long Frame Sync or Short Frame Sync mode, this pin accepts an 8 kHz clock, which synchronizes the input of the serial PCM data at the DR pin. FSR can be asynchronous to FST in the Long Frame Sync or Short Frame Sync modes. When an ISDN mode (IDL or GCI) has been selected with BCLKR, this pin selects either B1 (logic 0) or B2 (logic 1) as the active data channel.

BCLKR
Bit Clock, Receive (Pin 9)

When used in the Long Frame Sync or Short Frame Sync mode, this pin accepts any bit clock frequency from 64 to 4096 kHz. When this pin is held at a logic 1, FST, BCLKT, DT, and DR become IDL Interface compatible. When this pin is held at a logic 0, FST, BCLKT, DT, and DR become GCI Interface compatible.

DR
Data, Receive (Pin 8)

This pin is the PCM data input, and when in a Long Frame Sync or Short Frame Sync mode is controlled by FSR and BCLKR. When in the IDL or GCI mode, this data transfer is controlled by FST and BCLKT. FSR and BCLKR select the B channel and ISDN mode, respectively.

FUNCTIONAL DESCRIPTION

ANALOG INTERFACE AND SIGNAL PATH

The transmit portion of this device includes a low–noise, three–terminal op amp capable of driving a 2 kΩ load. This op amp has inputs of TI+ (Pin 19) and TI– (Pin 18) and its output is TG (Pin 17). This op amp is intended to be configured in an inverting gain circuit. The analog signal may be applied directly to the TG pin if this transmit op amp is independently powered down by connecting the TI+ and TI– inputs to the V_{DD} power supply. The TG pin becomes high impedance when the transmit op amp is powered down. The TG pin is internally connected to a 3–pole anti–aliasing pre–filter. This pre–filter incorporates a 2–pole Butterworth active low–pass filter, followed by a single passive pole. This pre–filter is followed by a single–ended to differential converter that is clocked at 512 kHz. All subsequent analog processing utilizes fully–differential circuitry. The next section is a fully–differential, 5–pole switched–capacitor low–pass filter with a 3.4 kHz frequency cutoff. After this filter is a 3–pole switched–capacitor high–pass filter having a cutoff frequency of about 200 Hz. This high–pass stage has a transmission zero at dc that eliminates any dc coming from the analog input or from accumulated op amp offsets in the preceding filter stages. The last stage of the high–pass filter is an autozeroed sample and hold amplifier.

One bandgap voltage reference generator and digital–to–analog converter (DAC) are shared by the transmit and receive sections. The autozeroed, switched–capacitor bandgap reference generates precise positive and negative reference voltages that are virtually independent of temperature and power supply voltage. A binary–weighted capacitor array (CDAC) forms the chords of the companding structure, while a resistor string (RDAC) implements the linear steps within each chord. The encode process uses the DAC, the voltage reference, and a frame–by–frame autozeroed comparator to implement a successive–approximation con-

version algorithm. All of the analog circuitry involved in the data conversion (the voltage reference, RDAC, CDAC, and comparator) are implemented with a differential architecture.

The receive section includes the DAC described above, a sample and hold amplifier, a 5–pole, 3400 Hz switched capacitor low–pass filter with sinX/X correction, and a 2–pole active smoothing filter to reduce the spectral components of the switched capacitor filter. The output of the smoothing filter is buffered by an amplifier, which is output at the RO+ and RO– pins. These outputs are capable of driving a 4 kΩ load differentially or a 2 kΩ load to the V_{AG} pin. The SE681512 also has a pair of power amplifiers that are connected in a push–pull configuration. The PI pin is the inverting input to the PO– power amplifier. The non–inverting input is internally tied to the V_{AG} pin. This allows this amplifier to be used in an inverting gain circuit with two external resistors. The PO+ amplifier has a gain of minus one, and is internally connected to the PO– output. This complete power amplifier circuit is a differential (push–pull) amplifier with adjustable gain that is capable of driving a 300 Ω load to +12 dBm. The power amplifier may be powered down independently of the rest of the chip by connecting the PI pin to V_{DD}.

POWER–DOWN

There are two methods of putting this device into a low power consumption mode, which makes the device nonfunctional and consumes virtually no power. $\overline{PDI}$ is the power–down input pin which, when taken low, powers down the device. Another way to power the device down is to hold both the FST and FSR pins low. When the chip is powered down, the V_{AG}, TG, RO+, RO–, PO+, PO–, and DT outputs are high impedance. To return the chip to the power–up state, $\overline{PDI}$ must be high and the FST frame sync pulse must be present. The DT output will remain in a high–impedance state for at least two FST pulses after power–up.

MASTER CLOCK

Since this codec–filter design has a single DAC architecture, the MCLK pin is used as the master clock for all analog signal processing including analog–to–digital conversion, digital–to–analog conversion, and for transmit and receive filtering functions of this device. The clock frequency applied to the MCLK pin may be 256 kHz, 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, 2.56 MHz, or 4.096 MHz. This device has a prescaler that automatically determines the proper divide ratio to use for the MCLK input, which achieves the required 256 kHz internal sequencing clock. The clocking requirements of the MCLK input are independent of the PCM data transfer mode (i.e., Long Frame Sync, Short Frame Sync, IDL mode, or GCI mode).

DIGITAL I/O

The SE681512 is pin selectable for Mu–Law or A–Law. Table 1 shows the 8–bit data word format for positive and negative zero and full scale for both companding schemes (see Tables 3 and 4 at the end of this document for a complete PCM word conversion table). Table 2 shows the series of eight PCM words for both Mu–Law and A–Law that correspond to a digital milliwatt. The digital mW is the 1 kHz calibration signal reconstructed by the DAC that defines the absolute gain or 0 dBm0 Transmission Level Point (TLP) of the DAC. The 0 dBm0 level for Mu–Law is 3.17 dB below the maximum level for an unclipped tone signal. The 0 dBm0 level for A–Law is 3.14 dB below the maximum level for an unclipped tone signal. The timing for the PCM data transfer is independent of the companding scheme selected. Refer to Figure 2 for a summary and comparison of the four PCM data interface modes of this device.

Table 1. PCM Codes for Zero and Full Scale

Level	Mu–Law			A–Law		
	Sign Bit	Chord Bits	Step Bits	Sign Bit	Chord Bits	Step Bits
+ Full Scale	1	0 0 0	0 0 0 0	1	0 1 0	1 0 1 0
+ Zero	1	1 1 1	1 1 1 1	1	1 0 1	0 1 0 1
– Zero	0	1 1 1	1 1 1 1	0	1 0 1	0 1 0 1
– Full Scale	0	0 0 0	0 0 0 0	0	0 1 0	1 0 1 0

Table 2. PCM Codes for Digital mW

Phase	Mu–Law			A–Law		
	Sign Bit	Chord Bits	Step Bits	Sign Bit	Chord Bits	Step Bits
π/8	0	0 0 1	1 1 1 0	0	0 1 1	0 1 0 0
3π/8	0	0 0 0	1 0 1 1	0	0 1 0	0 0 0 1
5π/8	0	0 0 0	1 0 1 1	0	0 1 0	0 0 0 1
7π/8	0	0 0 1	1 1 1 0	0	0 1 1	0 1 0 0
9π/8	1	0 0 1	1 1 1 0	1	0 1 1	0 1 0 0
11π/8	1	0 0 0	1 0 1 1	1	0 1 0	0 0 0 1
13π/8	1	0 0 0	1 0 1 1	1	0 1 0	0 0 0 1
15π/8	1	0 0 1	1 1 1 0	1	0 1 1	0 1 0 0

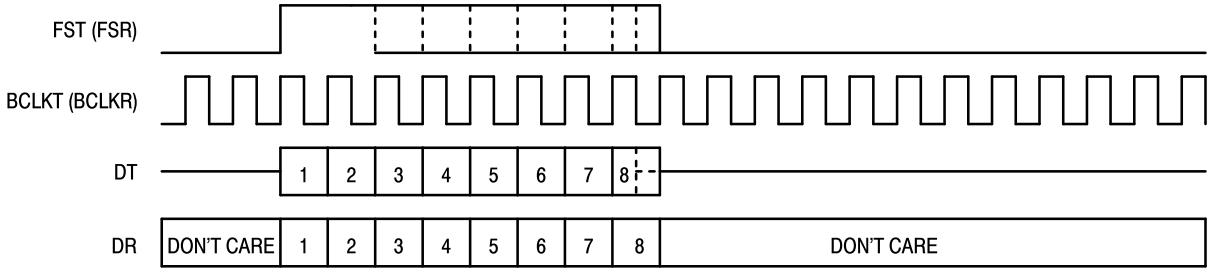


Figure 2a. Long Frame Sync (Transmit and Receive Have Individual Clocking)

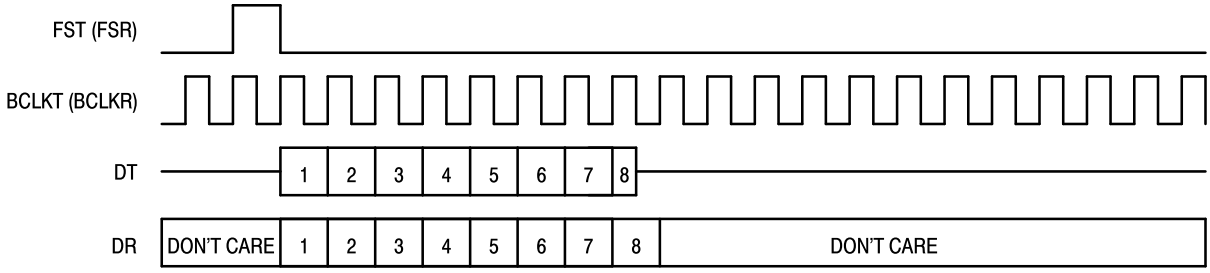


Figure 2b. Short Frame Sync (Transmit and Receive Have Individual Clocking)

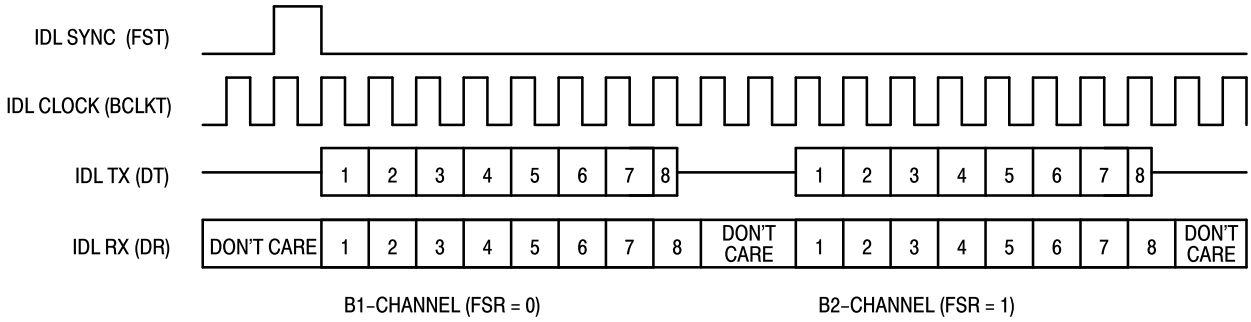


Figure 2c. IDL Interface — BCLKR = 1 (Transmit and Receive Have Common Clocking)

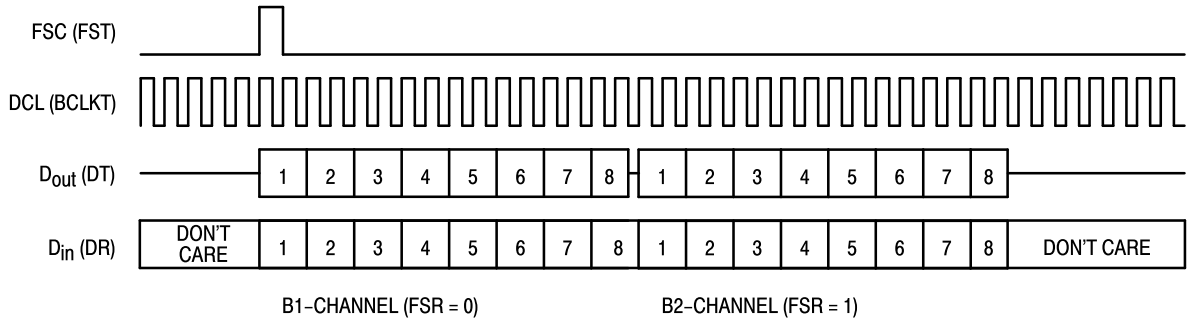


Figure 2d. GCI Interface — BCLKR = 0 (Transmit and Receive Have Common Clocking)

Figure 2. Digital Timing Modes for the PCM Data Interface

Long Frame Sync

Long Frame Sync is the industry name for one type of clocking format that controls the transfer of the PCM data words. (Refer to Figure 2a.) The ‘‘Frame Sync’’ or ‘‘Enable’’ is used for two specific synchronizing functions. The first is to synchronize the PCM data word transfer, and the second is to control the internal analog–to–digital and digital–to–analog conversions. The term ‘‘Sync’’ refers to the function of synchronizing the PCM data word onto or off of the multiplexed serial PCM data bus, which is also known as a PCM highway. The term ‘‘Long’’ comes from the duration of the frame sync measured in PCM data clock cycles. Long Frame Sync timing occurs when the frame sync is used directly as the PCM data output driver enable. This results in the PCM output going low impedance with the rising edge of the transmit frame sync, and remaining low impedance for the duration of the transmit frame sync.

The implementation of Long Frame Sync has maintained compatibility and been optimized for external clocking simplicity. This optimization includes the PCM data output going low impedance with the logical AND of the transmit frame sync (FST) with the transmit data bit clock (BCLKT). The optimization also includes the PCM data output (DT) remaining low impedance until the middle of the LSB (seven and a half PCM data clock cycles) or until the FST pin is taken low, whichever occurs last. This requires the frame sync to be approximately rising edge aligned with the initiation of the PCM data word transfer, but the frame sync does not have a precise timing requirement for the end of the PCM data word transfer. The device recognizes Long Frame Sync clocking when the frame sync is held high for two consecutive falling edges of the transmit data clock. The transmit logic decides on each frame sync whether it should interpret the next frame sync pulse as a Long or a Short Frame Sync. This decision is used for receive circuitry also. The device is designed to prevent PCM bus contention by not allowing the PCM data output to go low impedance for at least two frame sync cycles after power is applied or when coming out of the powered down mode.

The receive side of the device is designed to accept the same frame sync and data clock as the transmit side and to be able to latch its own transmit PCM data word. Thus the PCM digital switch needs to be able to generate only one type of frame sync for use by both transmit and receive sections of the device.

The logical AND of the receive frame sync with the receive data clock tells the device to start latching the 8–bit serial word into the receive data input on the falling edges of the receive data clock. The internal receive logic counts the receive data clock cycles and transfers the PCM data word to the digital–to–analog converter sequencer on the ninth data clock rising edge.

This device is compatible with four digital interface modes. To ensure that this device does not reprogram itself for a different timing mode, the BCLKR pin must change logic state no less than every 125 μs. The minimum PCM data bit clock frequency of 64 kHz satisfies this requirement.

Short Frame Sync

Short Frame Sync is the industry name for the type of clocking format that controls the transfer of the PCM data words (refer to Figure 2b). The ‘‘Frame Sync’’ or ‘‘Enable’’ is used for two specific synchronizing functions. The first is to synchronize the PCM data word transfer, and the second is to control the internal analog–to–digital and digital–to–analog conversions. The term ‘‘Sync’’ refers to the function of synchronizing the PCM data word onto or off of the multiplexed serial PCM data bus, which is also known as a PCM highway. The term ‘‘Short’’ comes from the duration of the frame sync measured in PCM data clock cycles. Short Frame Sync timing occurs when the frame sync is used as a ‘‘pre–synchronization’’ pulse that is used to tell the internal logic to clock out the PCM data word under complete control of the data clock. The Short Frame Sync is held high for one falling data clock edge. The device outputs the PCM data word beginning with the following rising edge of the data clock. This results in the PCM output going low impedance with the rising edge of the transmit data clock, and remaining low impedance until the middle of the LSB (seven and a half PCM data clock cycles).

The device recognizes Short Frame Sync clocking when the frame sync is held high for one and only one falling edge of the transmit data clock. The transmit logic decides on each frame sync whether it should interpret the next frame sync pulse as a Long or a Short Frame Sync. This decision is used for receive circuitry also. The device is designed to prevent PCM bus contention by not allowing the PCM data output to go low impedance for at least two frame sync cycles after power is applied or when coming out of the powered down mode.

The receive side of the device is designed to accept the same frame sync and data clock as the transmit side and to be able to latch its own transmit PCM data word. Thus the PCM digital switch needs to be able to generate only one type of frame sync for use by both transmit and receive sections of the device.

The falling edge of the receive data clock latching a high logic level at the receive frame sync input tells the device to start latching the 8–bit serial word into the receive data input on the following eight falling edges of the receive data clock. The internal receive logic counts the receive data clock cycles and transfers the PCM data word to the digital–to–analog converter sequencer on the rising data clock edge after the LSB has been latched into the device.

This device is compatible with four digital interface modes. To ensure that this device does not reprogram itself for a different timing mode, the BCLKR pin must change logic state no less than every 125 μs. The minimum PCM data bit clock frequency of 64 kHz satisfies this requirement.

Interchip Digital Link (IDL)

The Interchip Digital Link (IDL) Interface is one of two standard synchronous 2B+D ISDN timing interface modes with which this device is compatible. In the IDL mode, the device can communicate in either of the two 64 kbps B channels (refer to Figure 2c for sample timing). The IDL mode is selected when the BCLKR pin is held high for two or more FST (IDL SYNC) rising edges. The digital pins that control the transmit and receive PCM word transfers are reprogrammed to accommodate this mode. The pins affected are FST, FSR, BCLKT, DT, and DR. The IDL Interface consists of four pins: IDL SYNC (FST), IDL CLK (BCLKT), IDL TX (DT), and IDL RX (DR). The IDL interface mode provides access to both the transmit and receive PCM data words with common control clocks of IDL Sync and IDL Clock. In this mode, the

FSR pin controls whether the B1 channel or the B2 channel is used for both transmit and receive PCM data word transfers. When the FSR pin is low, the transmit and receive PCM words are transferred in the B1 channel, and for FSR high the B2 channel is selected. The start of the B2 channel is ten IDL CLK cycles after the start of the B1 channel.

The IDL SYNC (FST, Pin 14) is the input for the IDL frame synchronization signal. The signal at this pin is nominally high for one cycle of the IDL Clock signal and is rising edge aligned with the IDL Clock signal. (Refer to Figure 4 and the IDL Timing specifications for more details.) This event identifies the beginning of the IDL frame. The frequency of the IDL Sync signal is 8 kHz. The rising edge of the IDL SYNC (FST) should be aligned approximately with the rising edge of MCLK. MCLK must be one of the clock frequencies specified in the Digital Switching Characteristics table, and is typically tied to IDL CLK (BCLKT).

The IDL CLK (BCLKT, Pin 12) is the input for the PCM data clock. All IDL PCM transfers and data control sequencing are controlled by this clock following the IDL SYNC. This pin accepts an IDL data clock frequency of 256 kHz to 4.096 MHz.

The IDL TX (DT, Pin 13) is the output for the transmit PCM data word. Data bits are output for the B1 channel on sequential rising edges of the IDL CLK signal beginning after the IDL SYNC pulse. If the B2 channel is selected, then the PCM word transfer starts on the eleventh IDL CLK rising edge after the IDL SYNC pulse. The IDL TX pin will remain low impedance for the duration of the PCM word until the LSB after the falling edge of IDL CLK. The IDL TX pin will remain in a high impedance state when not outputting PCM data or when a valid IDL Sync signal is missing.

The IDL RX (DR, Pin 8) is the input for the receive PCM data word. Data bits are input for the B1 channel on sequential falling edges of the IDL CLK signal beginning after the IDL SYNC pulse. If the B2 channel is selected, then the PCM word is latched in starting on the eleventh IDL CLK falling edge after the IDL SYNC pulse.

General Circuit Interface (GCI)

The General Circuit Interface (GCI) is the second of two standard synchronous 2B+D ISDN timing interface modes with which this device is compatible. In the GCI mode, the device can communicate in either of the two 64 kbps B–channels. (Refer to Figure 2d for sample timing.) The GCI mode is selected when the BCLKR pin is held low for two or more FST (FSC) rising edges. The digital pins that control the transmit and receive PCM word transfers are reprogrammed to accommodate this mode. The pins affected are FST, FSR, BCLKT, DT, and DR. The GCI Interface consists of four pins: FSC (FST), DCL (BCLKT), D_{out} (DT), and D_{in} (DR). The GCI interface mode provides access to both the transmit and receive PCM data words with common control clocks of FSC (frame synchronization clock) and DCL (data clock). In this mode, the FSR pin controls whether the B1 channel or the B2 channel is used for both transmit and receive PCM data word transfers. When the FSR pin is low, the transmit and receive PCM words are transferred in the B1 channel, and for FSR high the B2 channel is selected. The start of the B2 channel is 16 DCL cycles after the start of the B1 channel.

The FSC (FST, Pin 14) is the input for the GCI frame synchronization signal. The signal at this pin is nominally rising edge aligned with the DCL clock signal. (Refer to Figure 6 and the GCI Timing specifications for more details.) This event identifies the beginning of the GCI frame. The frequency of the FSC synchronization signal is 8 kHz. The rising edge of the FSC (FST) should be aligned approximately with the rising edge of MCLK. MCLK must be one of the clock frequencies specified in the Digital Switching Characteristics table, and is typically tied to DCL (BCLKT).

The DCL (BCLKT, Pin 12) is the input for the clock that controls the PCM data transfers. The clock applied at the DCL input is twice the actual PCM data rate. The GCI frame begins with the logical AND of the FSC with the DCL. This event initiates the PCM data word transfers for both transmit and receive. This pin accepts a GCI data clock frequency of 512 kHz to 6.176 MHz for PCM data rates of 256 kHz to 3.088 MHz.

The GCI D_{out} (DT, Pin 13) is the output for the transmit PCM data word. Data bits are output for the B1 channel on alternate rising edges of the DCL clock signal, beginning with the FSC pulse. If the B2 channel is selected, then the PCM word transfer starts on the seventeenth DCL rising edge after the FSC rising edge. The D_{out} pin will remain low impedance for 15–1/2 DCL clock cycles. The D_{out} pin becomes high impedance after the second falling edge of the DCL clock during the LSB of the PCM word. The D_{out} pin will remain in a high–impedance state when not outputting PCM data or when a valid FSC signal is missing.

The D_{in} (DR, Pin 8) is the input for the receive PCM data word. Data bits are latched in for the B1 channel on alternate rising edges of the DCL clock signal, beginning with the second DCL clock after the rising edge of the FSC pulse. If the B2 channel is selected then the PCM word is latched in starting on the eighteenth DCL rising edge after the FSC rising edge.

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

The SE681512 is manufactured using high–speed CMOS VLSI technology to implement the complex analog signal processing functions of a PCM Codec–Filter. The fully–differential analog circuit design techniques used for this device result in superior performance for the switched capacitor filters, the analog–to–digital converter (ADC) and the digital–to–analog converter (DAC). Special attention was given to the design of this device to reduce the sensitivities of noise, including power supply rejection and susceptibility to radio frequency noise. This special attention to design includes a fifth order low–pass filter, followed by a third order high–pass filter whose output is converted to a digital signal with greater than 75 dB of dynamic range, all operating on a single 5 V power supply. This results in a Mu–Law LSB size for small audio signals of about 386 μV. The typical idle channel noise level of this device is less than one LSB. In addition to the dynamic range of the codec–filter function of this device, the input gain–setting op amp has the capability of greater than 35 dB of gain intended for an electret microphone interface.

This device was designed for ease of implementation, but due to the large dynamic range and the noisy nature of the environment for this device (digital switches, radio telephones, DSP front–end, etc.) special care must be taken to assure optimum analog transmission performance.

PC BOARD MOUNTING

It is recommended that the device be soldered to the PC board for optimum noise performance. If the device is to be used in a socket, it should be placed in a low parasitic pin inductance (generally, low–profile) socket.

POWER SUPPLY, GROUND, AND NOISE CONSIDERATIONS

This device is intended to be used in switching applications which often require plugging the PC board into a rack with power applied. This is known as "hot–rack insertion." In these applications care should be taken to limit the voltage on any pin from going positive of the V_{DD} pins, or negative of the V_{SS} pins. One method is to extend the ground and power contacts of the PCB connector. The device has input protection on all pins and may source or sink a limited amount of current without damage. Current limiting may be accomplished by series resistors between the signal pins and the connector contacts.

The most important considerations for PCB layout deal with noise. This includes noise on the power supply, noise generated by the digital circuitry on the device, and cross coupling digital or radio frequency signals into the audio signals of this device. The best way to prevent noise is to:

11. Keep digital signals as far away from audio signals as possible.
12. Keep radio frequency signals as far away from the audio signals as possible.
13. Use short, low inductance traces for the audio circuitry to reduce inductive, capacitive, and radio frequency noise sensitivities.
14. Use short, low inductance traces for digital and RF circuitry to reduce inductive, capacitive, and radio frequency radiated noise.
15. Bypass capacitors should be connected from the V_{DD} and V_{AG} pins to V_{SS} with minimal trace length. Ceramic monolithic capacitors of about 0.1 μF are acceptable to decouple the device from its own noise. The V_{DD} capacitor helps supply the instantaneous currents of the digital circuitry in addition to decoupling the noise which may be generated by other sections of the device or other circuitry on the power supply. The V_{AG} decoupling capacitor helps to reduce the impedance of the V_{AG} pin to V_{SS} at frequencies above the bandwidth of the V_{AG} generator, which reduces the susceptibility to RF noise.
16. Use a short, wide, low inductance trace to connect the V_{SS} ground pin to the power supply ground. The V_{SS} pin is the digital ground and the most negative power supply pin for the analog circuitry. All analog signal processing is referenced to the V_{AG} pin, but because digital and RF circuitry will probably be powered by this same ground, care must be taken to minimize high frequency noise in the V_{SS} trace. Depending on the application, a double–sided PCB with a V_{SS} ground plane connecting all of the digital and analog V_{SS} pins together would be a good grounding method. A multilayer PC board with a ground plane connecting all of the digital and analog V_{SS} pins together would be the optimal ground configuration. These methods will result in the lowest resistance and the lowest inductance in the ground circuit. This is important to reduce voltage spikes in the ground circuit resulting from the high speed digital current spikes. The magnitude of digitally induced voltage spikes may be hundreds of times larger than the analog signal the device is required to digitize.
17. Use a short, wide, low inductance trace to connect the V_{DD} power supply pin to the 5 V power supply. Depending on the application, a double–sided PCB with V_{DD} bypass capacitors to the V_{SS} ground plane, as described above, may complete the low impedance coupling for the power supply. For a multilayer PC board with a power plane, connecting all of the V_{DD} pins to the power plane would be the optimal power distribution method. The integrated circuit layout and packaging considerations for the 5 V V_{DD} power circuit are essentially the same as for the V_{SS} ground circuit.
18. The V_{AG} pin is the reference for all analog signal processing. In some applications the audio signal to be digitized may be referenced to the V_{SS} ground. To reduce the susceptibility to noise at the input of the ADC section, the three–terminal op amp may be used in a differential to single–ended circuit to provide level conversion from the V_{SS} ground to the V_{AG} ground with noise cancellation. The op amp may be used for more than 35 dB of gain in microphone interface circuits, which will require a compact layout with minimum trace lengths as well as isolation from noise sources. It is recommended that the layout be as symmetrical as possible to avoid any imbalances which would reduce the noise cancelling benefits of this differential op amp circuit. Refer to the application schematics for examples of this circuitry.

    If possible, reference audio signals to the V_{AG} pin instead of to the V_{SS} pin. Handset receivers and telephone line interface circuits using transformers may be audio signal referenced completely to the V_{AG} pin. Refer to the application schematics for examples of this circuitry. The V_{AG} pin cannot be used for ESD or line protection.
19. For applications using multiple SE681512 PCM Codec–Filters, the V_{AG} pins cannot be tied together. The V_{AG} pins are capable of sourcing and sinking current and will each be driving the node, which will result in large contention currents, crosstalk susceptibilities, and increased noise.
20. The SE681512 is fabricated with advanced high–speed CMOS technology that is capable of responding to noise pulses on the clock pins of 1 ns or less. It should be noted that noise pulses of such short duration may not be seen with oscilloscopes that have less bandwidth than 600 MHz. The most often encountered sources of clock noise spikes are inductive or capacitive coupling of high–speed logic signals, and ground bounce. The best solution for addressing clock spikes from coupling is to separate the traces and use short low inductance PC board traces. To address ground bounce problems, all integrated circuits should have high frequency bypass capacitors directly across their power supply pins, with low inductance traces for ground and power supply. A less than optimum solution may be to limit the bandwidth of the trace by adding series resistance and/or capacitance at the input pin.

MAXIMUM RATINGS (Voltages Referenced to V_{SS} Pin)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to 6	V
Voltage on Any Analog Input or Output Pin		V_{SS} – 0.3 to V_{DD} + 0.3	V
Voltage on Any Digital Input or Output Pin		V_{SS} – 0.3 to V_{DD} + 0.3	V
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 85 to +150	°C

POWER SUPPLY (T_A = – 40 to + 85°C)

Characteristics	Min	Typ	Max	Unit
DC Supply Voltage	4.75	5.0	5.25	V
Active Power Dissipation (V_{DD} = 5 V) (No Load, PI ≥ V_{DD} – 0.5 V) (No Load, PI ≤ V_{DD} – 1.5 V)	— —	***15*** ***15***	***24*** ***25***	mW
Power–Down Dissipation (V_{IH} for Logic Levels Must be ≥ 3.0 V) $\overline{PDI}$ = V_{SS} FST and FSR = V_{SS}, $\overline{PDI}$ = V_{DD}	— —	0.01 ***0.05***	0.5 1.0	mW

DIGITAL LEVELS (V_{DD} = + 5 V ± 5%, V_{SS} = 0 V, T_A = – 40 to + 85°C)

Characteristics	Symbol	Min	Max	Unit
Input Low Voltage	V_{IL}	—	0.6	V
Input High Voltage	V_{IH}	2.4	—	V
Output Low Voltage (DT Pin, I_{OL}= 2.5 mA)	V_{OL}	—	0.4	V
Output High Voltage (DT Pin, I_{OH} = – 2.5 mA)	V_{OH}	V_{DD} – 0.5	—	V
Input Low Current (V_{SS} ≤ V_{in} ≤ V_{DD})	I_{IL}	– 10	+ 10	μA
Input High Current (V_{SS} ≤ V_{in} ≤ V_{DD})	I_{IH}	– 10	+ 10	μA
Output Current in High Impedance State (V_{SS} ≤ DT ≤ V_{DD})	I_{OZ}	– 10	+ 10	μA
Input Capacitance of Digital Pins (Except DT)	C_{in}	—	10	pF
Input Capacitance of DT Pin when High–Z	C_{out}	—	15	pF

NOTE: Bold type indicates a change from the SE681512 to the SE681512.

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = + 5 V ± 5%, V_{SS} = 0 V, T_A = – 40 to + 85°C)

Characteristics		Min	Typ	Max	Unit
Input Current	TI+, TI–	—	± 0.1	± 1.0	µA
Input Resistance to V_{AG} (V_{AG} – 0.5 V ≤ V_{in} ≤ V_{AG} + 0.5 V)	TI+, TI–	***10***	**—**	—	MΩ
Input Capacitance	TI+, TI–	—	—	10	pF
Input Offset Voltage of TG Op Amp	TI+, TI–	—	—	± 5	mV
Input Common Mode Voltage Range	TI+, TI–	1.2		V_{DD} – 2.0	V
Input Common Mode Rejection Ratio	TI+, TI–	—	60	—	dB
Gain Bandwidth Product (10 kHz) of TG Op Amp (R_L ≥ 10 kΩ)		—	3000	—	kHz
DC Open Loop Gain of TG Op Amp (R_L ≥ 10 kΩ)		—	95	—	dB
Equivalent Input Noise (C–Message) Between TI+ and TI– at TG		—	– 30	—	dBrnC
Output Load Capacitance for TG Op Amp		0	—	100	pF
Output Voltage Range for TG (R_L = 10 kΩ to V_{AG}) (R_L = 2 kΩ to V_{AG})		 0.5 1.0	 — —	 V_{DD} – 0.5 V_{DD} – 1.0	V
Output Current (0.5 V ≤ V_{out} ≤ V_{DD} – 0.5 V)	TG, RO+, RO–	± 1.0	—	—	mA
Output Load Resistance to V_{AG}	TG, RO+, and RO–	2	—	—	kΩ
Output Impedance (0 to 3.4 kHz)	RO+ or RO–	—	1	—	Ω
Output Load Capacitance	RO+ or RO–	0	—	500	pF
DC Output Offset Voltage of RO+ or RO– Referenced to V_{AG}		—	—	± 25	mV
V_{AG} Output Voltage Referenced to V_{SS} (No Load)		2.2	2.4	2.6	V
V_{AG} Output Current with ± 25 mV Change in Output Voltage		± 2.0	± 10	—	mA
Power Supply Rejection Ratio (0 to 100 kHz @100 mVrms Applied to V_{DD}, C–Message Weighting, All Analog Signals Referenced to V_{AG} Pin)	Transmit Receive	50 50	80 75	— —	dBC
Power Drivers PI, PO+, PO–					
Input Current (V_{AG} – 0.5 V ≤ PI ≤ V_{AG} + 0.5 V)	PI	—	± 0.05	± 1.0	µA
Input Resistance (V_{AG} – 0.5 V ≤ PI ≤ V_{AG} + 0.5 V)	PI	10	—	—	MΩ
Input Offset Voltage	PI	—	—	± 20	mV
Output Offset Voltage of PO+ Relative to PO– (Inverted Unity Gain for PO–)		—	—	± 50	mV
Output Current (V_{SS} + 0.7 V ≤ PO+ or PO– ≤ V_{DD} – 0.7 V)		± 10	—	—	mA
PO+ or PO– Output Resistance (Inverted Unity Gain for PO–)		—	1	—	Ω
Gain Bandwidth Product (10 kHz, Open Loop for PO–)		—	1000	—	kHz
Load Capacitance (PO+ or PO– to V_{AG}, or PO+ to PO–)		0	—	1000	pF
Gain of PO+ Relative to PO– (R_L = 300 Ω, + 3 dBm0, 1 kHz)		– 0.2	0	+ 0.2	dB
Total Signal to Distortion at PO+ and PO– with a 300 Ω Differential Load		45	60	—	dBC
Power Supply Rejection Ratio (0 to 25 kHz @ 100 mVrms Applied to V_{DD}. PO– Connected to PI. Differential or Measured Referenced to V_{AG} Pin.)	0 to 4 kHz 4 to 25 kHz	40 —	55 40	— —	dB

NOTE: Bold type indicates a change from the SE681512 to the SE681512.

ANALOG TRANSMISSION PERFORMANCE

(V_{DD} = + 5 V ± 5%, V_{SS} = 0 V, All Analog Signals Referenced to V_{AG}, 0 dBm0 = 0.775 Vrms = + 0 dBm @ 600 Ω, FST = FSR = 8 kHz, BCLKT = MCLK = 2.048 MHz Synchronous Operation, T_A = – 40 to + 85°C, Unless Otherwise Noted)

Characteristics	End–to–End		A/D		D/A		Units
	Min	Max	Min	Max	Min	Max	
Absolute Gain (0 dBm0 @ 1.02 kHz, T_A = 25°C, V_{DD} = 5.0 V)	—	—	– 0.25	+ 0.25	– 0.25	+ 0.25	dB
Absolute Gain Variation with Temperature ***(Referenced to 25°C)***							
0 to + 70°C	—	—	—	± 0.03	—	± 0.03	dB
– 40 to + 85°C	—	—	—	± 0.05	—	± 0.05	
Absolute Gain Variation with Power Supply (T_A = 25°C)	—	—	—	± 0.03	—	± ***0.03***	dB
Gain vs Level Tone (Mu–Law, Relative to – 10 dBm0, 1.02 kHz)							
+ 3 to – 40 dBm0	—	—	***– 0.30***	***+ 0.20***	– 0.20	+ 0.20	dB
– 40 to – 50 dBm0	—	—	– 0.8	***+ 0.40***	***– 0.40***	***+ 0.40***	
– 50 to – 55 dBm0	—	—	***– 1.2***	***+ 0.80***	***– 0.80***	***+ 0.80***	
Gain vs Level Pseudo Noise, CCITT G.712 – 10 to – 40 dBm0	—	—	– 0.25	+ 0.25	– 0.25	+ 0.25	dB
(A–Law, Relative to – 10 dBm0) – 40 to – 50 dBm0	—	—	– 0.60	+ 0.30	– 0.30	+ 0.30	
– 50 to – 55 dBm0	—	—	– 1.00	+ 0.45	– 0.45	+ 0.45	
Total Distortion, 1.02 kHz Tone (Mu–Law, C–Message Weighting)							
+ 3 dBm0	—	—	34	—	34	—	dBC
0 to – 30 dBm0	—	—	36	—	36	—	
– 40 dBm0	—	—	30	—	30	—	
– 45 dBm0	—	—	25	—	25	—	
Total Distortion, Pseudo Noise, CCITT G.714 (A–Law) – 3 dBm0	—	—	30	—	30	—	dB
– 6 to – 27 dBm0	—	—	***36***	—	36	—	
– 34 dBm0	—	—	34	—	***35***	—	
– 40 dBm0	—	—	***29***	—	***30***	—	
– 50 dBm0	—	—	***19***	—	***20***	—	
– 55 dBm0	—	—	***14***	—	***15***	—	
Idle Channel Noise (For End–to–End and A/D, See Note 1)							
(Mu–Law, C–Message Weighted)	—	—	—	***17***	—	11	dBrnc0
(A–Law, Psophometric Weighted)	—	—	—	***– 69***	—	***– 79***	dBm0p
Frequency Response (Relative to 1.02 kHz @ 0 dBm0) 15 Hz	—	—	—	– 40	– 0.5	0	dB
50 Hz	—	—	—	– 30	– 0.5	0	
60 Hz	—	—	—	– 26	– 0.5	0	
200 Hz	—	—	– 1.0	– 0.4	– 0.5	0	
300 to 3000 Hz	—	—	– 0.20	+ 0.15	– 0.15	+ 0.15	
3000 to 3200 Hz	***—***	***—***	***– 0.20***	***+ 0.20***	***– 0.20***	***+ 0.20***	
3300 Hz	—	—	– 0.35	+ 0.15	– 0.35	+ 0.15	
3400 Hz	—	—	– 0.8	0	***– 0.85***	0	
4000 Hz	—	—	—	– 14	—	– 14	
4600 Hz to 100 kHz	—	—	—	– 32	—	30	
In–Band Spurious (1.02 kHz @ 0 dBm0, Transmit and Receive)							dB
300 to ***3400*** Hz	—	– 48	—	– 48	—	– 48	
Out–of–Band Spurious at RO+ (300 to 3400 Hz @ 0 dBm0 in)							
4600 to 7600 Hz	—	– 30	—	—	—	– 30	dB
7600 to 8400 Hz	—	– 40	—	—	—	– 40	
8400 to 100,000 Hz	—	– 30	—	—	—	– 30	
Idle Channel Noise Selective (8 kHz, Input = V_{AG}, 30 Hz Bandwidth)	—	– 70	—	—	—	– 70	dBm0
Absolute Delay (1600 Hz)	—	—	—	315	—	205	µs
Group Delay Referenced to 1600 Hz 500 to 600 Hz	—	—	—	210	– 40	—	µs
600 to 800 Hz	—	—	—	130	– 40	—	
800 to 1000 Hz	—	—	—	70	– 40	—	
1000 to 1600 Hz	—	—	—	35	– 30	—	
1600 to 2600 Hz	—	—	—	70	—	85	
2600 to 2800 Hz	—	—	—	95	—	110	
2800 to 3000 Hz	—	—	—	145	—	175	
Crosstalk of 1020 Hz @ 0 dBm0 from A/D or D/A (Note 2)	—	—	—	– 75	—	***– 75***	dB
Intermodulation Distortion of Two Frequencies of Amplitudes							dB
(– 4 to – 21 dBm0 from the Range 300 to 3400 Hz)	—	– 41	—	– 41	—	– 41	

NOTES:

1. Extrapolated from a 1020 Hz @ – 50 dBm0 distortion measurement to correct for encoder enhancement.
2. Selectively measured while stimulated with 2667 Hz @ – 50 dBm0.
3. **Bold type indicates a change from the SE681512 to the SE681512.**

DIGITAL SWITCHING CHARACTERISTICS, LONG FRAME SYNC AND SHORT FRAME SYNC

(V_{DD} = + 5 V ± 5%, V_{SS} = 0 V, All Digital Signals Referenced to V_{SS}, T_A = – 40 to + 85°C, C_L = 150 pF, Unless Otherwise Noted)

Ref. No.	Characteristics	Min	Typ	Max	Unit
1	Master Clock Frequency for MCLK	— — — — — — —	256 512 1536 1544 2048 2560 4096	— — — — — — —	kHz
1	MCLK Duty Cycle for 256 kHz Operation	45	—	55	%
2	Minimum Pulse Width High for MCLK (Frequencies of 512 kHz or Greater)	50	—	—	ns
3	Minimum Pulse Width Low for MCLK (Frequencies of 512 kHz or Greater)	50	—	—	ns
4	Rise Time for All Digital Signals	—	—	50	ns
5	Fall Time for All Digital Signals	—	—	50	ns
6	Setup Time from MCLK Low to FST High	50	—	—	ns
7	Setup Time from FST High to MCLK Low	50	—	—	ns
8	Bit Clock Data Rate for BCLKT or BCLKR	64	—	4096	kHz
9	Minimum Pulse Width High for BCLKT or BCLKR	50	—	—	ns
10	Minimum Pulse Width Low for BCLKT or BCLKR	50	—	—	ns
11	Hold Time from BCLKT (BCLKR) Low to FST (FSR) High	20	—	—	ns
12	Setup Time for FST (FSR) High to BCLKT (BCLKR) Low	80	—	—	ns
13	Setup Time from DR Valid to BCLKR Low	0	—	—	ns
14	Hold Time from BCLKR Low to DR Invalid	50	—	—	ns
	LONG FRAME SPECIFIC TIMING				
15	Hold Time from 2nd Period of BCLKT (BCLKR) Low to FST (FSR) Low	50	—	—	ns
16	Delay Time from FST or BCLKT, Whichever is Later, to DT for Valid MSB Data	—	—	60	ns
17	Delay Time from BCLKT High to DT for Valid Chord and Step Bit Data	—	—	60	ns
18	Delay Time from the Later of the 8th BCLKT Falling Edge, or the Falling Edge of FST to DT Output High Impedance	10	—	60	ns
19	Minimum Pulse Width Low for FST or FSR	50	—	—	ns
	SHORT FRAME SPECIFIC TIMING				
20	Hold Time from BCLKT (BCLKR) Low to FST (FSR) Low	50	—	—	ns
21	Setup Time from FST (FSR) Low to MSB Period of BCLKT (BCLKR) Low	50	—	—	ns
22	Delay Time from BCLKT High to DT Data Valid	10	—	60	ns
23	Delay Time from the 8th BCLKT Low to DT Output High Impedance	10	—	60	ns

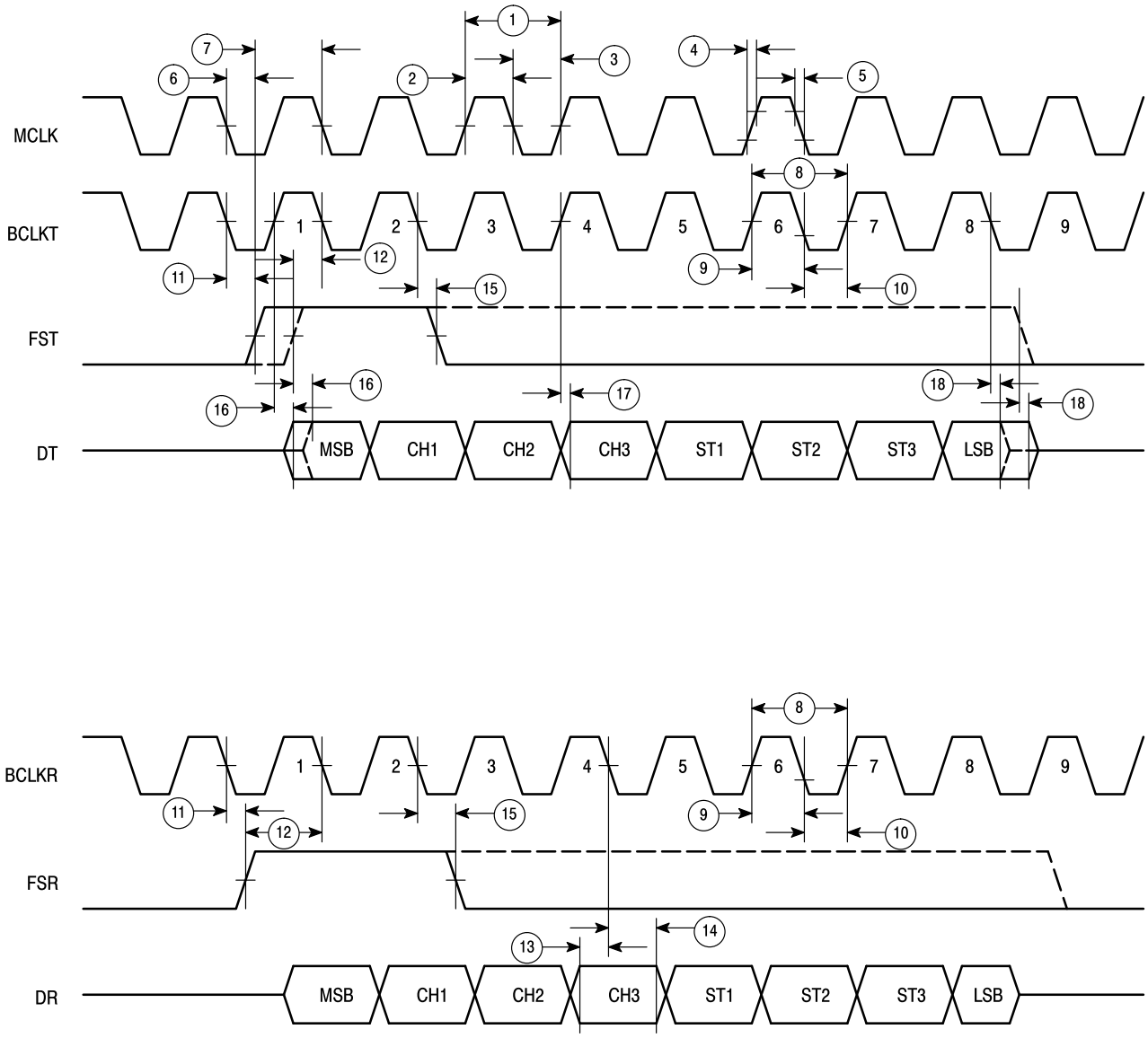


Figure 3. Long Frame Sync Timing

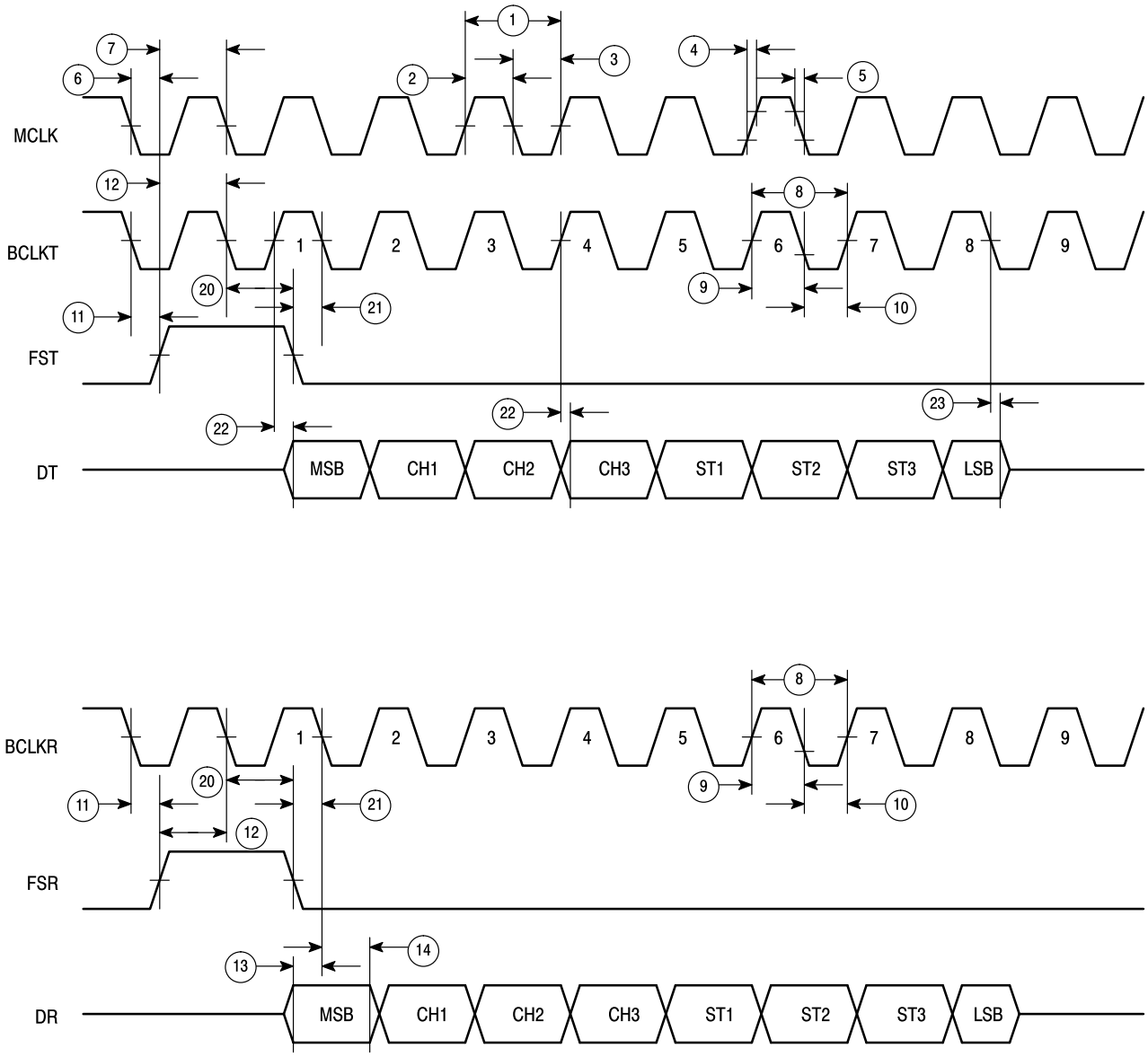


Figure 4. Short Frame Sync Timing

DIGITAL SWITCHING CHARACTERISTICS FOR IDL MODE

(V_{DD} = 5.0 V ± 5%, T_A = – 40 to + 85°C, C_L = 150 pF, See Figure 5 and Note 1)

Ref. No.	Characteristics	Min	Max	Unit
31	Time Between Successive IDL Syncs	Note 2		
32	Hold Time of IDL SYNC After Falling Edge of IDL CLK	20	—	ns
33	Setup Time of IDL SYNC Before Falling Edge IDL CLK	60	—	ns
34	IDL Clock Frequency	256	4096	kHz
35	IDL Clock Pulse Width High	50	—	ns
36	IDL Clock Pulse Width Low	50	—	ns
37	Data Valid on IDL RX Before Falling Edge of IDL CLK	20	—	ns
38	Data Valid on IDL RX After Falling Edge of IDL CLK	75	—	ns
39	Falling Edge of IDL CLK to High–Z on IDL TX	10	50	ns
40	Rising Edge of IDL CLK to Low–Z and Data Valid on IDL TX	10	60	ns
41	Rising Edge of IDL CLK to Data Valid on IDL TX	—	50	ns

NOTES:

1. Measurements are made from the point at which the logic signal achieves the guaranteed minimum or maximum logic level.
2. In IDL mode, both transmit and receive 8–bit PCM words are accessed during the B1 channel, or both transmit and receive 8–bit PCM words are accessed during the B2 channel as shown in Figure 5. IDL accesses must occur at a rate of 8 kHz (125 μs interval).

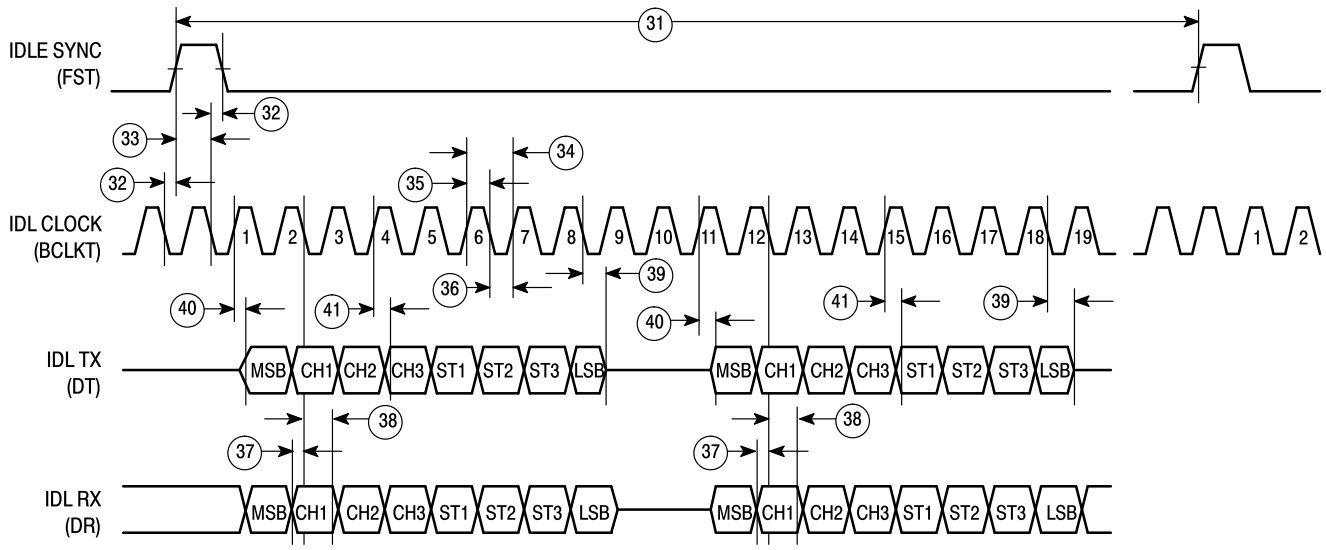


Figure 5. IDL Interface Timing

DIGITAL SWITCHING CHARACTERISTICS FOR GCI MODE

(V_{DD} = 5.0 V ± 5%, T_A = – 40 to + 85°C, C_L = 150 pF, See Figure 6 and Note 1)

Ref. No.	Characteristics	Min	Max	Unit
42	Time Between Successive FSC Pulses	Note 2		
43	DCL Clock Frequency	512	6176	kHz
44	DCL Clock Pulse Width High	50	—	ns
45	DCL Clock Pulse Width Low	50	—	ns
46	Hold Time of FSC After Falling Edge of DCL	20	—	ns
47	Setup Time of FSC to DCL Falling Edge	60	—	ns
48	Rising Edge of DCL (After Rising Edge of FSC) to Low Impedance and Valid Data of D_{out}	—	60	ns
49	Rising Edge of FSC (While DCL is High) to Low Impedance and Valid Data of D_{out}	—	60	ns
50	Rising Edge of DCL to Valid Data on D_{out}	—	60	ns
51	Second DCL Falling Edge During LSB to High Impedance of D_{out}	10	50	ns
52	Setup Time of D_{in} Before Rising Edge of DCL	20	—	ns
53	Hold Time of D_{in} After DCL Rising Edge	—	60	ns

NOTES:

1. Measurements are made from the point at which the logic signal achieves the guaranteed minimum or maximum logic level.
2. In GCI mode, both transmit and receive 8–bit PCM words are accessed during the B1 channel, or both transmit and receive 8–bit PCM words are accessed during the B2 channel as shown in Figure 6. GCI accesses must occur at a rate of 8 kHz (125 μs interval).

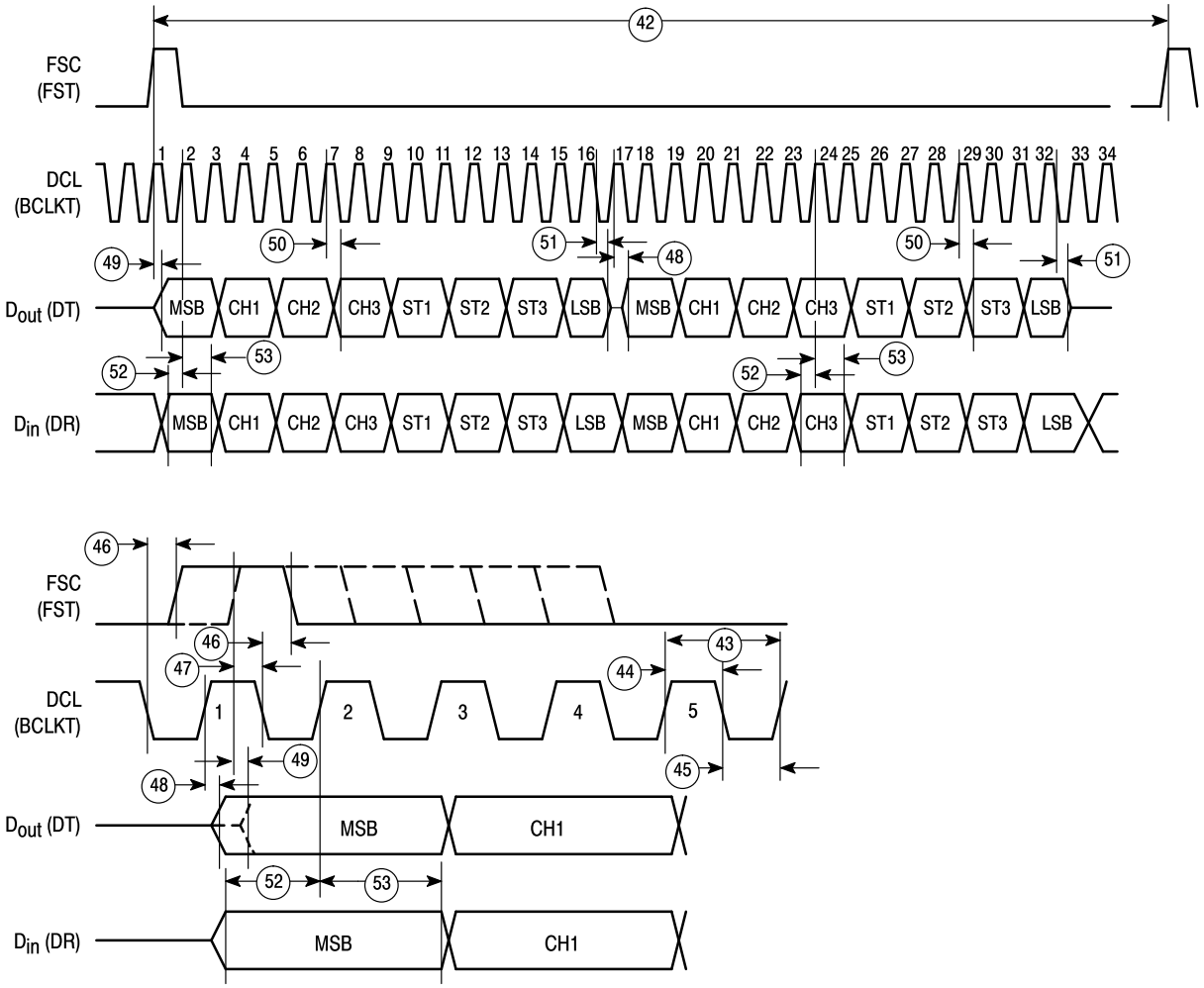


Figure 6. GCI Interface Timing

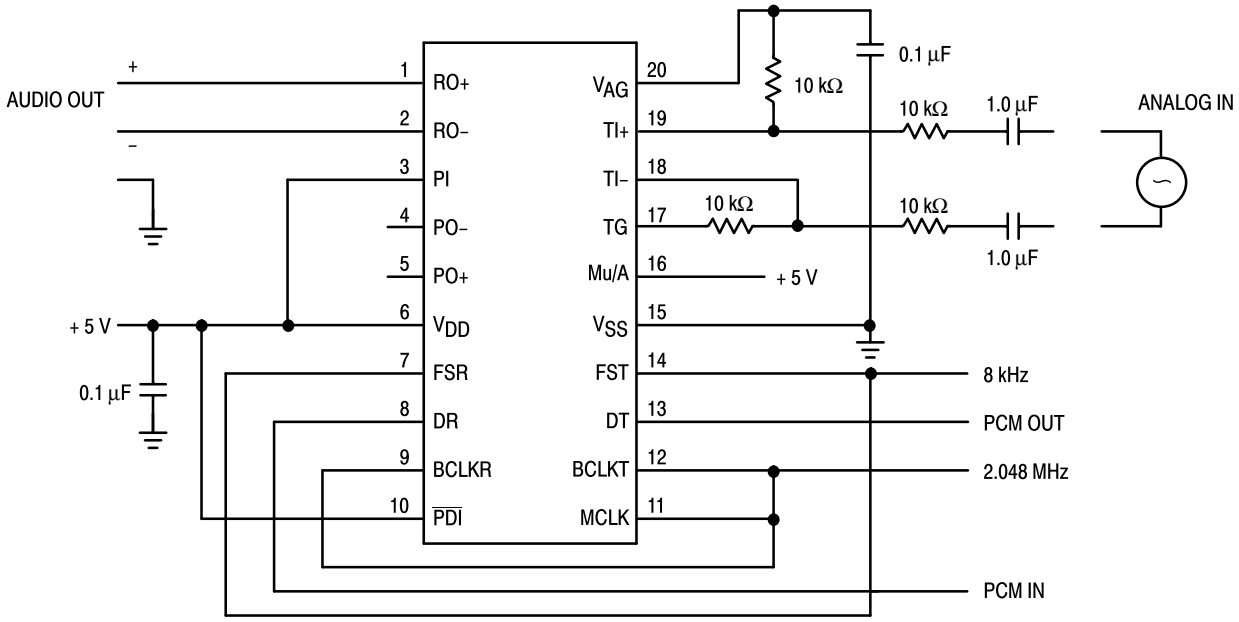


Figure 7. SE681512 Test Circuit with Differential Input and Output

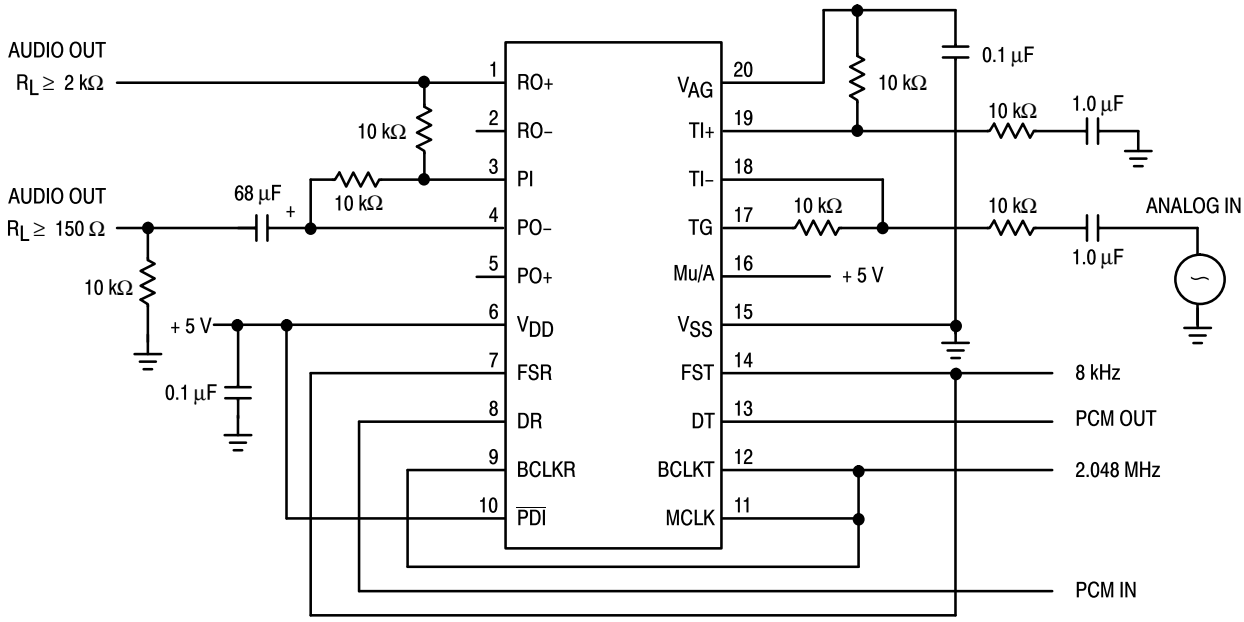


Figure 8. SE681512 Test Circuit with Input and Output Referenced to V_{SS}

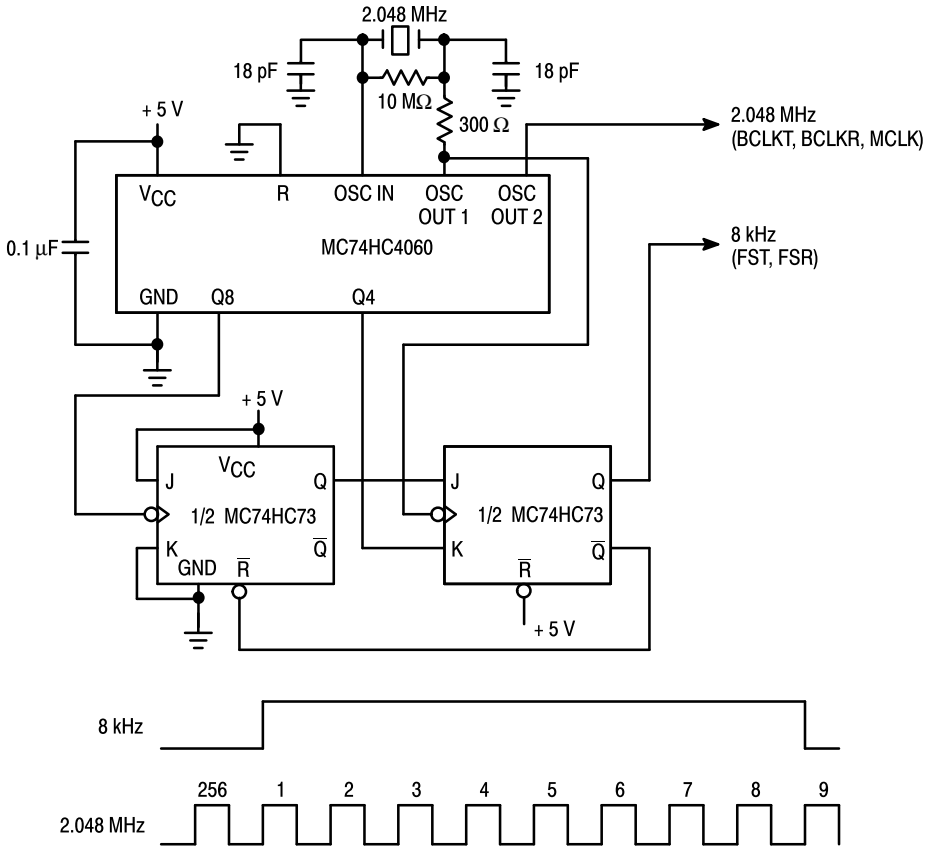


Figure 9. Long Frame Sync Clock Circuit for 2.048 MHz

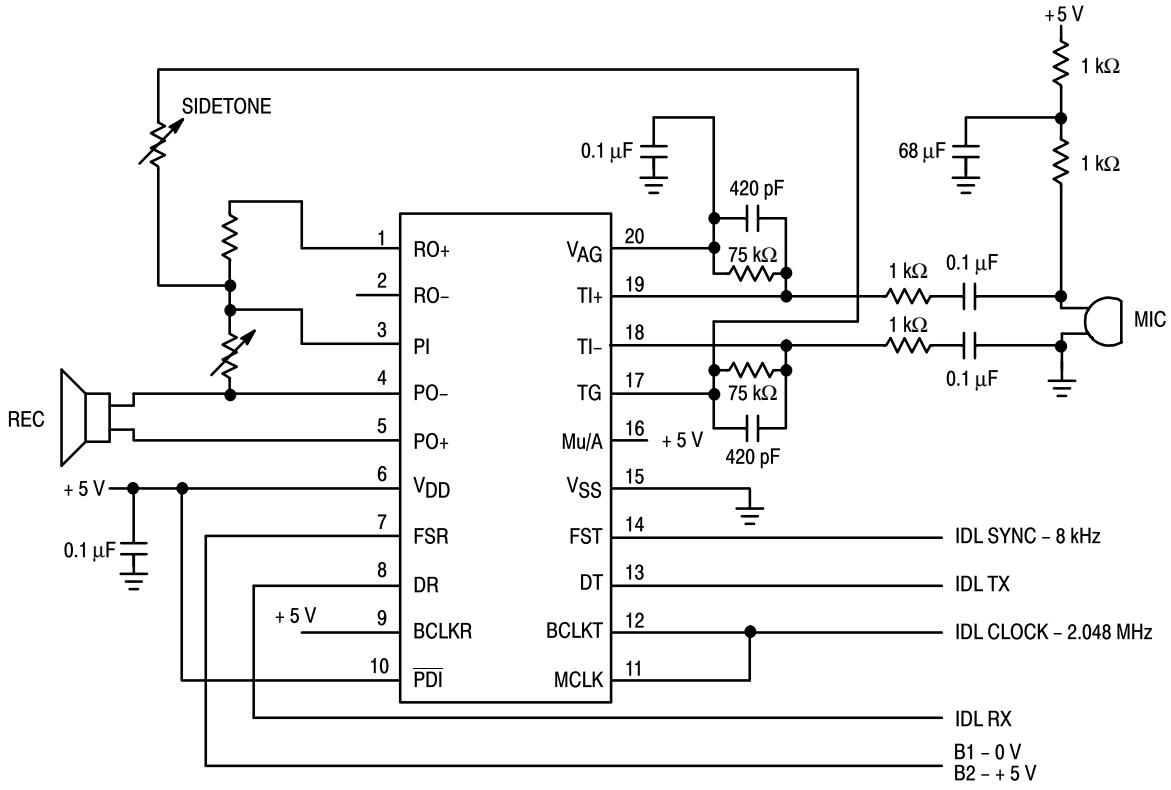


Figure 10. SE681512 Analog Interface to Handset with IDL Clocking

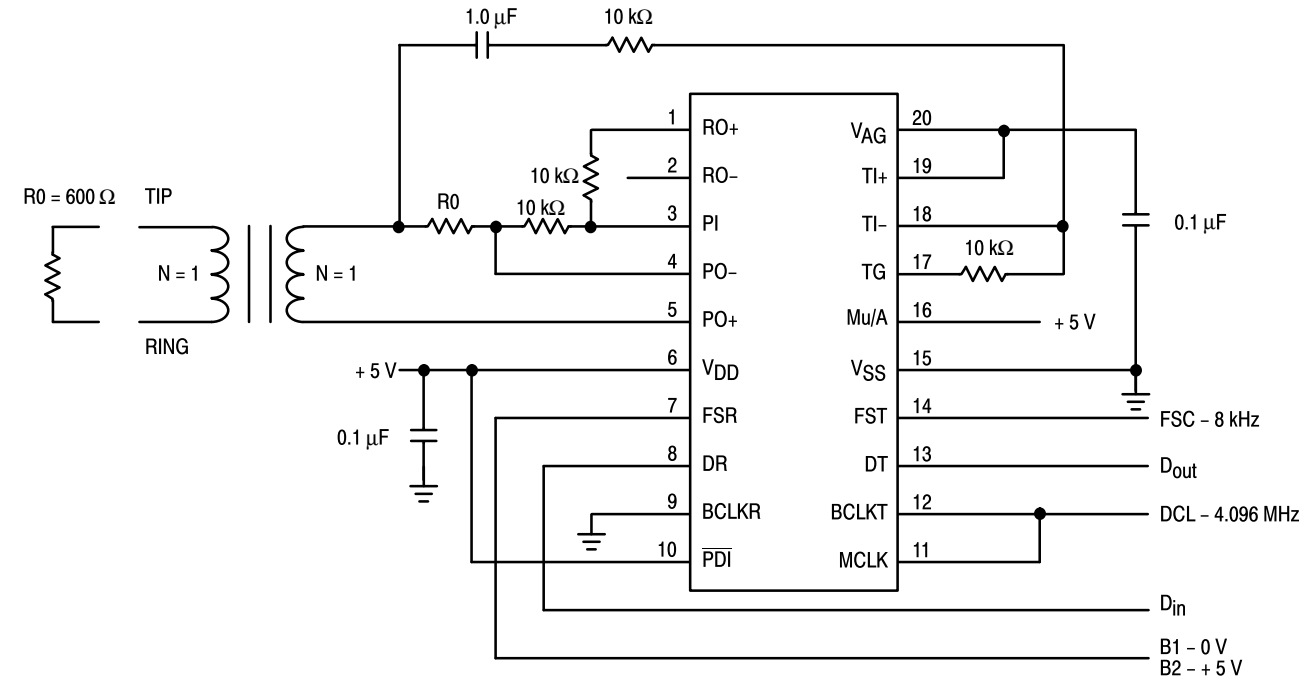


Figure 11. SE681512 Transformer Interface to 600 Ω Telephone Line with GCI Clocking

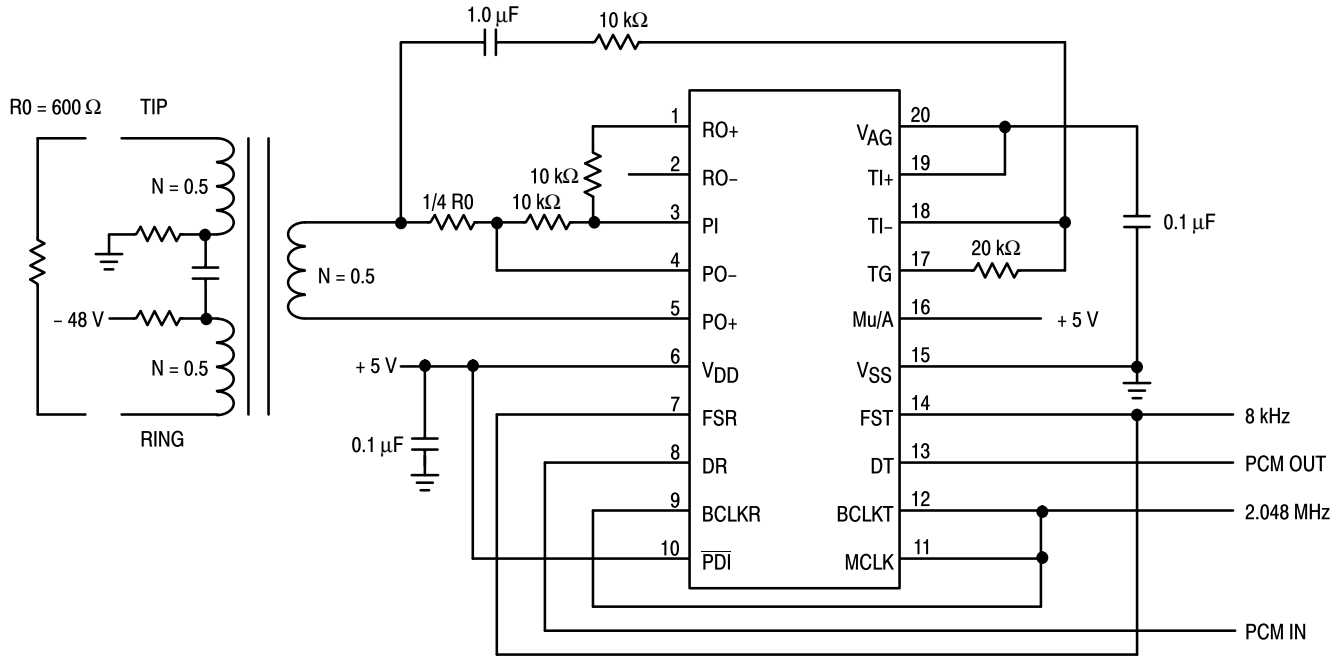


Figure 12. SE681512 Step–Up Transformer Interface to 600 Ω Telephone Line

Table 3. Mu–Law Encode–Decode Characteristics

Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code 1 Sign	2 Chord	3 Chord	4 Chord	5 Step	6 Step	7 Step	8 Step	Normalized Decode Levels
			8159									
8	16	256		1	0	0	0	0	0	0	0	8031
			7903 ⋮ 4319					⋮				⋮
				1	0	0	0	1	1	1	1	4191
7	16	128	4063 ⋮ 2143					⋮				⋮
				1	0	0	1	1	1	1	1	2079
6	16	64	2015 ⋮ 1055					⋮				⋮
				1	0	1	0	1	1	1	1	1023
5	16	32	991 ⋮ 511					⋮				⋮
				1	0	1	1	1	1	1	1	495
4	16	16	479 ⋮ 239					⋮				⋮
				1	1	0	0	1	1	1	1	231
3	16	8	223 ⋮ 103					⋮				⋮
				1	1	0	1	1	1	1	1	99
2	16	4	95 ⋮ 35					⋮				⋮
				1	1	1	0	1	1	1	1	33
1	15	2	31 ⋮ 3					⋮				⋮
				1	1	1	1	1	1	1	0	2
	1	1	1	1	1	1	1	1	1	1	1	0
			0									

NOTES:
1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes inversion of all magnitude bits.

Table 4. A–Law Encode–Decode Characteristics

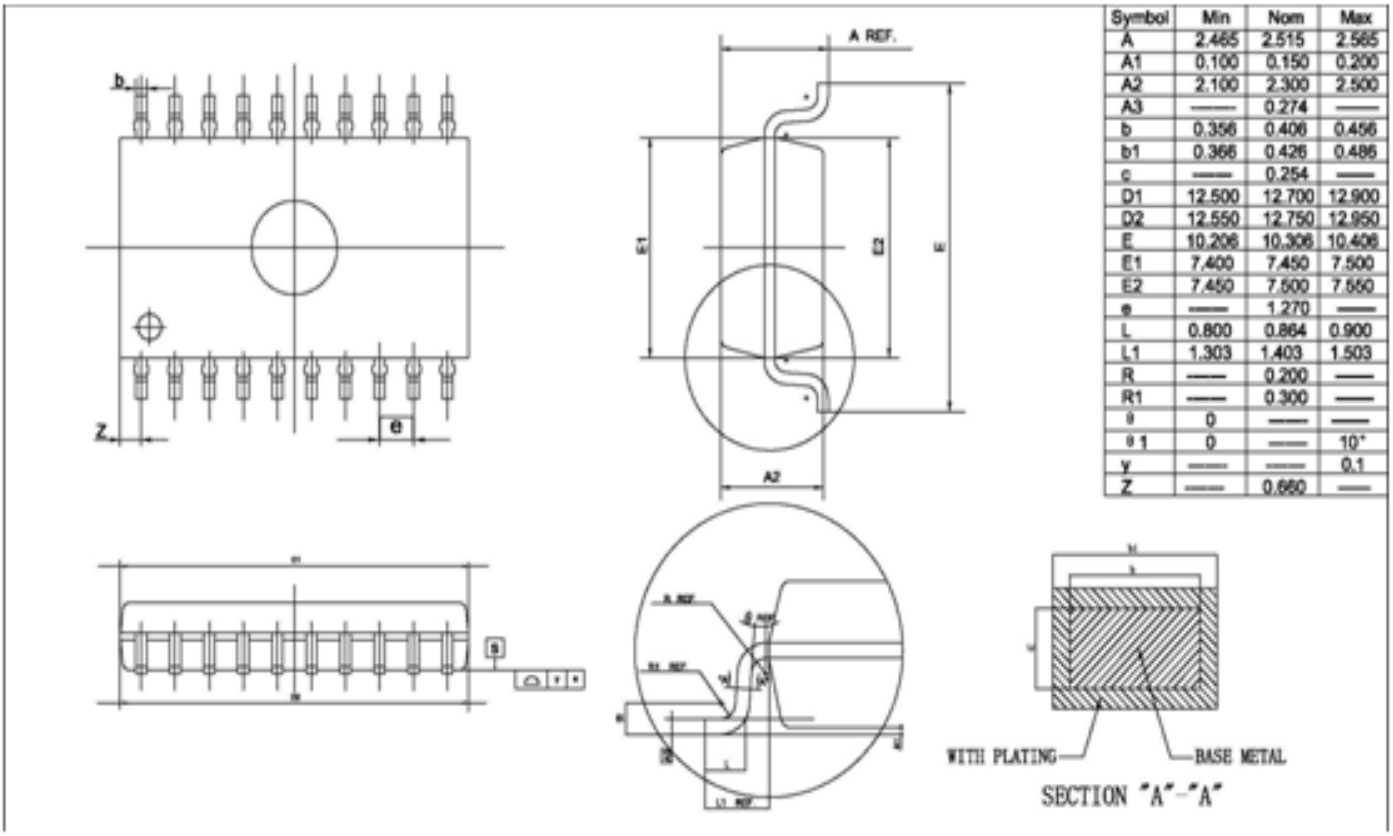
Chord Number	Number of Steps	Step Size	Normalized Encode Decision Levels	Digital Code 1 Sign	2 Chord	3 Chord	4 Chord	5 Step	6 Step	7 Step	8 Step	Normalized Decode Levels
			4096									
7	16	128		1	0	1	0	1	0	1	0	4032
			3968 ⋮					⋮				⋮
			2176	1	0	1	0	0	1	0	1	2112
6	16	64	2048 ⋮					⋮				⋮
			1088	1	0	1	1	0	1	0	1	1056
5	16	32	1024 ⋮					⋮				⋮
			544	1	0	0	0	0	1	0	1	528
4	16	16	512 ⋮					⋮				⋮
			272	1	0	0	1	0	1	0	1	264
3	16	8	256 ⋮					⋮				⋮
			136	1	1	1	0	0	1	0	1	132
2	16	4	128 ⋮					⋮				⋮
			68	1	1	1	1	0	1	0	1	66
1	32	2	64 ⋮					⋮				⋮
			2	1	1	0	1	0	1	0	1	1
			0									

NOTES:

1. Characteristics are symmetrical about analog zero with sign bit = 0 for negative analog values.
2. Digital code includes inversion of all even numbered bits.

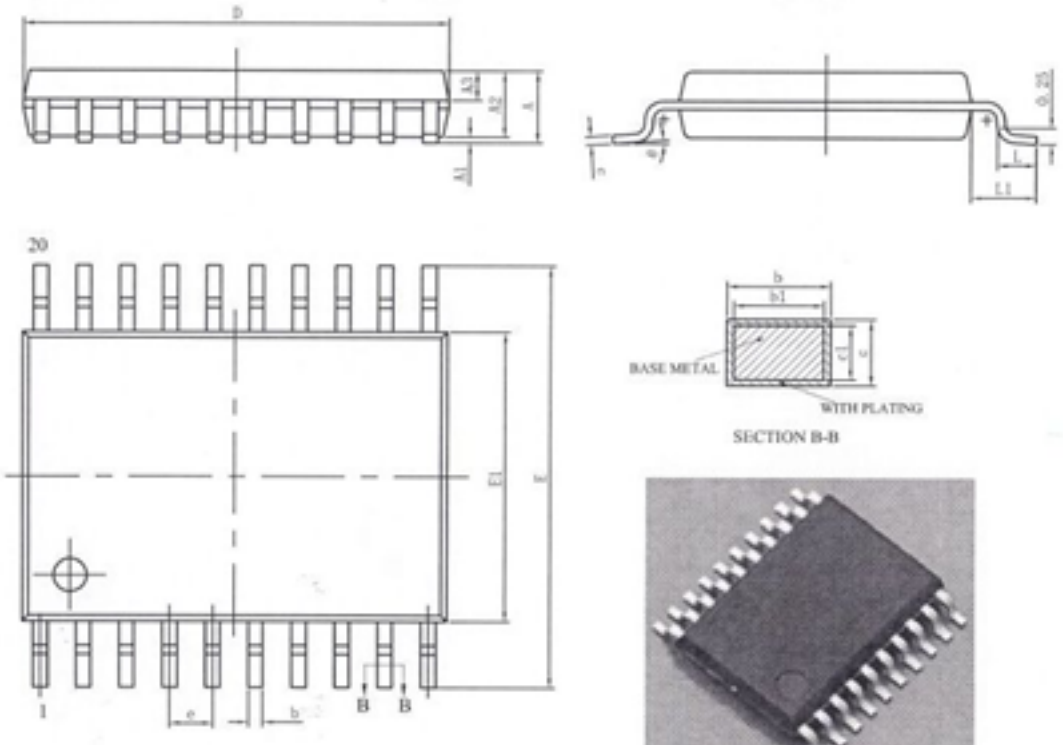
PACKAGE DIMENSIONS

SOP20L



Symbol	Min	Nom	Max
A	2.465	2.515	2.565
A1	0.100	0.150	0.200
A2	2.100	2.300	2.500
A3	——	0.274	——
b	0.356	0.406	0.456
b1	0.366	0.426	0.486
c	——	0.254	——
D1	12.500	12.700	12.900
D2	12.550	12.750	12.950
E	10.206	10.306	10.406
E1	7.400	7.450	7.500
E2	7.450	7.500	7.550
e	——	1.270	——
L	0.800	0.864	0.900
L1	1.303	1.403	1.503
R	——	0.200	——
R1	——	0.300	——
θ	0	——	——
θ1	0	——	10°
y	——	——	0.1
Z	——	0.660	——

TSSOP20



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.29
b1	0.19	0.22	0.25
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°

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