



# XTSD01G/XTSD02G/XTSD04G/XTSD08G

## SD NAND

## Datasheet

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## 1. Introduction

XTX SD NAND is an embedded storage solution designed in a LGA8 package form. The operation of SD NAND is similar to an SD card which is an industry standard.

SD NAND consists of NAND flash and a high performance controller. 3.3V supply voltage is required for the NAND area (VCC). SD NAND is fully compliant with SD2.0 interface, which allows most of general CPU to utilize. SD NAND has high performance at a competitive cost, high quality and low power consumption.

## 2. Product List

| Capacity | Part number   | Package                | Size  |
|----------|---------------|------------------------|-------|
| 1Gb      | XTSD01GLGEAG  | LGA8 (Land Grid Array) | 8x6mm |
|          | XTSD01GDLGEGA | LGA8 (Land Grid Array) | 8x6mm |
|          | XTSD01GCLGEGA | LGA8 (Land Grid Array) | 8x6mm |
|          | XTSD01GBLGEGA | LGA8 (Land Grid Array) | 8x6mm |
| 2Gb      | XTSD02GLGEAG  | LGA8 (Land Grid Array) | 8x6mm |
| 4Gb      | XTSD04GLGEAG  | LGA8 (Land Grid Array) | 8x6mm |
|          | XTSD04GCLGEGA | LGA8 (Land Grid Array) | 8x6mm |
| 8Gb      | XTSD08GLGEAG  | LGA8 (Land Grid Array) | 8x6mm |
|          | XTSD08GCLGEGA | LGA8 (Land Grid Array) | 8x6mm |

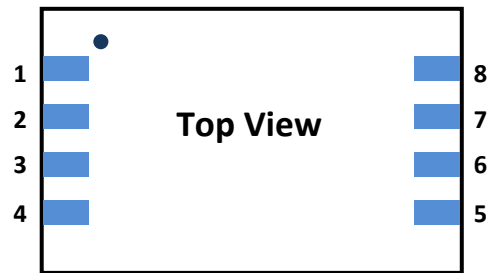
## 3. Features

- Support up to 50Mhz clock frequency
- Support 1/4 bit mode
- Built-in HW ECC Engine and highly reliable NAND management mechanism
- Write speed up to class 8
- Smaller package LGA8 (Land Grid Array)

## 4. Physical Characteristic Temperature

- Operation Conditions  
Temperature Range: Ta = -30 to +85 degrees centigrade
- Storage Conditions  
Temperature Range: Tstg = -40 to +85 degrees centigrade

## 5. Pin Assignments



| Pin No. | Pin name (SD mode)  | Pin name (SPI mode) |
|---------|---------------------|---------------------|
| 1       | SD2, I/O pin        | NC, no connection   |
| 2       | SD3, I/O pin        | /CS, chip select    |
| 3       | CLK, clock signal   | CLK, clock signal   |
| 4       | Vss, ground         | Vss, ground         |
| 5       | CMD, command signal | DI, data in         |
| 6       | SD0, I/O pin        | DO, data out        |
| 7       | SD1, I/O pin        | NC, no connection   |
| 8       | Vdd, power supply   | Vdd, power supply   |

## 6. Usage

### 6.1. Product Protocol

As SD NAND is the realize SD2.0 standard product, thus please refer to the SD2.0 related protocol : SD Physical Layer Specification Version 2.00.

### 6.2. DC Characteristics

| Item                     | Symbol           | MIN             | MAX       | Unit      | Note                              |                                      |
|--------------------------|------------------|-----------------|-----------|-----------|-----------------------------------|--------------------------------------|
| Supply voltage           | VDD              | 2.7             | 3.6       | V         |                                   |                                      |
| Input voltage            | High Level       | V <sub>IH</sub> | VDD*0.625 | VDD+0.3   | V                                 |                                      |
|                          | Low Level        | V <sub>IL</sub> | VSS-0.3   | VDD*0.25  | V                                 |                                      |
| Output voltage           | High Level       | V <sub>OH</sub> | VDD*0.75  | --        | V                                 | I <sub>OH</sub> =-2mA,<br>VDD=VDDmin |
|                          | Low Level        | V <sub>CL</sub> | --        | VDD*0.125 | V                                 | I <sub>OL</sub> =2ma,<br>VDD=VDDmin  |
| Standby Current(*)       | I <sub>cc1</sub> | --              | 20*       | mA        | VDD=3.6V,<br>clock 25MHz          |                                      |
|                          |                  | --              | 0.2       |           | VDD=3.0V, clock<br>STOP, Ta=25° C |                                      |
| Operation Current(*)     | Write            | I               | --        | 30        | mA                                | 3.6V/25MHz,50MHz                     |
|                          | Read             | I               | --        | 30        |                                   |                                      |
| Input voltage setup Time | V <sub>rs</sub>  | --              | 250       | ms        |                                   |                                      |

Note: Standby current max 20mA with CLOCK 25Mhz only based on 100 pcs samples

#### Peak Voltage and Leak Current

| Item                                   | Symbol | MIN  | MAX     | Unit | Note |
|--|--------|------|---------|------|------|
| Peak voltage on all lines              |        | -0.3 | VDD+0.3 | V    |      |
| Input Leakage Current for all pins     |        | -10  | 10      | uA   |      |
| Output Leakage Current for all outputs |        | -10  | 10      | uA   |      |

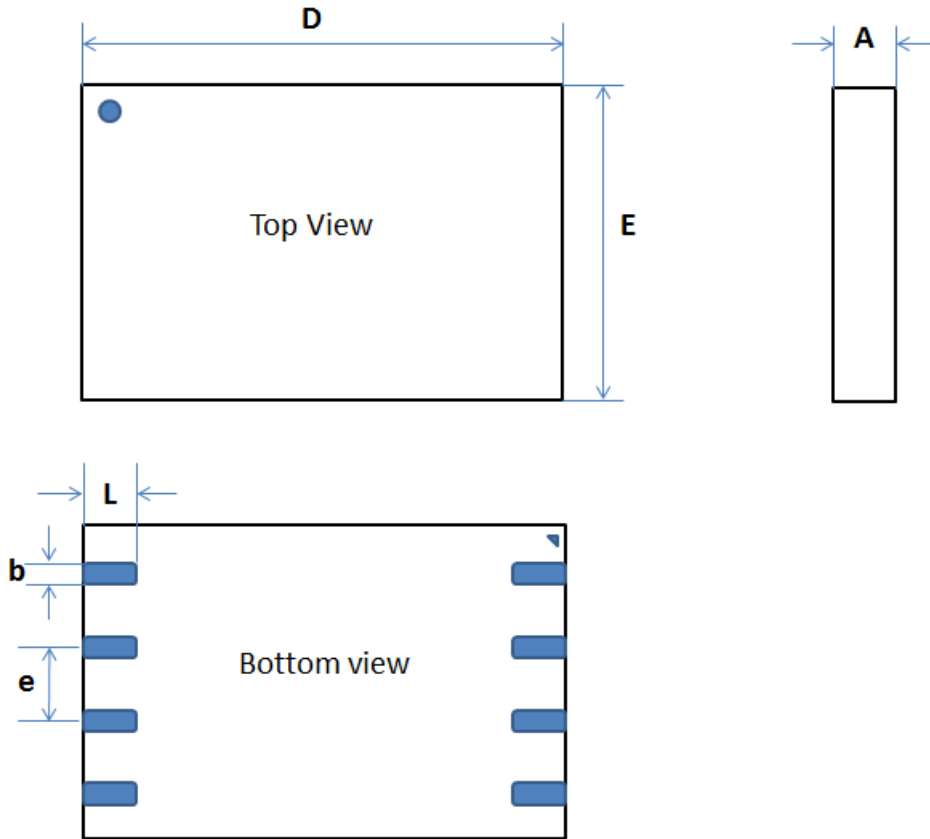
#### Signal Capacitance

| Item                                       | Symbol                             | MIN | MAX | Unit | Note   |
|--|------------------------------------|-----|-----|------|--|
| Pull up Resistance                         | R <sub>CMD</sub> /R <sub>DAT</sub> | 10  | 100 | k    |  |
| Total bus capacitance for each signal line | C <sub>L</sub>                     | -   | 40  | pF   | 1 card<br>C <sub>HOST</sub> +C <sub>BUS</sub> ≤ 30pF |
| Card Capacitance for signal pin            | C <sub>CARD</sub>                  | -   | 10  | pF   |  |
| Pull up Resistance inside card (pin1)      | R <sub>DAT3</sub>                  | 10  | 90  | k    |  |
| Capacity Connected to Power line           | C <sub>C</sub>                     | -   | 5   | pF   |  |

Note: WP pull-up (R<sub>wp</sub>) Value is depend on the Host Interface drive circuit.

## 7. Package Dimensions

### LGA8 (8\*6mm) (Land Grid Array)

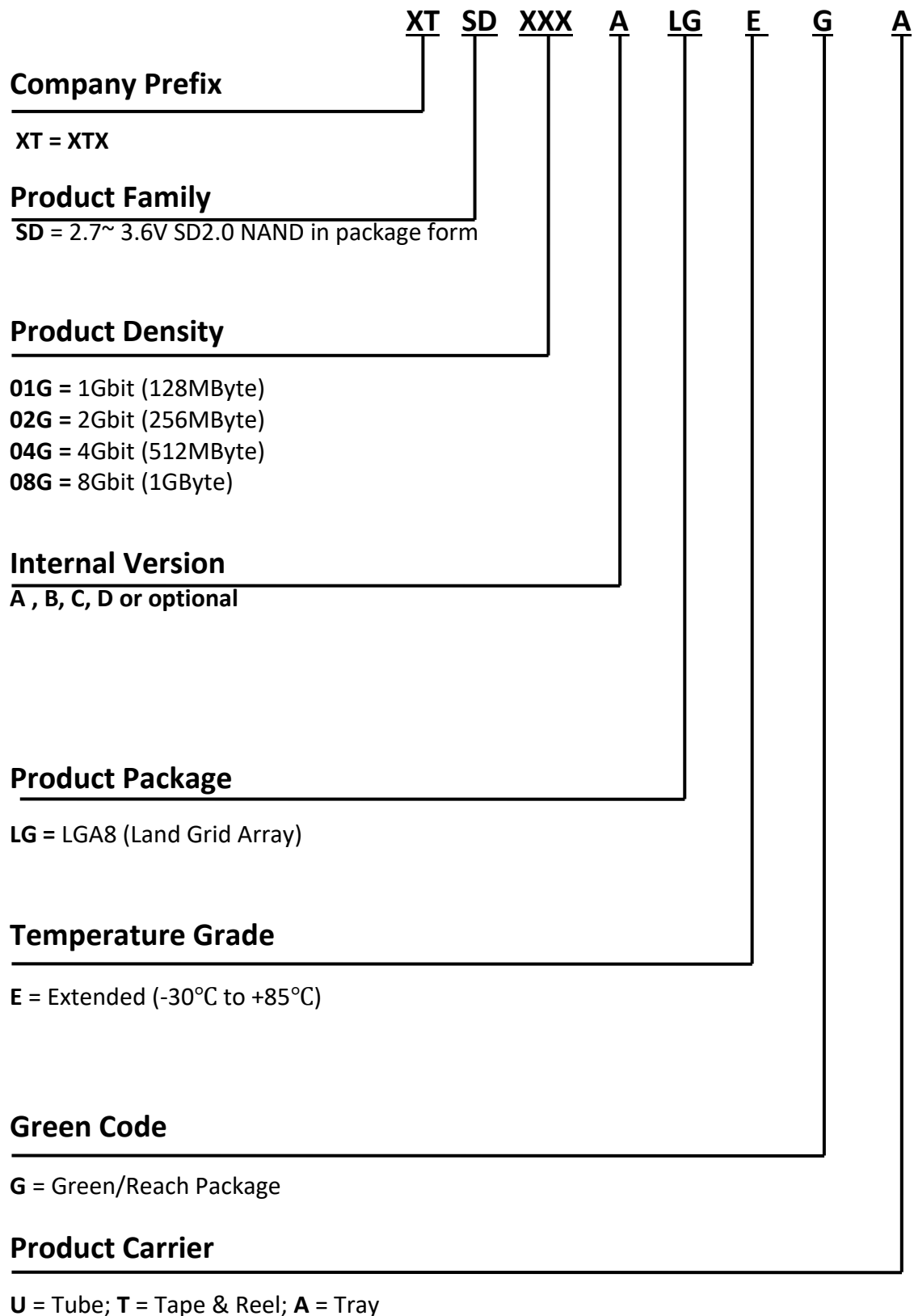


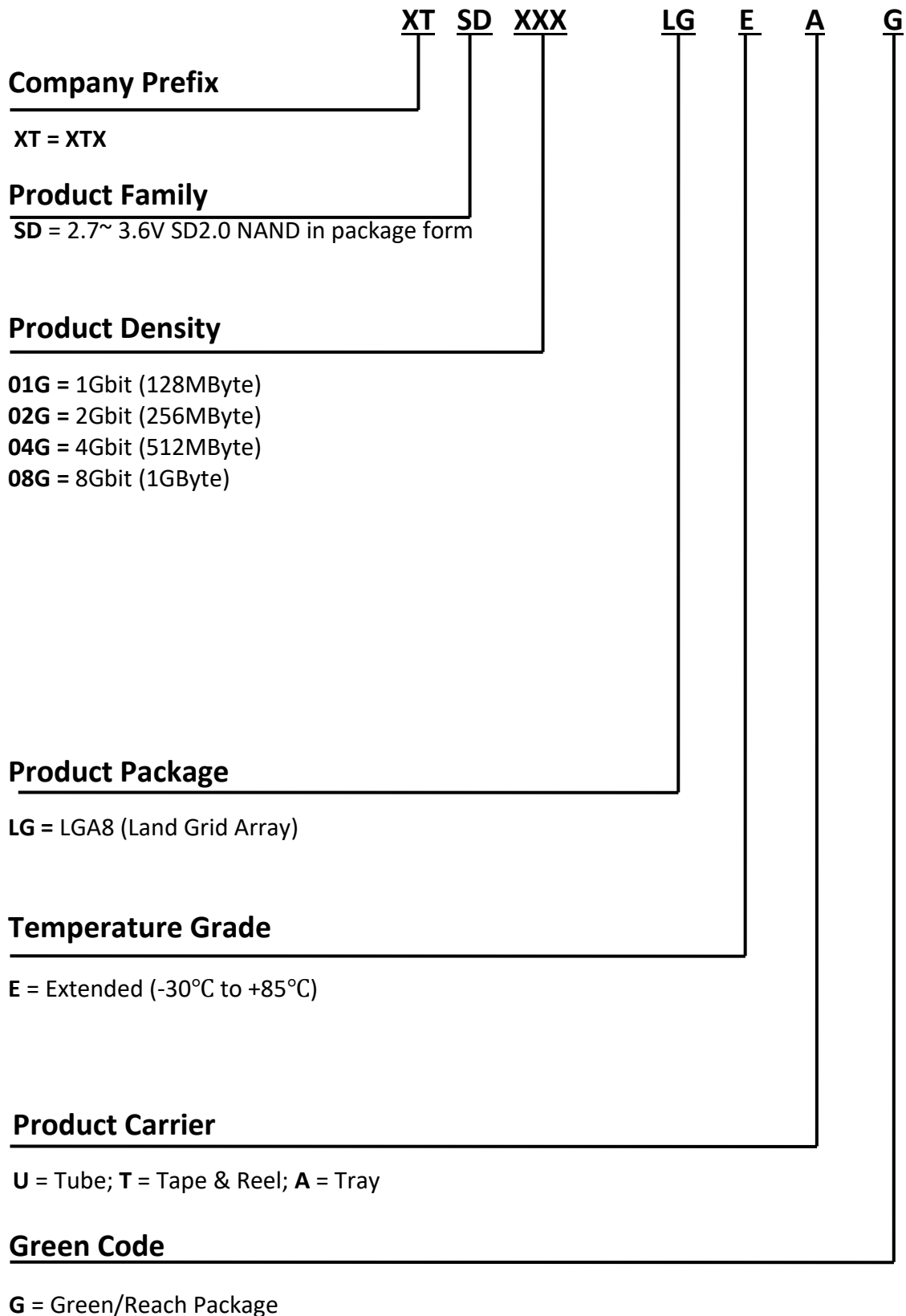
Dimensions

| Symbol |      | A    |  |  | b    | D    |  | E    |  | e    |  | L    |
|--------|------|------|--|--|------|------|--|------|--|------|--|------|
| Unit   |      |      |  |  |      |      |  |      |  |      |  |      |
| Mm     | Min  | 0.85 |  |  | 0.55 | 7.95 |  | 5.95 |  |      |  | 0.75 |
|        | Norm | 0.90 |  |  | 0.60 | 8.00 |  | 6.00 |  | 1.27 |  | 0.80 |
|        | Max  | 0.95 |  |  | 0.65 | 8.05 |  | 6.05 |  |      |  | 0.85 |

## 8. Ordering Information

The ordering part number is formed by a valid combination of the following







## 9. Revision History

| Version No. | Change Description  | Date       |
|-------------|---|------------|
| V1.0        | Initial release, part number is based on extended temperature, WSON 8*6mm package, tape & reel packing, 1Gb/2Gb/4Gb density were included.  | 2017/1/10  |
| V1.1        | Add 8Gb density, and correct some typos;  | 2017/1/10  |
| V2.1        | Part number change from PNSDxxGWS to PNSDxxGLG;<br>Package change from WSON8 to LGA8;<br>Package dimension b change from 0.7mm to 0.6mm;<br>Package dimension picture updated without the dissipating pad;<br>Add a page for part number description; | 2017/1/22  |
| V2.2        | Modify part number description; Page head re-layout;  | 2017/1/23  |
| V2.3        | Add SPI mode pin description  | 2017/2/1   |
| V2.4        | Set default Part number and PNSDxxGLGEAG (tray packing)   | 2017/2/14  |
| V2.5        | Part number update from PNSDxxxx to XTSDxxxx  | 2017/3/3   |
| V2.6        | Rename company name to XTX  | 2017/3/23  |
| V2.7        | Revise page #8,9 & 10 register table to include 8Gb, add cover page & page  | 2018/4/2   |
| V2.8        | Revise page #7 leakage unit error correction to uA.   | 2018/4/25  |
| V2.9        | Revise OPN to new ordering format & add new OPN, include manual content option  | 2018/10/23 |
| V3.0        | Remove the Incomplete SD protocol and correct the ordering information  | 2019/2/27  |
| V3.1        | Revise the ordering information   | 2019/5/15  |

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