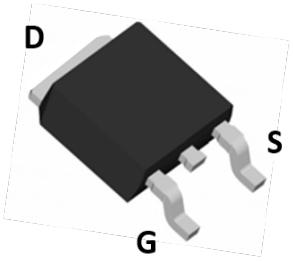
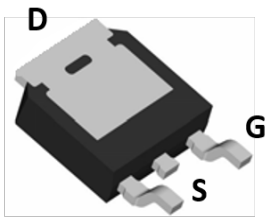
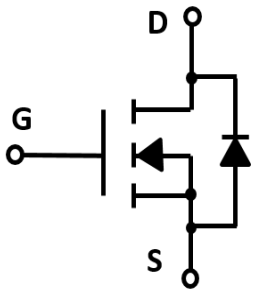
N-Channel Enhancement Mode Field Effect Transistor





TO-252



Product Summary

- V_{DS} 40 V
- I_D 120 A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜3.5 mohm
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜4.8 mohm
- 100% UIS Tested
- 100% ▽V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- DC-DC Converters
- Power management functions
- Backlighting

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current	T_C=25℃	I_D	120	A
	T_C=100℃		76	
Pulsed Drain Current [A]		I_{DM}	390	A
Total Power Dissipation @ T_C=25℃ [B]		P_D	110	W
Total Power Dissipation @ T_C=100℃ [B]		P_D	44	W
Total Power Dissipation @ T_A=25℃ [C]		P_D	6.2	W
Single Pulse Avalanche Energy [D]		E_{AS}	272	mJ
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	1.14	℃/ W
Thermal Resistance Junction-to-Ambient		$R_{\theta JA}$	20	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJD120N04A	F2	YJD120N04A	2500	/	25000	13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	40			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=15A		2.8	3.5	mΩ
		V_{GS}= 4.5V, I_D=10A		4.0	4.8	
Diode Forward Voltage	V_{SD}	I_S=15A,V_{GS}=0V		0.80	1.2	V
Maximum Body-Diode Continuous Current	I_S				120	A
Gate resistance	Rg	f=1 MHz, Open drain		3.1		Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=20V,V_{GS}=0V,f=1MHZ		4645		pF
Output Capacitance	C_{oss}			436		
Reverse Transfer Capacitance	C_{rss}			360		
Switching Parameters						
Total Gate Charge	Q_g(10V)	V_{GS}=10V,V_{DS}=20V,I_D=20A		102		nC
Total Gate Charge	Q_g(4.5V)			49		
Gate-Source Charge	Q_{gs}			15.8		
Gate-Drain Charge	Q_{gd}			21.9		
Reverse Recovery Charge	Q_{rr}	I_F=20A, di/dt=100A/us		7.4		
Reverse Recovery Time	t_{rr}			22.3		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=20V , I_D=20A R_{GEN}=3Ω		12		
Turn-on Rise Time	t_r			54		
Turn-off Delay Time	$t_{D(off)}$			120		
Turn-off fall Time	t_f			80		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150℃, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. The value of $R_{\theta JA}$ is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25℃.
D. T_j=25℃, V_{DD}=40V, V_G=10V, L=0.5mH.

■ Typical Performance Characteristics

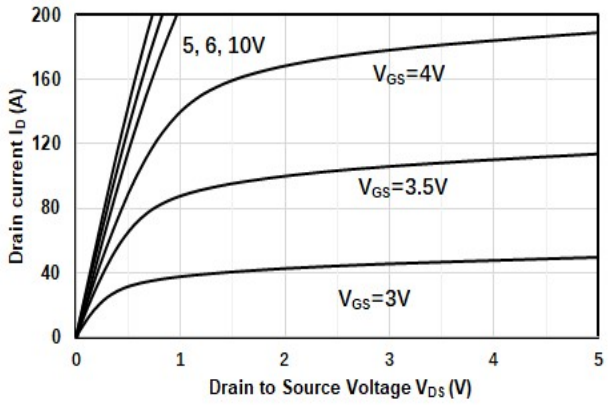


Figure1. Output Characteristics

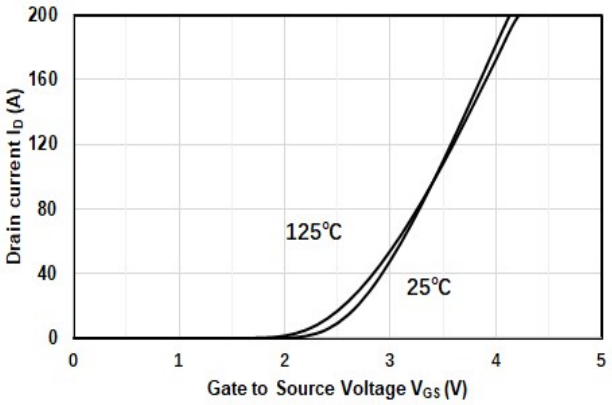


Figure2. Transfer Characteristics

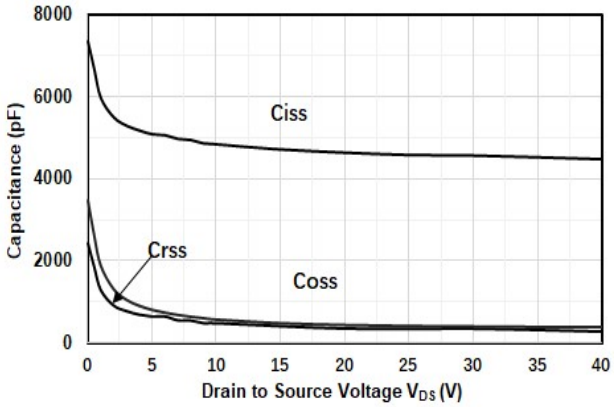


Figure3. Capacitance Characteristics

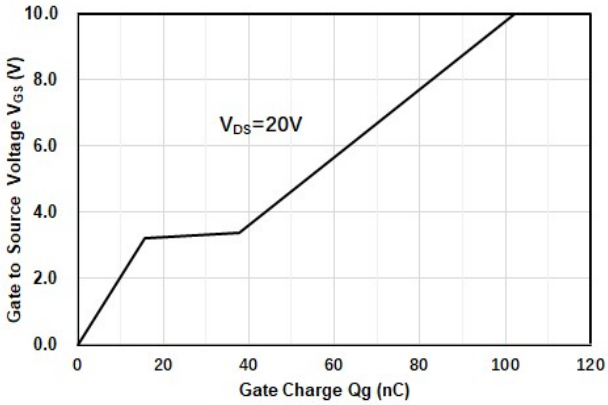


Figure4. Gate Charge

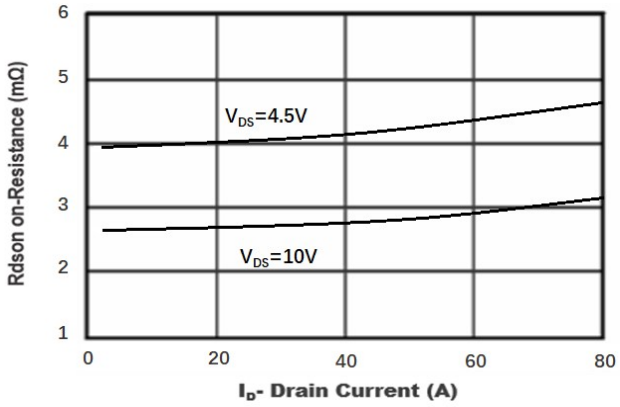


Figure5. Drain-Source on Resistance

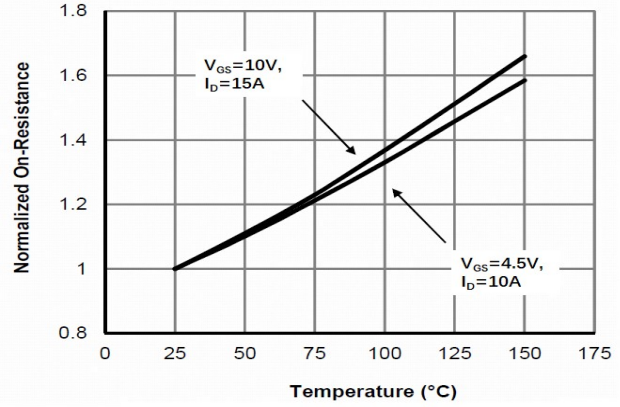


Figure6. Drain-Source on Resistance

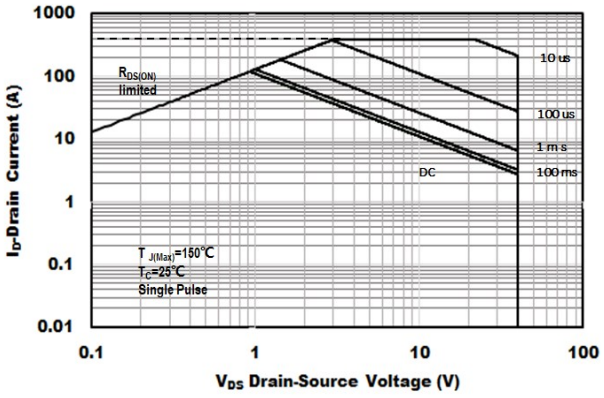


Figure7. Safe Operation Area

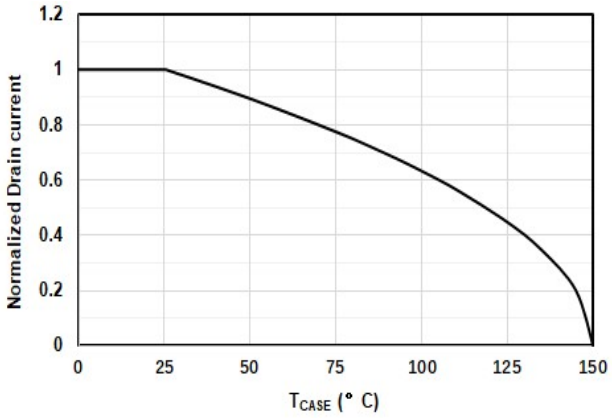


Figure8. Drain current vs. Case Temperature

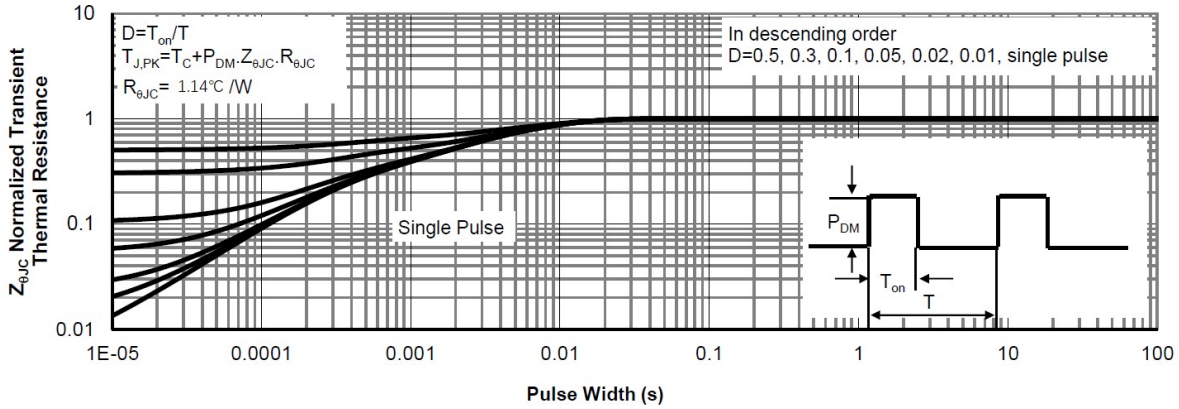
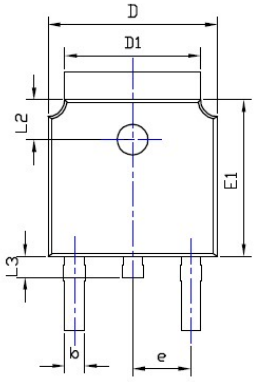
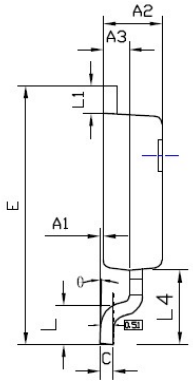


Figure9. Normalized Maximum Transient Thermal Impedance

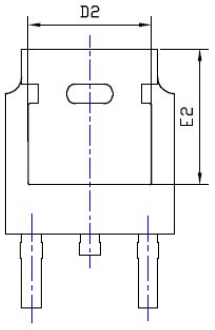
■TO-252 Package information



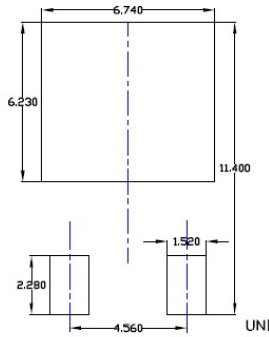
TOP VIEW



SIDE VIEW



BOTTOM VIEW



UNIT: mm

SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS					
	INCHES			Millmeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.008	0.000	---	0.200
A2	0.087	0.091	0.094	2.200	2.300	2.400
A3	0.035	0.039	0.043	0.900	1.000	1.100
b	0.026	0.030	0.034	0.660	0.760	0.860
c	0.018	0.020	0.023	0.460	0.520	0.580
D	0.256	0.260	0.264	6.500	6.600	6.700
D1	0.203	0.209	0.215	5.150	5.300	5.450
D2	0.181	0.189	0.195	4.600	4.800	4.950
E	0.390	0.398	0.406	9.900	10.100	10.300
E1	0.236	0.240	0.244	6.000	6.100	6.200
E2	0.203	0.209	0.215	5.150	5.300	5.450
e	0.090BSC			2.286BSC		
L	0.049	0.059	0.069	1.250	1.500	1.750
L1	0.035	---	0.050	0.900	---	1.270
L2	0.055	---	0.075	1.400	---	1.900
L3	0.240	0.310	0.039	0.600	0.800	1.000
L4	0.114REF			2.900REF		
θ	0°	---	10°	0°	---	10°

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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