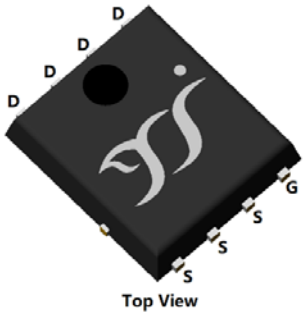
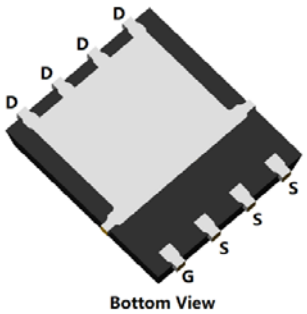
P-Channel Enhancement Mode Field Effect Transistor

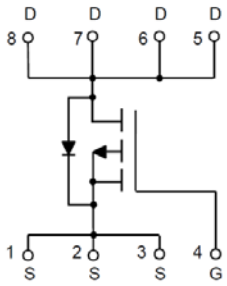


Top View



Bottom View

PDFN5060-8L



Product Summary

- V_{DS} -30V
- I_D -70A
- $R_{DS(ON)}$(at V_{GS}=-10V) ＜5.5mohm
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜9.5mohm
- 100% EAS Tested
- 100% ▽VDS Tested

General Description

- Trench Power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Battery management
- Load switch
- Power management

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-30	V
Gate-source Voltage		V_{GS}	±25	V
Drain Current	T_C=25℃	I_D	-70	A
	T_C=100℃		-44	
Pulsed Drain Current [A]		I_{DM}	-280	A
Total Power Dissipation	T_C=25℃	P_D	89	W
	T_C=100℃		36	W
Total Power Dissipation	T_A=25℃	P_D	7.4	W
Single Pulse Avalanche Energy [B]		E_{AS}	360	mJ
Thermal Resistance Junction-to-Case [C]		$R_{\theta JC}$	1.4	℃/ W
Thermal Resistance Junction-to-Ambient [C]		$R_{\theta JA}$	17	℃/ W
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG70P03A	F1	YJG70P03A	5000	10000	100000	13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Static Parameter							
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA		-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V	T_J=25℃			-1	μA
			T_J=55℃			-5	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±25V, V_{DS}=0V				±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA		-1.2	-1.8	-2.8	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= -10V, I_D=-20A			4.0	5.5	mΩ
		V_{GS}= -4.5V, I_D=-20A			6.0	9.5	
Diode Forward Voltage	V_{SD}	I_S=-20A,V_{GS}=0V				-1.2	V
Maximum Body-Diode Continuous Current	I_S					-70	A
Dynamic Parameters							
Input Capacitance	C_{iss}	V_{DS}=-15V,V_{GS}=0V,f=1MHZ			6464		pF
Output Capacitance	C_{oss}				779		
Reverse Transfer Capacitance	C_{rss}				477		
Gate Resistance	Rg	Drain open, f=1Mhz			6.5		Ω
Switching Parameters							
Total Gate Charge	Q_g	V_{GS}=-10V,V_{DS}=-15V,I_D=-20A			111.7		nC
Gate-Source Charge	Q_{gs}				21.1		
Gate-Drain Charge	Q_{gd}				22.9		
Reverse Recovery Charge	Q_{rr}	I_F=-15A, di/dt=-100A/us			8.5		
Reverse Recovery Time	t_{rr}				24		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}= -10V,V_{DD}= -15V,R_G=3Ω,R_L= 0.75Ω			15		
Turn-on Rise Time	t_r				75		
Turn-off Delay Time	$t_{D(off)}$				130		
Turn-off fall Time	t_f				80		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. T_j=25℃, V_{DD}=-25V, V_G=-10V, L=2mH, I_{AS}=-19A.

C. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the soldermounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics

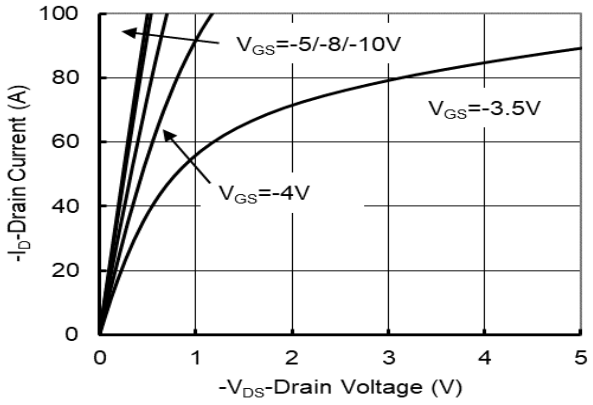


Figure1. Output Characteristics

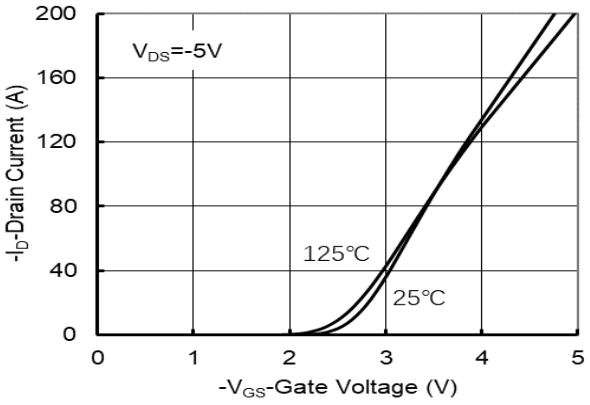


Figure2. Transfer Characteristics

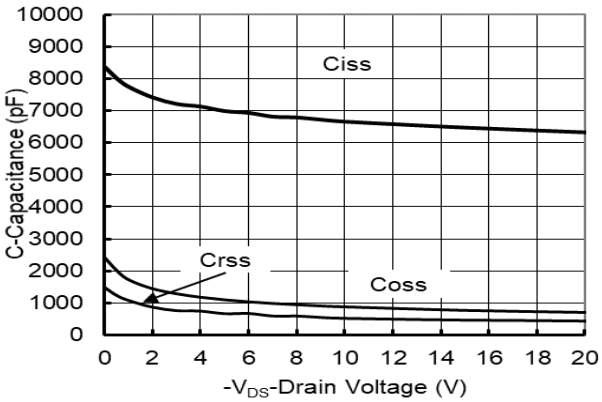


Figure3. Capacitance Characteristics

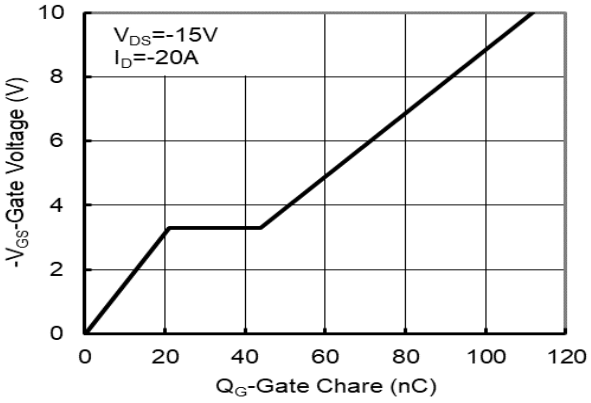


Figure4. Gate Charge

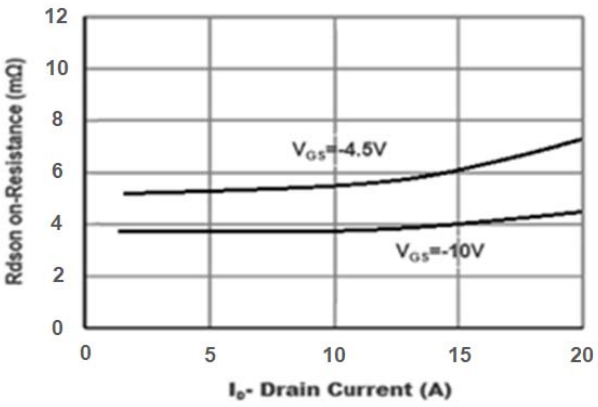


Figure5. Drain-Source on Resistance

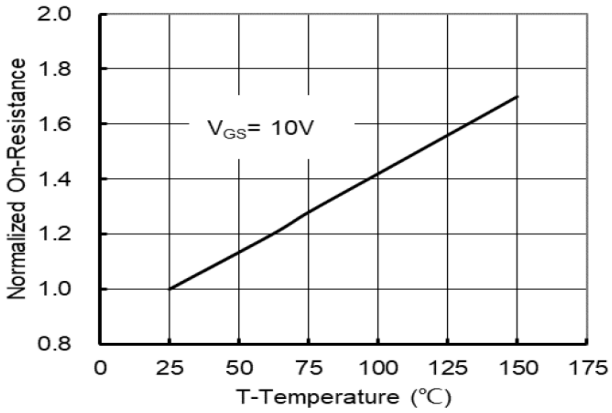


Figure6. Drain-Source on Resistance

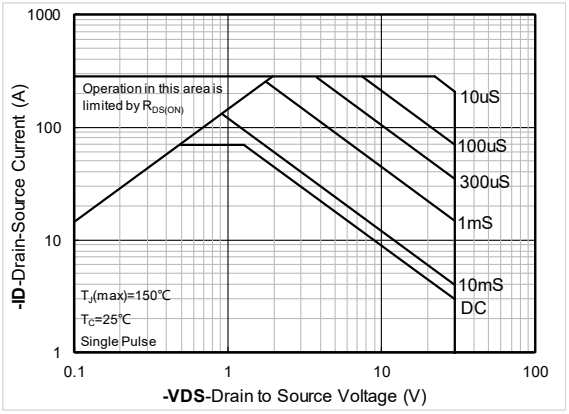


Figure7. Safe Operation Area

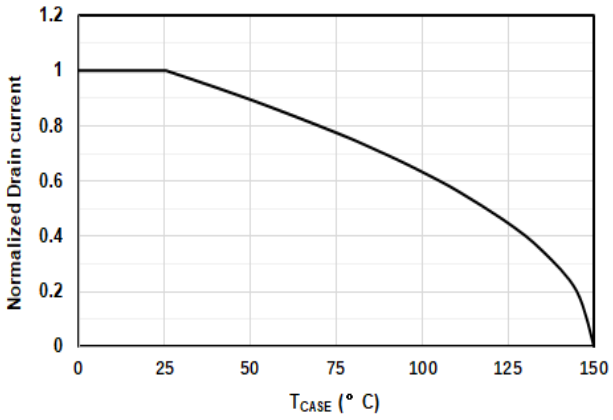


Figure8. Drain current vs. Case Temperature

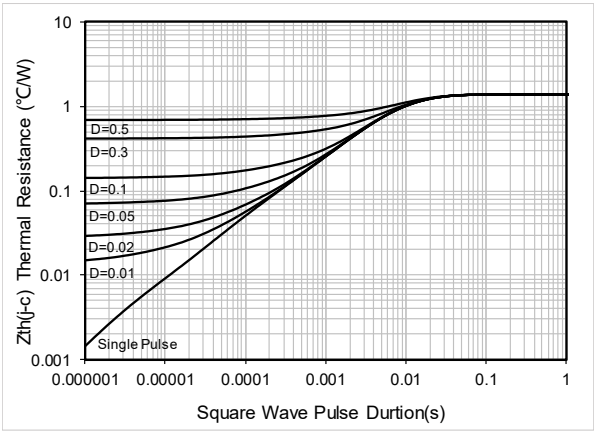
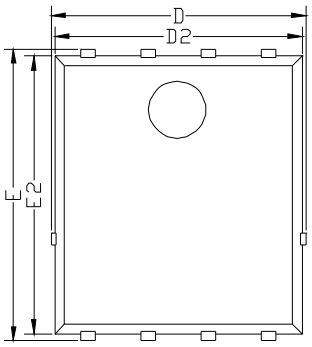
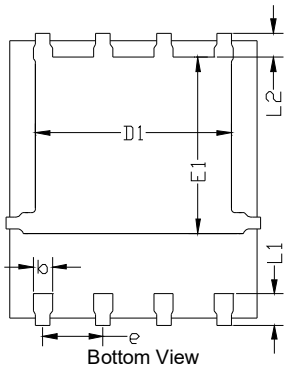


Figure9. Normalized Maximum Transient Thermal Impedance

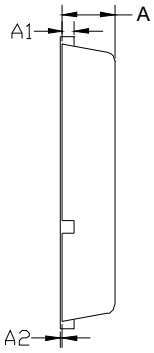
■ PDFN5060-8L Package information



Top View
正面视图



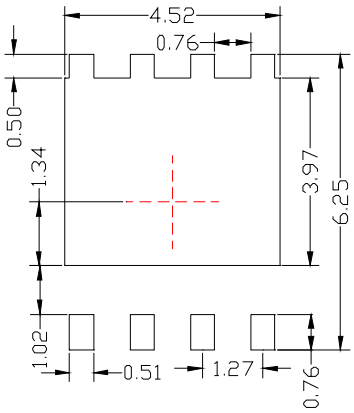
Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:+/-0.10mm.
3.The pad layout is for reference purposes only.



Suggested Solder Pad Layout
Top View

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