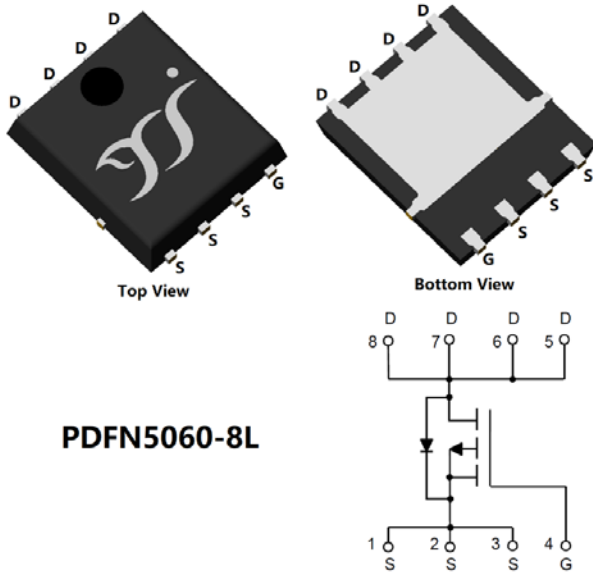


P-Channel Enhancement Mode Field Effect Transistor



PDFN5060-8L

Product Summary

- V_{DS} -60 V
- I_D -80 A
- $R_{DS(ON)}$ (at $V_{GS}=-10V$) <8.5m Ω
- 100% UIS Tested
- 100% ∇V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Low $R_{DS(on)}$ & FOM
- Excellent stability and uniformity
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- Power management
- Portable equipment
- 12 and 24V Automotive systems

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-60	V
Gate-source Voltage		V_{GS}	± 18	V
Drain Current	$T_A=25^\circ C$	I_D	-12	A
	$T_A=100^\circ C$		-7.5	
	$T_C=25^\circ C$		-80	
	$T_C=100^\circ C$		-50	
Pulsed Drain Current ^A		I_{DM}	-320	A
Avalanche energy ^B		EAS	400	mJ
Total Power Dissipation ^C	$T_A=25^\circ C$	P_D	2.5	W
	$T_A=100^\circ C$		1	
	$T_C=25^\circ C$		120	
	$T_C=100^\circ C$		48	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 ~ +150	$^\circ C$

■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient ^D	Steady-State	$R_{\theta JA}$	40	50	$^\circ C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.8	1.04	



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■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG80GP06BQ	F1	YJG80GP06B	5000	10000	100000	13" reel

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-60V, V _{GS} =0V	-	-	-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±18V, V _{DS} =0V	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-2	-2.7	-4	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-20A	-	6.1	8.5	mΩ
Diode Forward Voltage	V _{SD}	I _S =-20A, V _{GS} =0V	-	-0.9	-1.3	V
Gate resistance	R _G	f=1MHz, Open drain	-	10	-	Ω
Maximum Body-Diode Continuous Current	I _S		-	-	-80	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-25V, V _{GS} =0V, f=1MHz	-	5500	-	pF
Output Capacitance	C _{oss}		-	1555	-	
Reverse Transfer Capacitance	C _{rss}		-	220	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-30V, I _D =-20A	-	80.7	-	nC
Gate-Source Charge	Q _{gs}		-	19	-	
Gate-Drain Charge	Q _{gd}		-	18.3	-	
Reverse Recovery Charge	Q _{rr}	I _F =-20A, di/dt=100A/us	-	84	-	nC
Reverse Recovery Time	t _{rr}		-	57.5	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V, V _{DD} =-30V, R _{GEN} =1.6Ω, I _D =-20A	-	13.2	-	ns
Turn-on Rise Time	t _r		-	27.7	-	
Turn-off Delay Time	t _{D(off)}		-	137.8	-	
Turn-off fall Time	t _f		-	59.5	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T_J=25°C, V_{DD}=-40V, V_{GS}=-10V, L=2mH, I_{AS}=-20A.

C. P_d is based on max. junction temperature, using junction-case and junction-ambient thermal resistance.

D. The value of R^θ JA is measured with the device mounted on the 40mm*40mm*1.1mm FR-4 PCB board with 1 in2 pad of 2oz. Copper, in the still air environment with TA =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



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Typical Electrical and Thermal Characteristics Diagrams

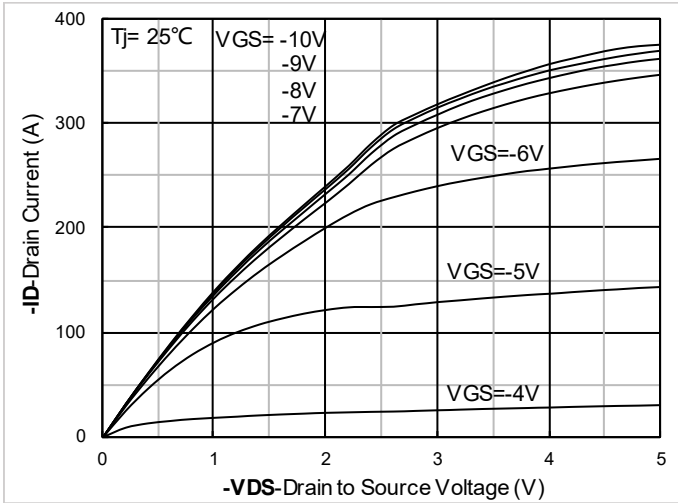


Figure 1. Output Characteristics

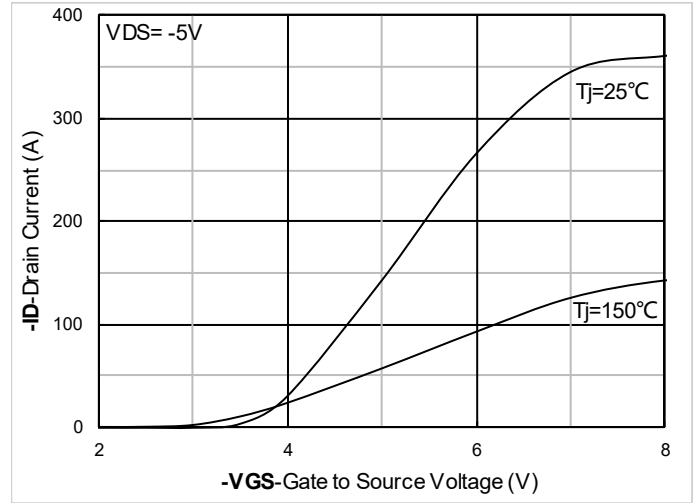


Figure 2. Transfer Characteristics

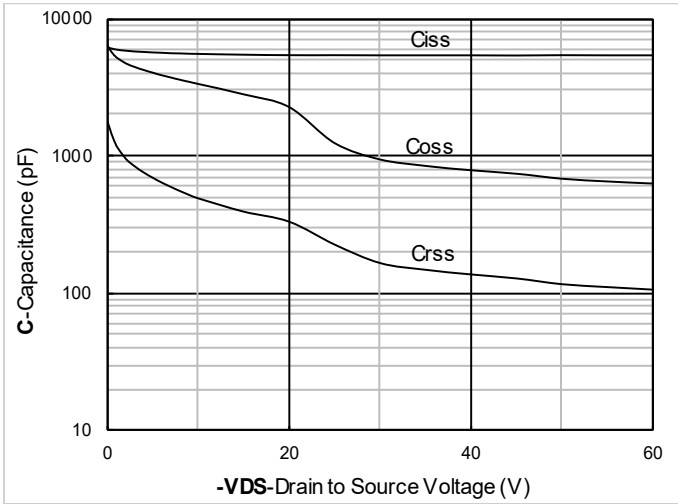


Figure 3. Capacitance Characteristics

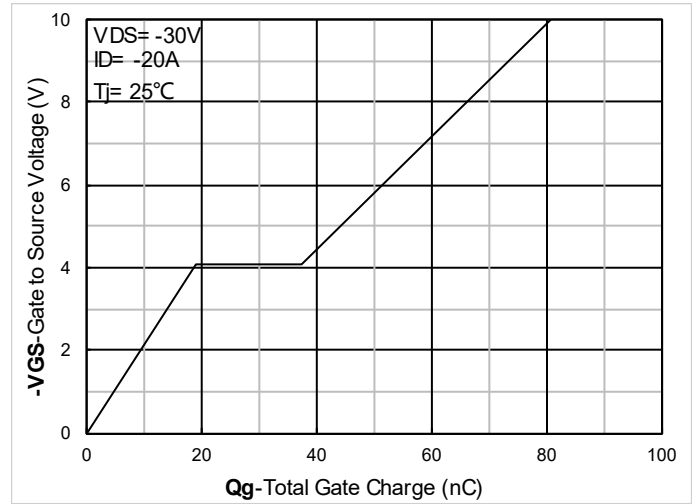


Figure 4. Gate Charge

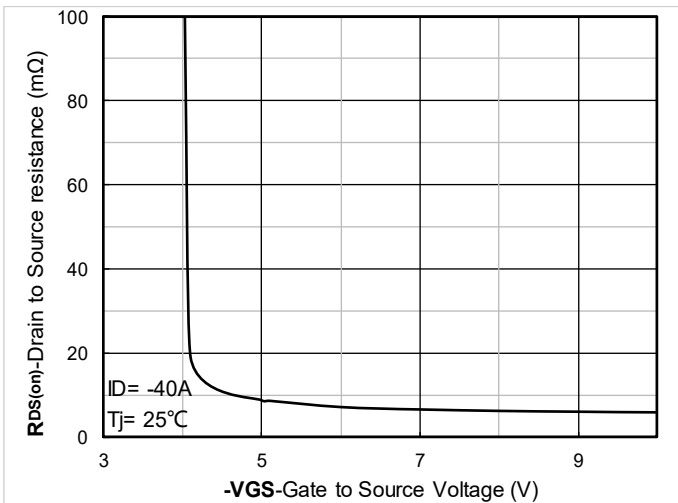


Figure 5. On-Resistance vs Gate to Source Voltage

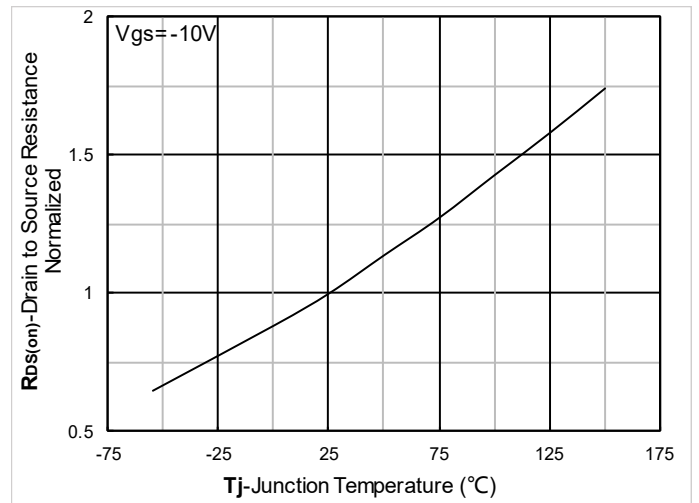


Figure 6. Normalized On-Resistance



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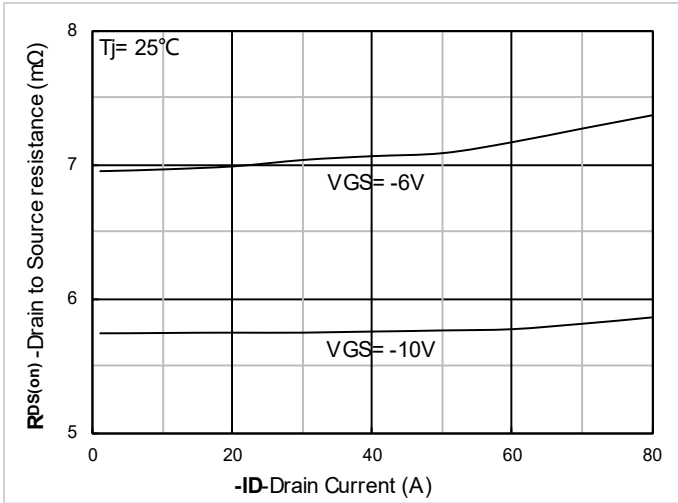


Figure 7. $R_{DS(on)}$ VS Drain Current

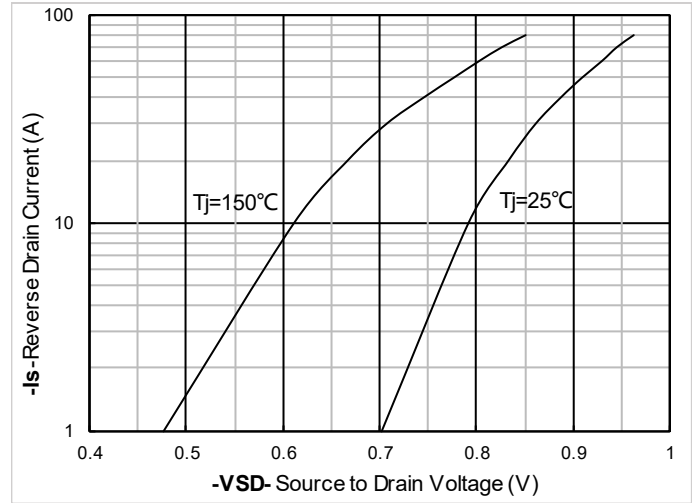


Figure 8. Forward characteristics of reverse diode

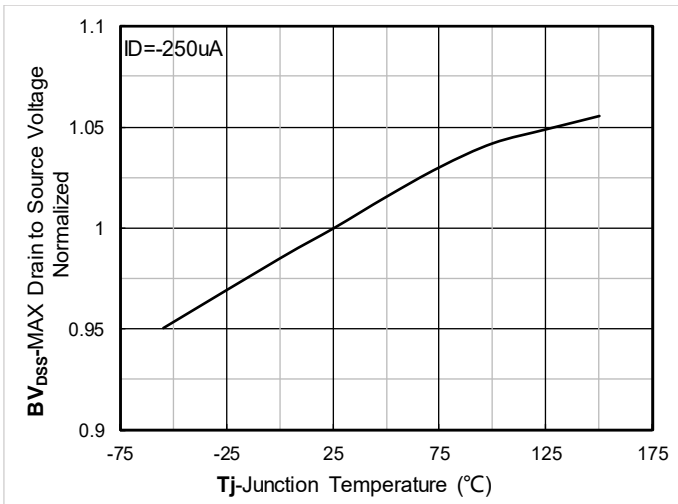


Figure 9. Normalized breakdown voltage

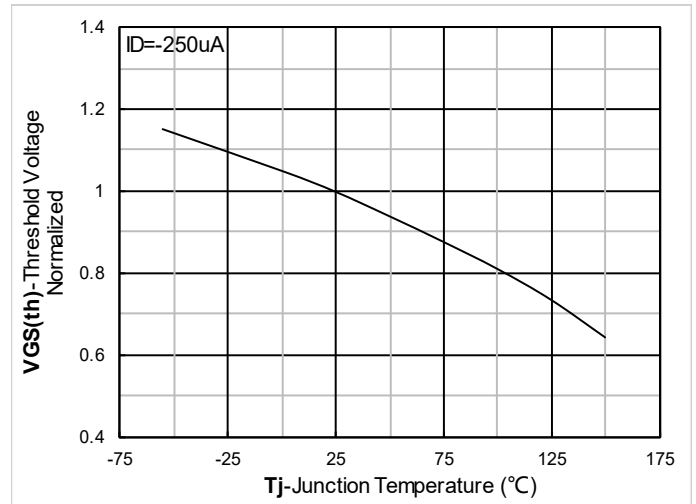


Figure 10. Normalized Threshold voltage

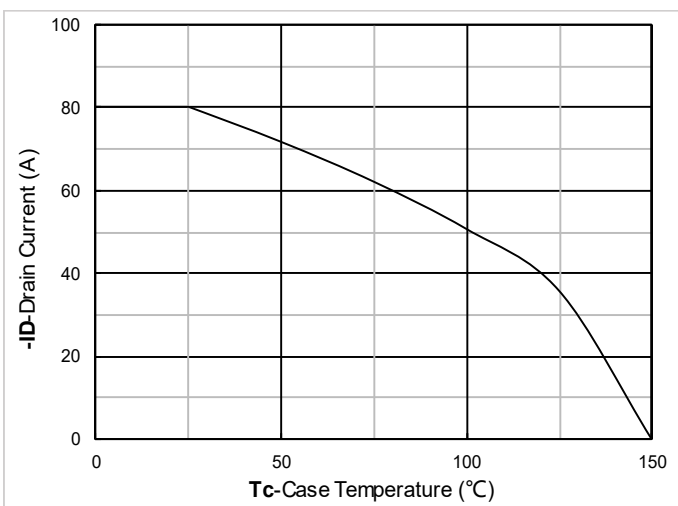


Figure 11. Current dissipation

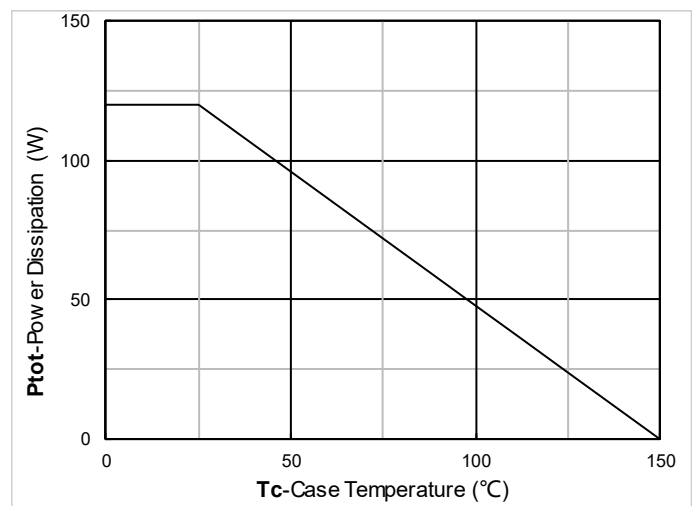


Figure 12. Power dissipation



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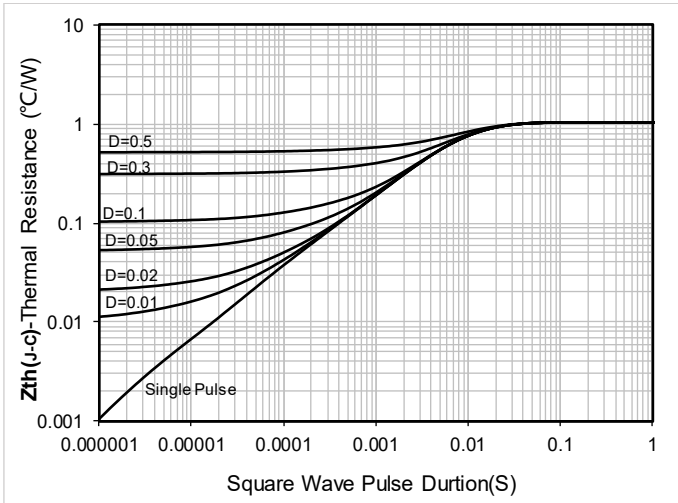


Figure 13. Maximum Transient Thermal Impedance

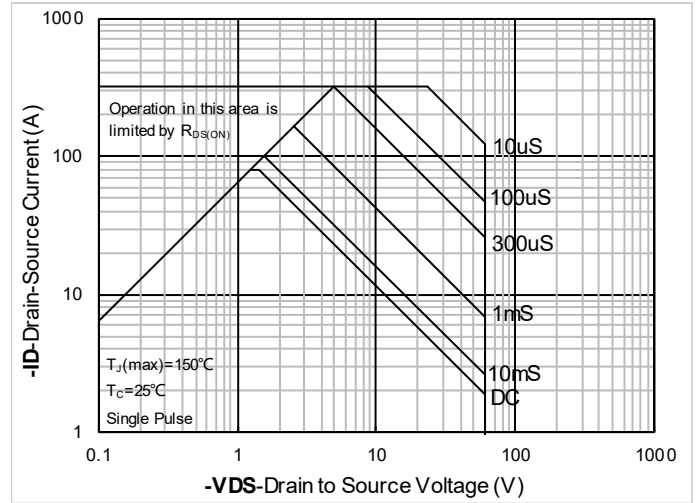
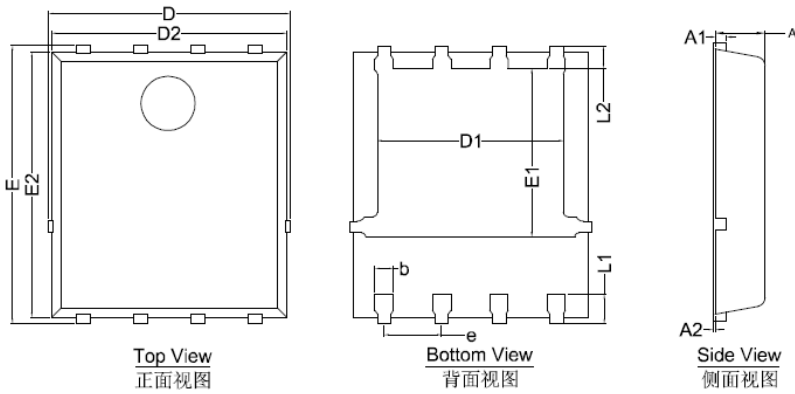


Figure 14. Safe Operation Area

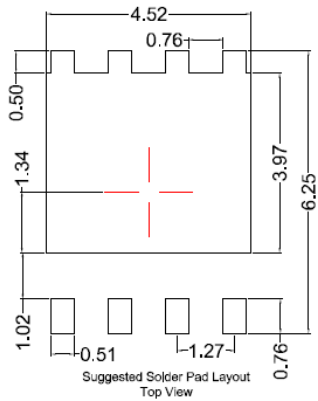


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■ Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		



Note:
 1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.10\text{mm}$.
 3. The pad layout is for reference purposes only.



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