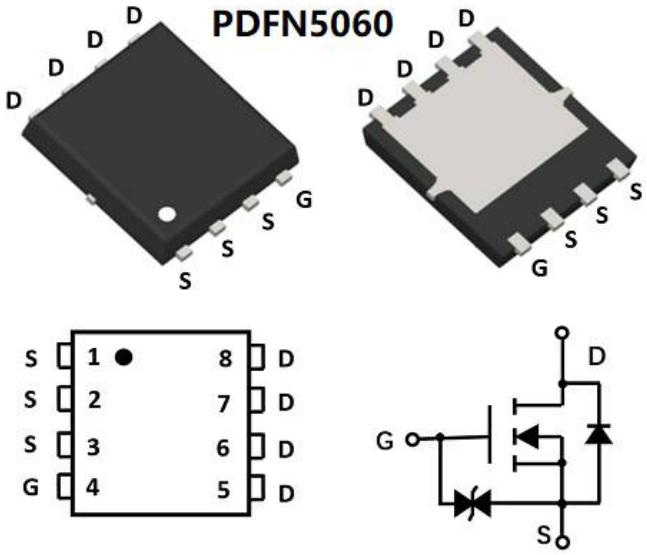
N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 60V
- I_D 85A
- $R_{DS(ON)}$(at V_{GS}=10V) ＜3.7 mohm
- $R_{DS(ON)}$(at V_{GS}=4.5V) ＜5.0 mohm
- 100% UIS Tested
- 100% ▽V_{DS} Tested
- ESD Protected up to 2.0KV(HBM)

General Description

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- DC-DC Converters
- Power management functions
- Synchronous-rectification application

■ Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	±20	V
Drain Current [A]	T_C=25℃	I_D	85	A
	T_C=100℃		54	
Pulsed Drain Current [B]		I_{DM}	340	A
Avalanche energy		E_{AS}	400	mJ
Total Power Dissipation [C]	Tc=25℃	P_D	110	W
	Tc=100℃		44	
Junction and Storage Temperature Range		T_J ,T_{STG}	-55～+150	℃

■Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient [D]	t≤10S	$R_{\theta JA}$	14	17	℃/W
Thermal Resistance Junction-to-Ambient [D]	Steady-State		40	55	
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	0.85	1.1	

■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJG85G06AK	F1	YJG85G06AK	5000	10000	100000	13“ reel

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V			±10	μA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.0	1.6	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= 10V, I_D=20A		2.9	3.7	mΩ
		V_{GS}= 4.5V, I_D=20A		3.8	5.0	
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V		0.8	1.3	V
Maximum Body-Diode Continuous Current	I_S				85	A
Gate resistance	R_g	f=1MHz，open drain		2		Ω
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=30V,V_{GS}=0V,f=1MHZ		4650		pF
Output Capacitance	C_{oss}			850		
Reverse Transfer Capacitance	C_{rss}			65		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=30V,I_D=25A		70.78		nC
Gate-Source Charge	Q_{gs}			16.64		
Gate-Drain Charge	Q_{gd}			10.62		
Reverse Recovery Chrage	Q_{rr}	I_F=20A, di/dt=500A/us		39.8		
Reverse Recovery Time	t_{rr}			41.6		ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V,V_{DD}=30V,ID=25A R_{GEN}=2Ω		15.9		
Turn-on Rise Time	t_r			55.2		
Turn-off Delay Time	$t_{D(off)}$			57.5		
Turn-off fall Time	t_f			91.3		

A. Repetitive rating; pulse width limited by max. junction temperature.
B. V_{DD}=50V, V_{GS}=10V, L=2mH, I_{AS}=20A.
C. Pd is based on max. junction temperature, using junction-case thermal resistance.
D. The value of RqJA is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C. The Power dissipation PDSM is based on R qJA t≤ 10s and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

■ Typical Performance Characteristics

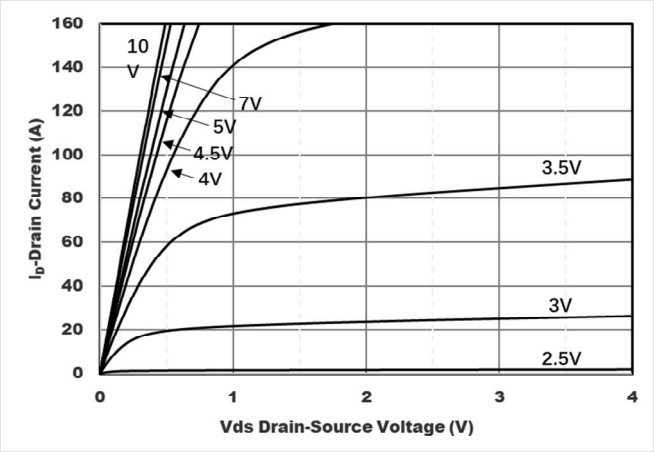


Figure1. Output Characteristics

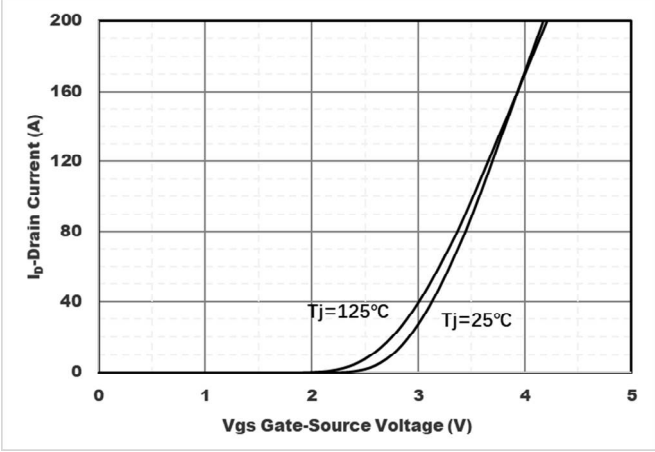


Figure2. Transfer Characteristics

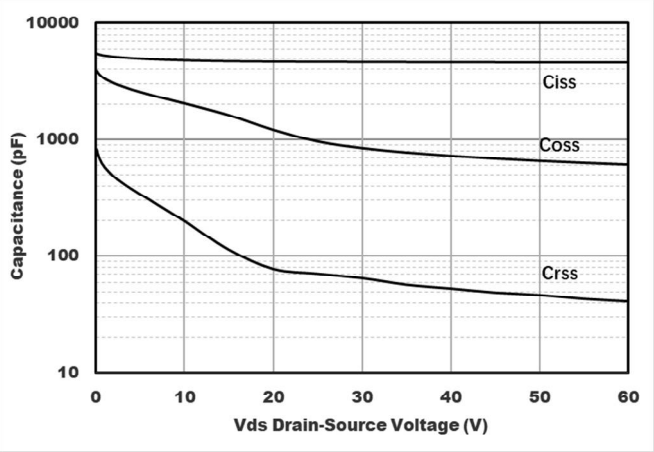


Figure3. Capacitance Characteristics

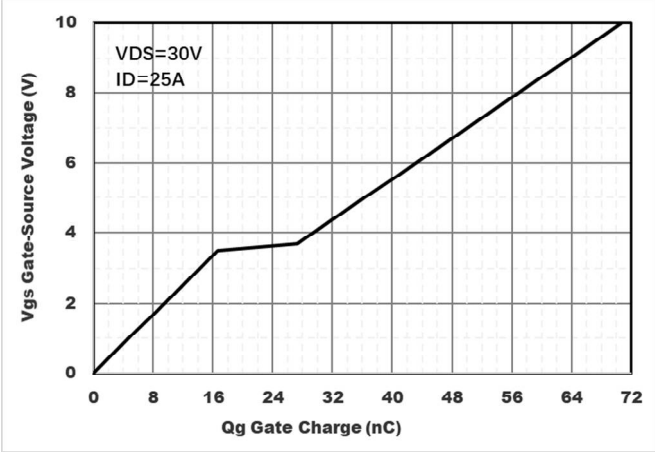


Figure4. Gate Charge

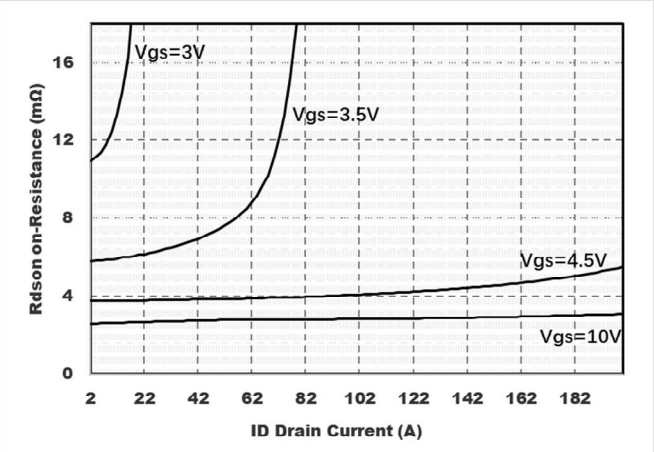


Figure5. Drain-Source on Resistance

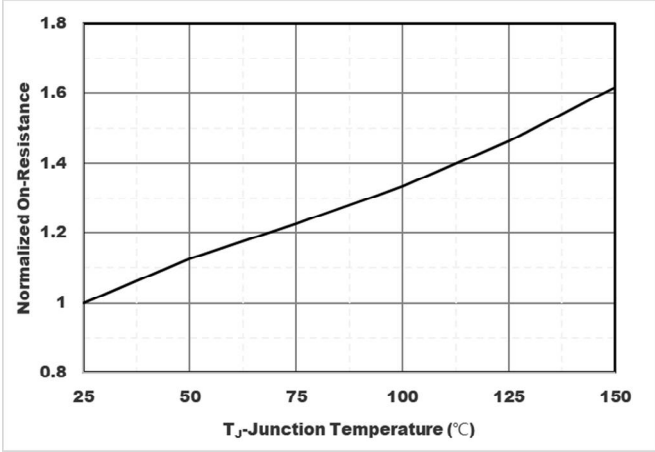


Figure6. Drain-Source on Resistance

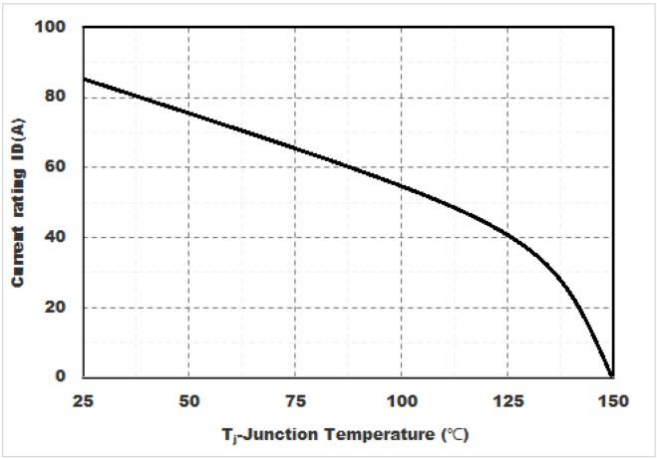


Figure7. Drain current

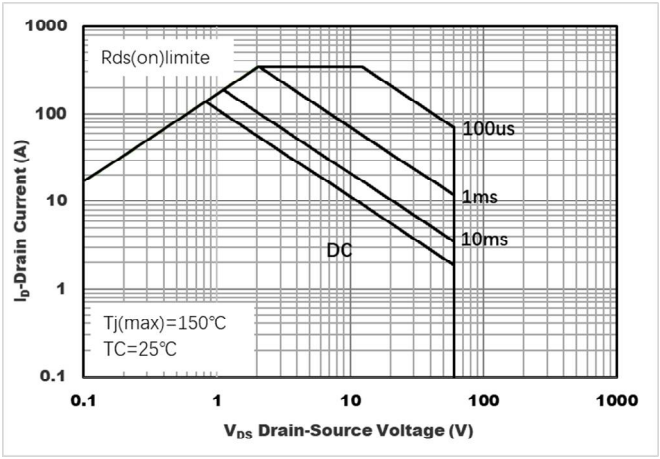


Figure8. Safe Operation Area

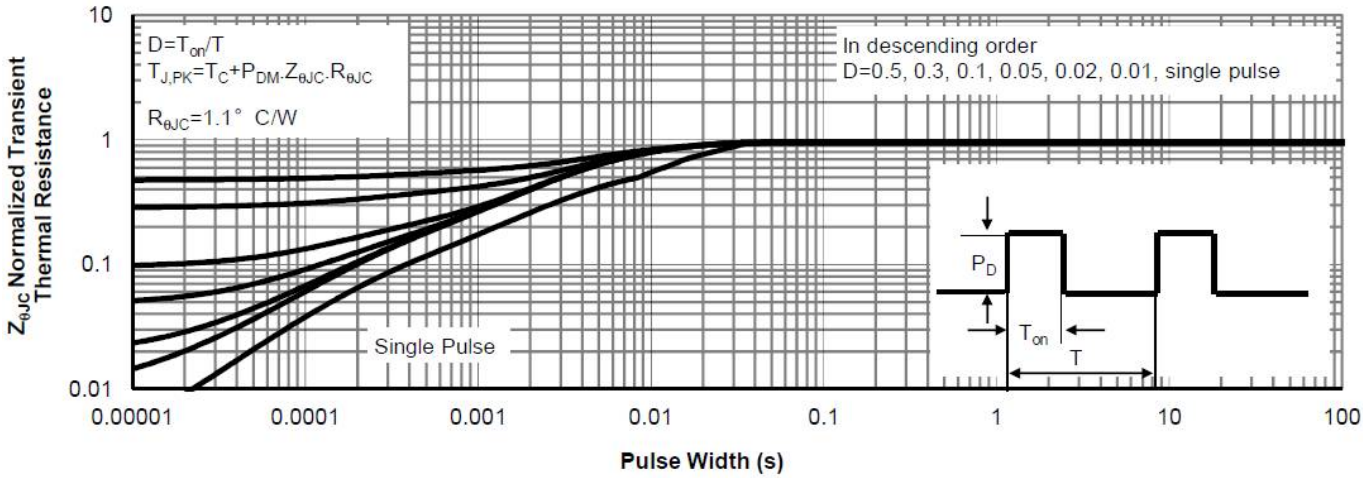
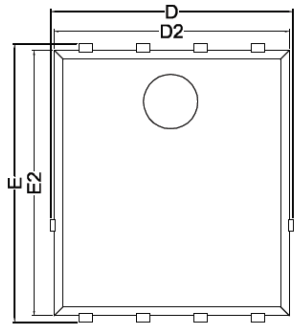
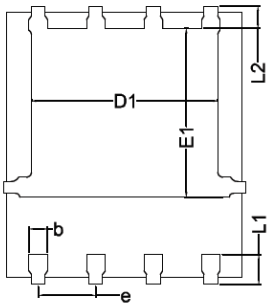


Figure9. Normalized Maximum Transient Thermal Impedance

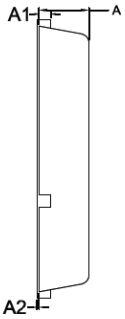
■ PDFN5060-8L Package information



Top View
正面视图



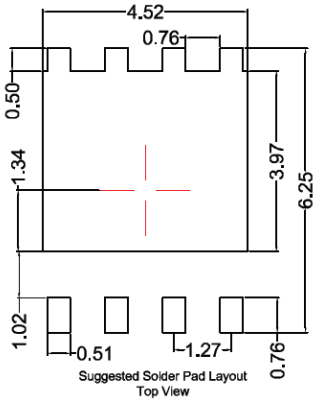
Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1		0.254 BSC	
A2			0.10
D1	3.92	4.12	4.32
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
L1	0.56	0.66	0.76
L2		0.50 BSC	
b	0.31	0.41	0.51
e		1.27 BSC	

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.



Suggested Solder Pad Layout
Top View

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