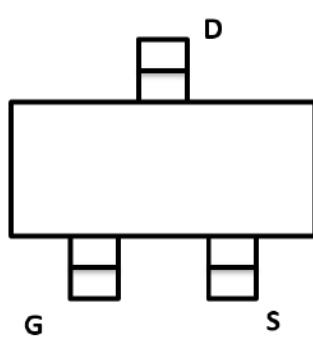
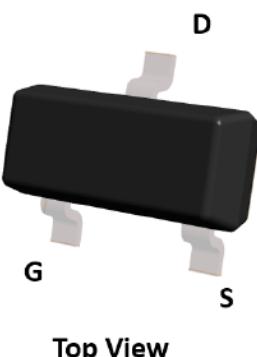
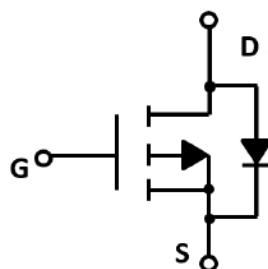


P-Channel Enhancement Mode Field Effect Transistor

**SOT-23**

Product Summary

- V_{DS} -30V
- I_D -4.1A
- $R_{DS(ON)}$ (at $V_{GS}=-10V$) <49mohm
- $R_{DS(ON)}$ (at $V_{GS}=-4.5V$) <65mohm

General Description

- Trench Power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- Battery protection
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-30	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ\text{C}$	I_D	-4.1	A
	$T_A=70^\circ\text{C}$		-3.2	
Pulsed Drain Current ^A		I_{DM}	-15	A
Total Power Dissipation	$T_A=25^\circ\text{C}$	P_D	1.2	W
	$T_A=70^\circ\text{C}$		0.8	W
Thermal Resistance Junction-to-Ambient ^B		$R_{\theta JA}$	105	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJL3407AQ	F2	3407.	3000	30000	120000	7" reel



YJL3407AQ

■ Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=-250\mu\text{A}$	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}}=-30\text{V}, V_{\text{GS}}=0\text{V}$			-1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 10\text{V}, V_{\text{DS}}=0\text{V}$			± 100	nA
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=-250\mu\text{A}$	-1	-1.5	-2.4	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=-10\text{V}, I_{\text{D}}=-4.1\text{A}$		36	49	$\text{m}\Omega$
		$V_{\text{GS}}=-4.5\text{V}, I_{\text{D}}=-3.5\text{A}$		52	65	
Diode Forward Voltage	V_{SD}	$I_{\text{S}}=-4.1\text{A}, V_{\text{GS}}=0\text{V}$			-1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{\text{DS}}=-15\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$		572		pF
Output Capacitance	C_{oss}			82		
Reverse Transfer Capacitance	C_{rss}			70		
Switching Parameters						
Total Gate Charge	Q_g	$V_{\text{GS}}=-10\text{V}, V_{\text{DS}}=-15\text{V}, I_{\text{D}}=-4.1\text{A}$		11.65		nC
Gate-Source Charge	Q_{gs}			2.32		
Gate-Drain Charge	Q_{gd}			2.08		
Reverse Recovery Charge	Q_{rr}	$I_F=-10\text{A}, dI/dt=100\text{A/us}$		0.643		ns
Reverse Recovery Time	t_{rr}			15.7		
Turn-on Delay Time	$t_{\text{D(on)}}$			3.8		
Turn-on Rise Time	t_r	$V_{\text{GS}}=-10\text{V}, V_{\text{DS}}=-15\text{V}, R_L=15\Omega, R_{\text{GEN}}=2.5\Omega$		17.6		ns
Turn-off Delay Time	$t_{\text{D(off)}}$			17.8		
Turn-off fall Time	t_f			21.8		

A. Pulse Test: Pulse Width $\leq 300\text{us}$, Duty cycle $\leq 2\%$.

B. $R_{\theta\text{JA}}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta\text{JC}}$ is guaranteed by design, while $R_{\theta\text{JA}}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² FR-4 board with 2oz copper.

■ Typical Performance Characteristics

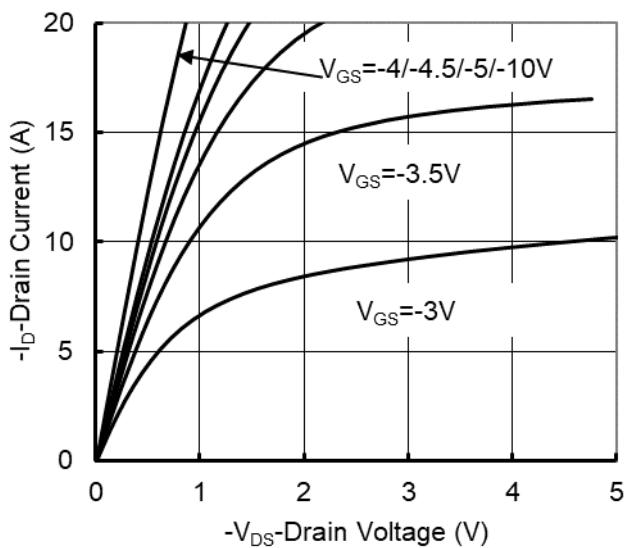


Figure 1. Output Characteristics

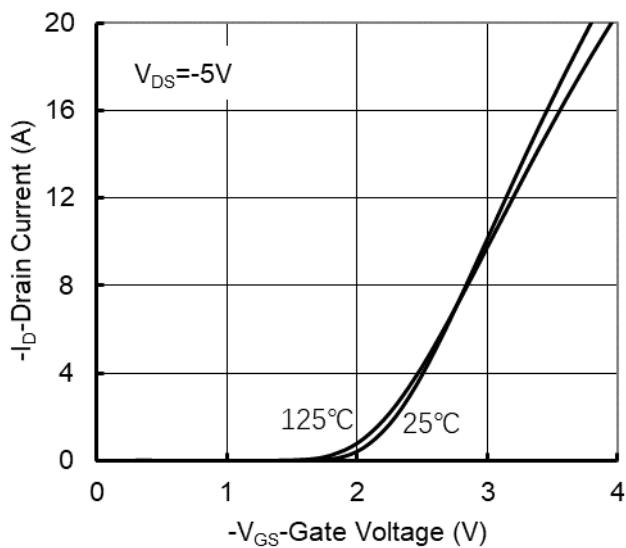


Figure 2. Transfer Characteristics

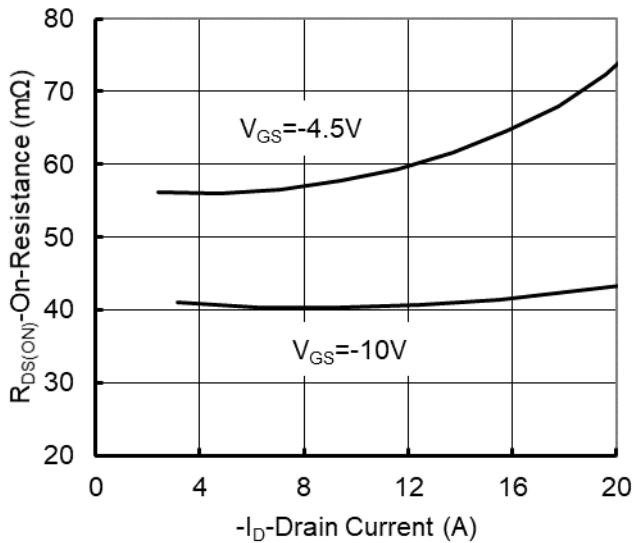


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

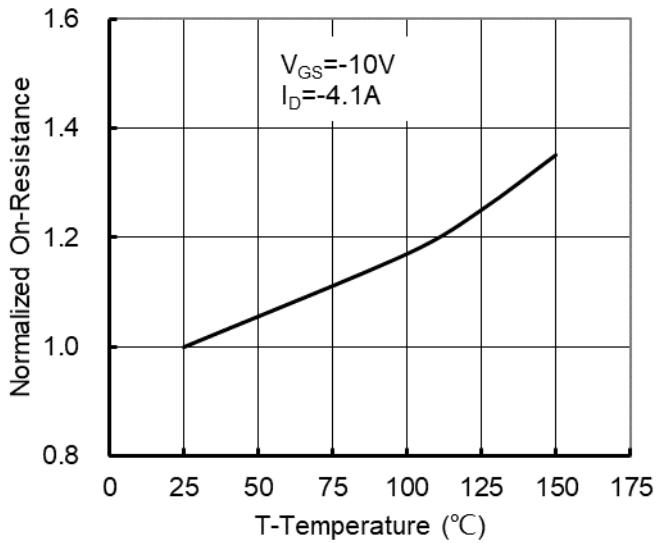


Figure 4: On-Resistance vs. Junction Temperature

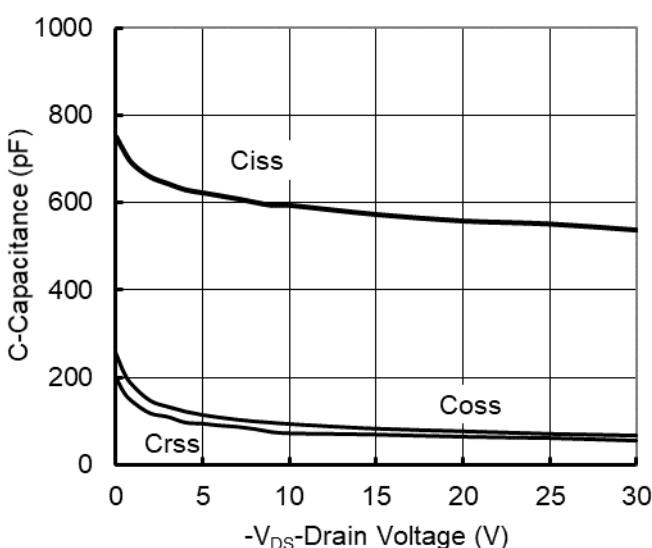


Figure 5. Capacitance Characteristics

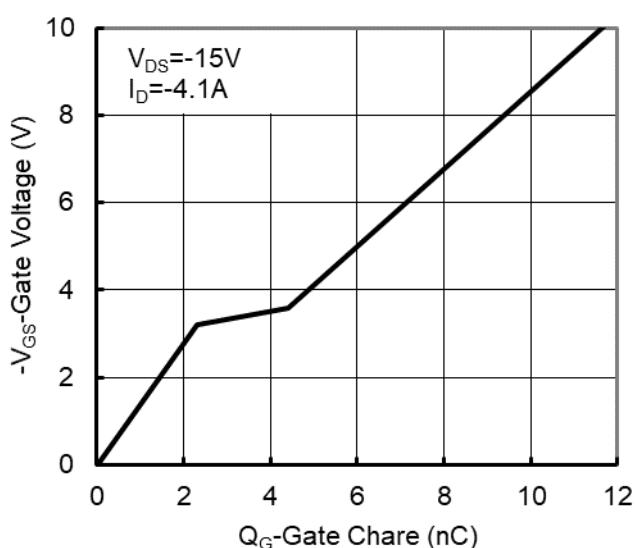
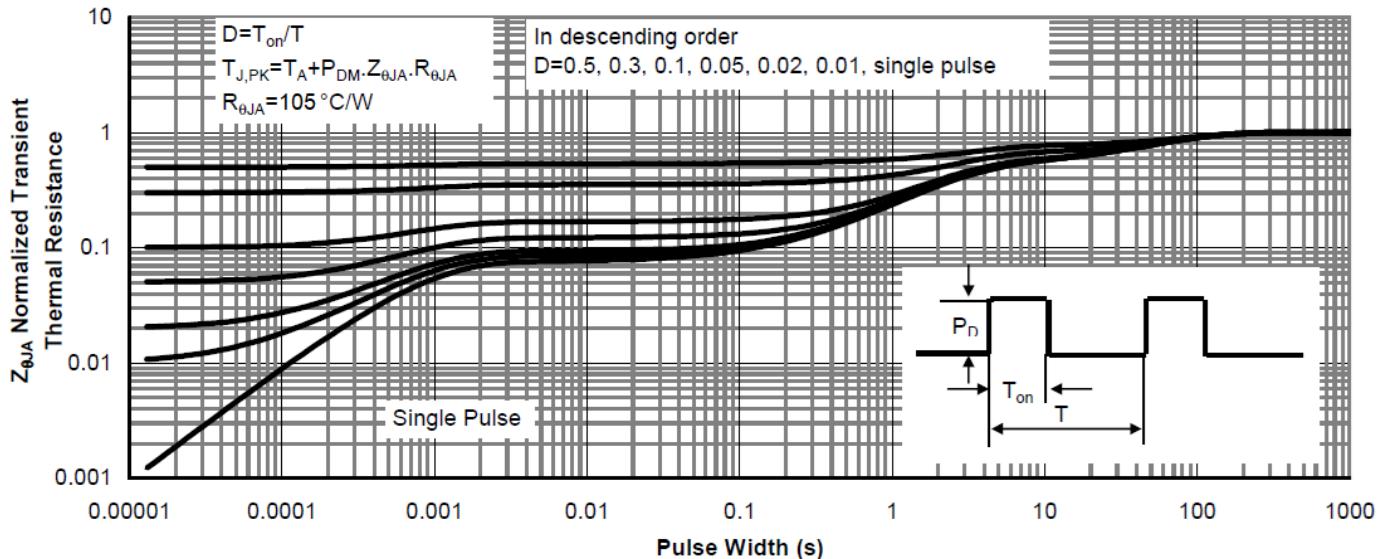
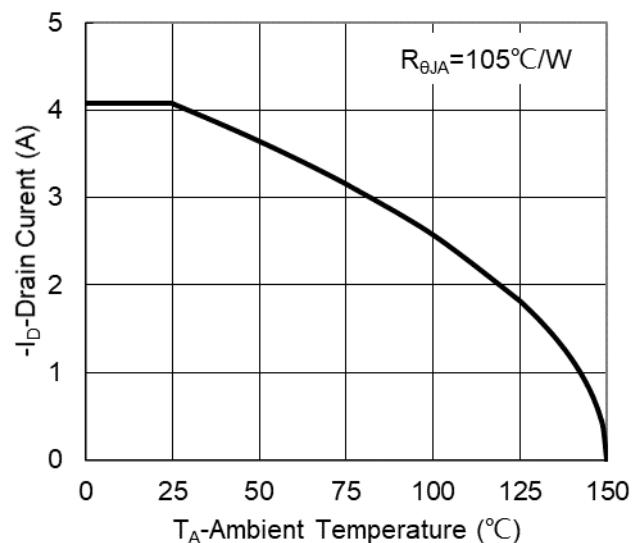
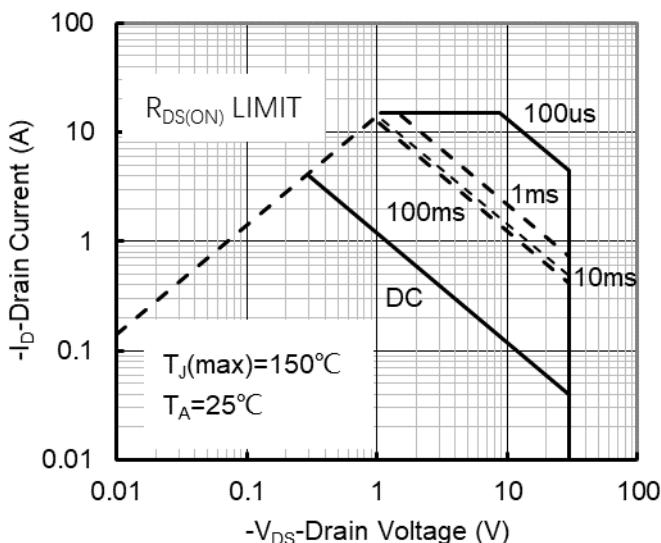
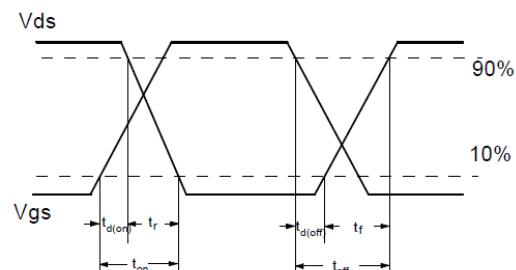
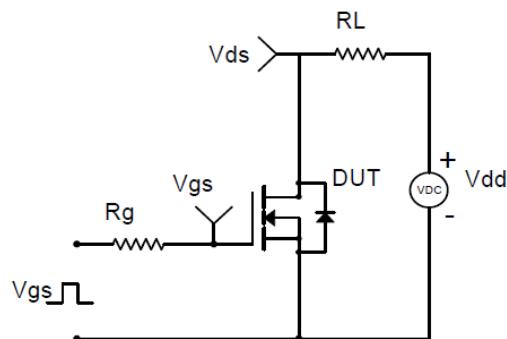
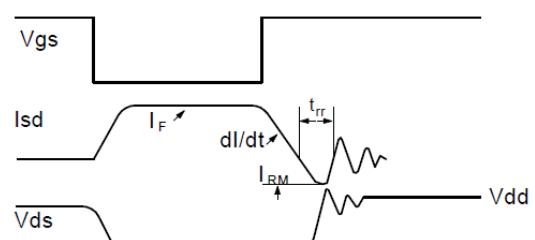
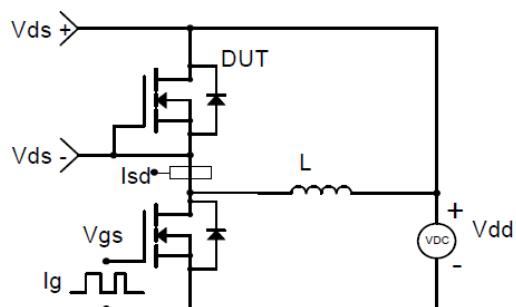
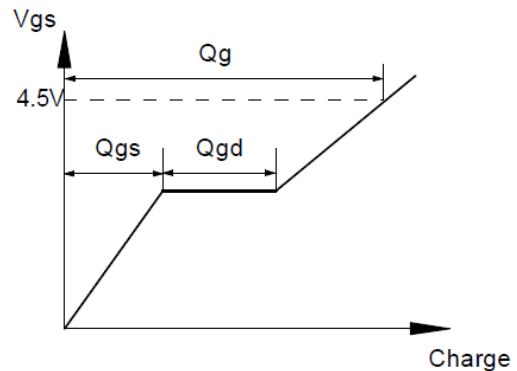
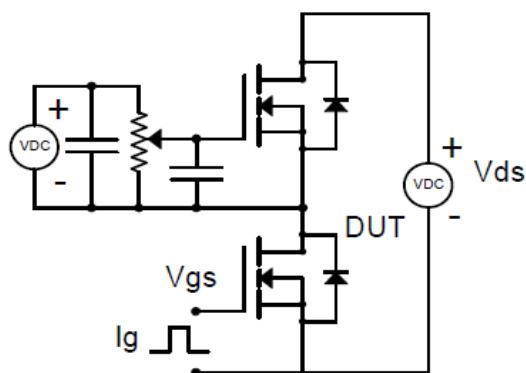
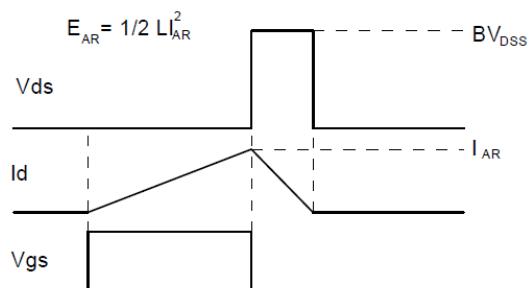
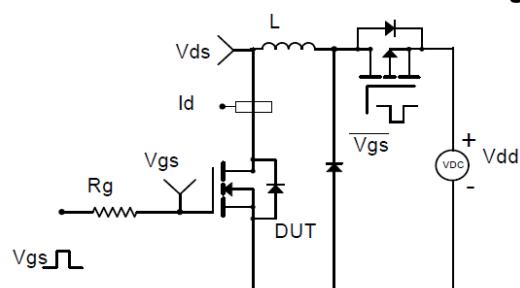
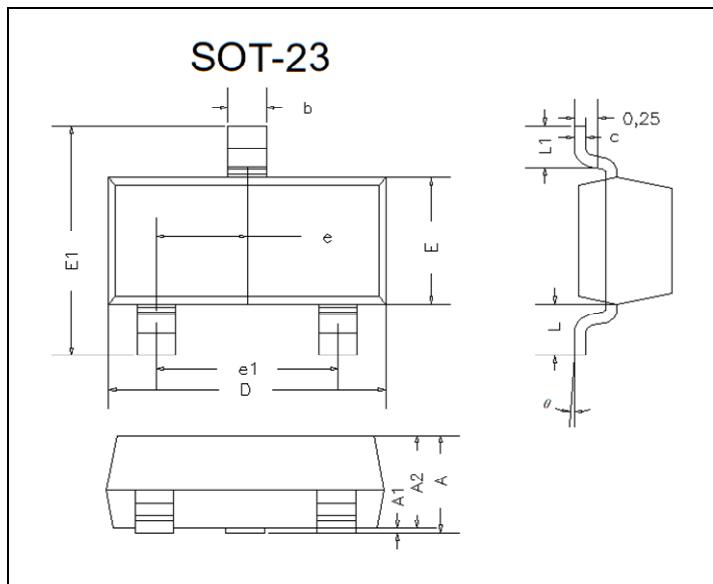


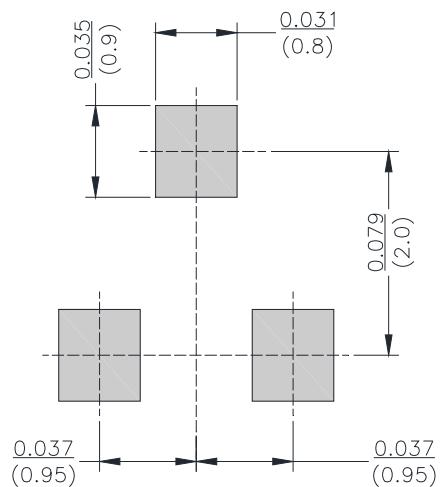
Figure 6. Gate Charge




Resistive Switching Test Circuit & Waveforms

Diode Recovery Test Circuit & Waveforms

Gate Charge Test Circuit & Waveform

Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

**■ SOT-23 Package information**

DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	0.035	0.045	0.90	1.15	
A1	0.000	0.004	0.00	0.10	
A2	0.035	0.041	0.90	1.05	
b	0.012	0.020	0.30	0.50	
c	0.004	0.008	0.10	0.20	
D	0.110	0.118	2.80	3.00	
E	0.047	0.055	1.20	1.40	
E1	0.089	0.100	2.25	2.55	
e	0.370TYP		0.95TYP		
e1	0.071	0.079	1.80	2.00	
L	0.220REF		0.55REF		
L1	0.012	0.020	0.30	0.50	
θ	0°	8°	0°	8°	

■ SOT-23 Suggested Pad Layout



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