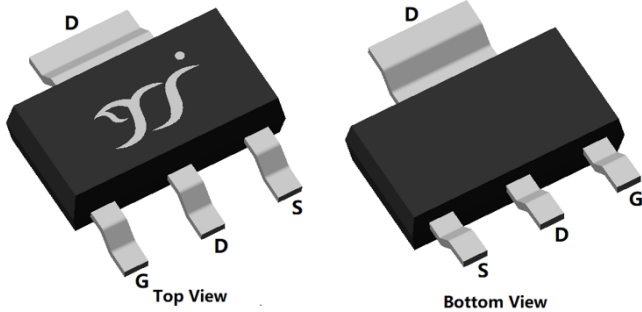
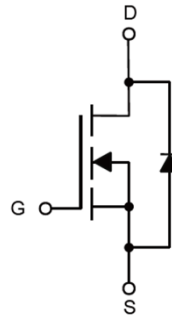


N-Channel Enhancement Mode Field Effect Transistor



SOT-223



Product Summary

- V_{DS} 60V
- I_D 5.0A
- $R_{DS(ON)}$ (at $V_{GS}= 10V$) <44mohm
- $R_{DS(ON)}$ (at $V_{GS}= 4.5V$) <49mohm

General Description

- Trench Power MV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Battery protection
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-source Voltage	V_{DS}	60	V
Gate-source Voltage	V_{GS}	± 20	V
Drain Current	I_D	$T_A=25^\circ\text{C}$ @ Steady State	5.0
		$T_A=70^\circ\text{C}$ @ Steady State	4.0
Pulsed Drain Current ^A	I_{DM}	25	A
Total Power Dissipation @ $T_A=25^\circ\text{C}$	P_D	2.5	W
Thermal Resistance Junction-to-Ambient @ Steady State ^B	$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJM05N06A	F2	6005	2500	/	40000	13" reel



YJM05N06A

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D =5.0A		35	44	mΩ
		V _{GS} = 4.5V, I _D =4.0A		39	49	
Diode Forward Voltage	V _{SD}	I _S =5.0A, V _{GS} =0V		0.8	1.2	V
Maximum Body-Diode Continuous Current	I _S				5.0	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V, f=1MHZ		1018		pF
Output Capacitance	C _{oss}			70		
Reverse Transfer Capacitance	C _{rss}			62		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =30V, I _D =10A		26		nC
Gate Source Charge	Q _{gs}			5.4		
Gate Drain Charge	Q _{gd}			6.5		
Reverse Recovery Charge	Q _{rr}	I _F =20A, di/dt=500A/us		11.7		ns
Reverse Recovery Time	t _{rr}			23		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =30V, I _D =2A, R _{GEN} =3Ω		10		ns
Turn-on Rise Time	t _r			20		
Turn-off Delay Time	t _{D(off)}			29		
Turn-off Fall Time	t _f			21		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R_{θJA} is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins. R_{θJL} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

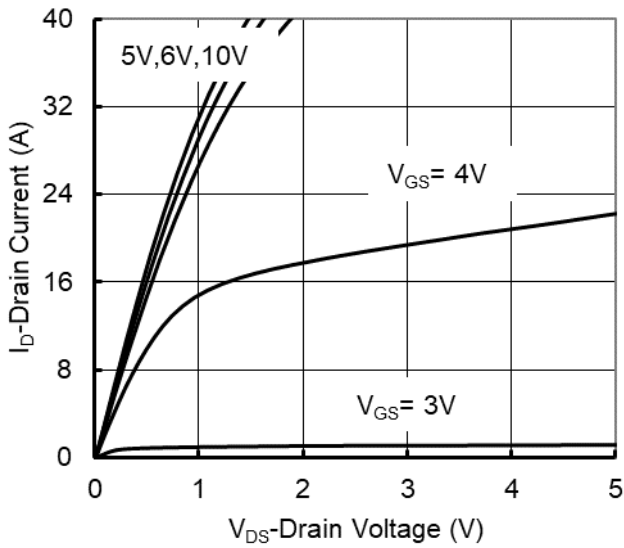


Figure 1. Output Characteristics

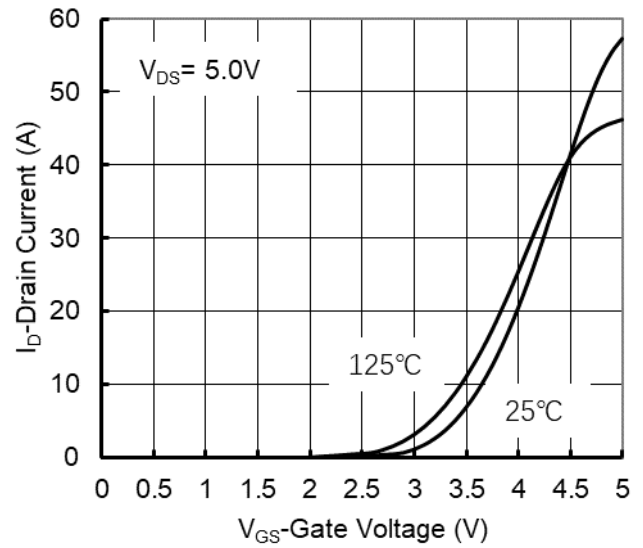


Figure 2. Transfer Characteristics

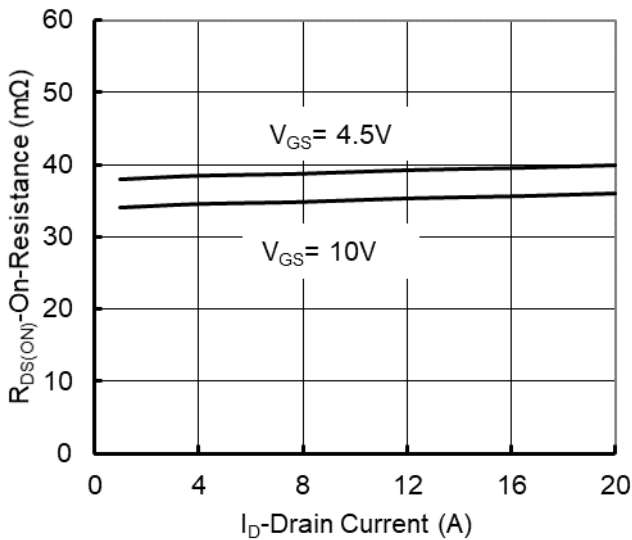


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

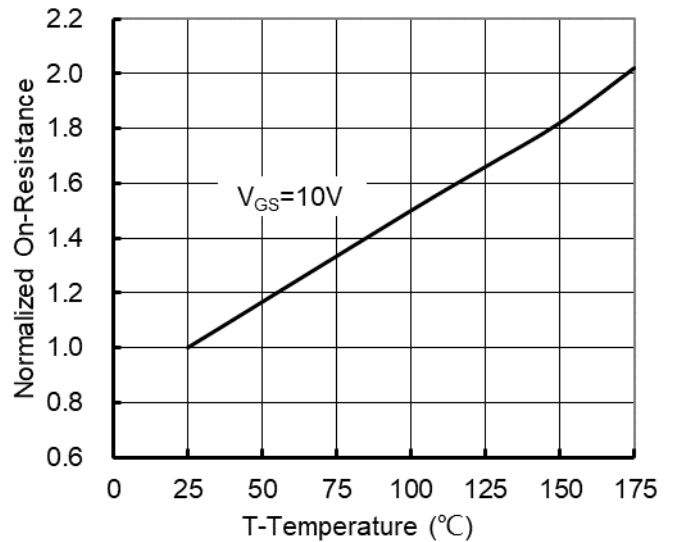


Figure 4. On-Resistance vs. Junction Temperature

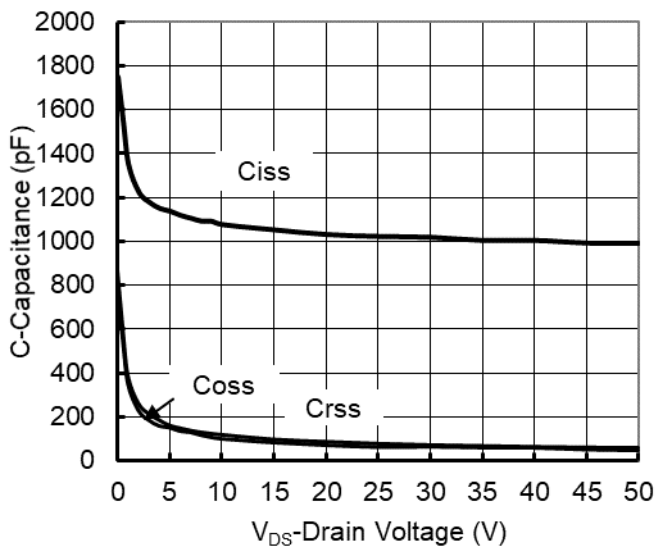


Figure 5. Capacitance Characteristics

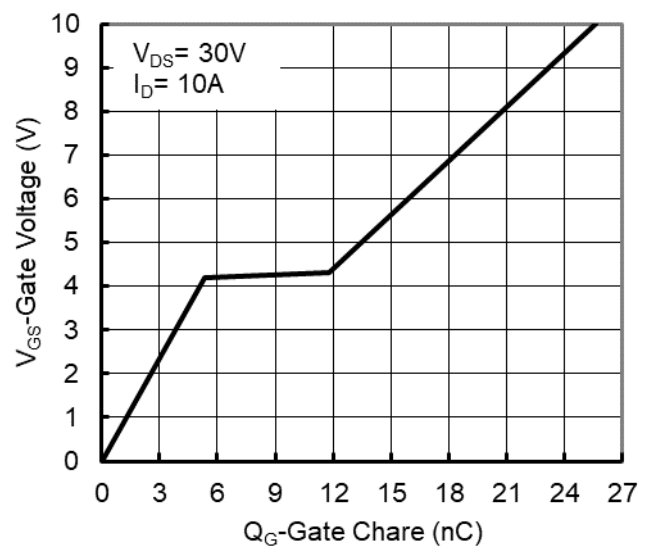


Figure 6. Gate Charge



YJM05N06A

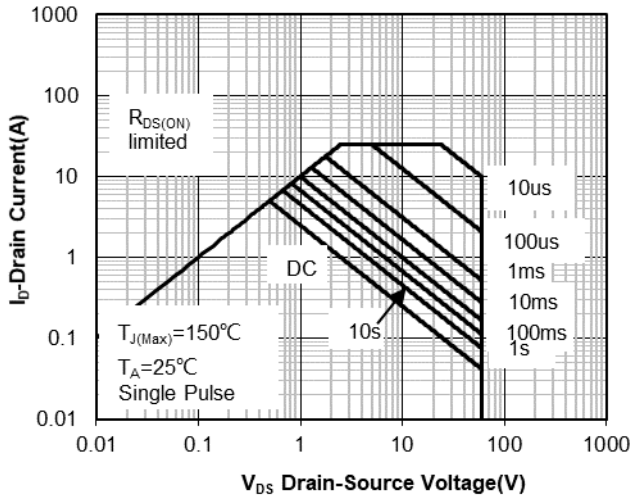


Figure 7. Safe Operation Area

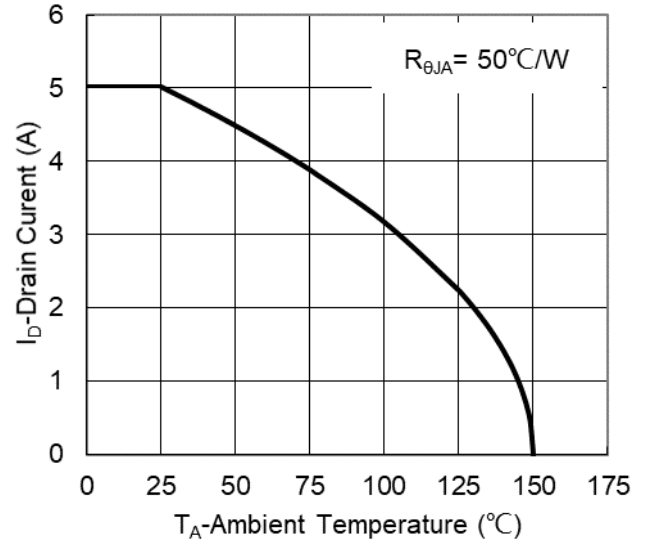


Figure 8. Maximum Continuous Drain Current vs Ambient Temperature

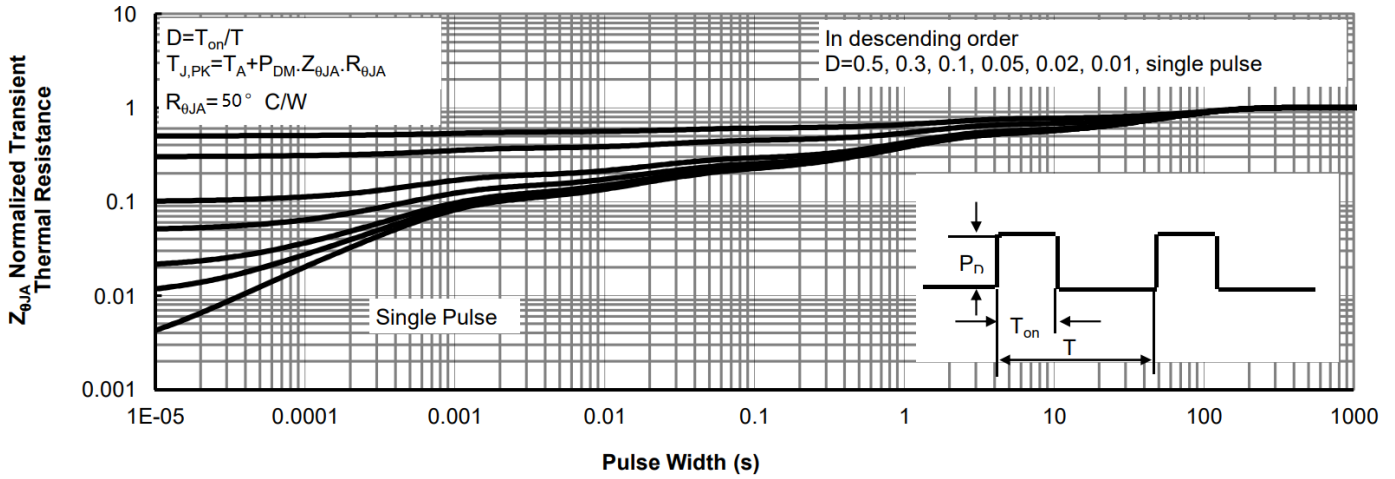
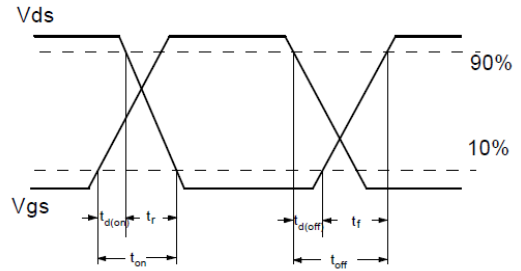
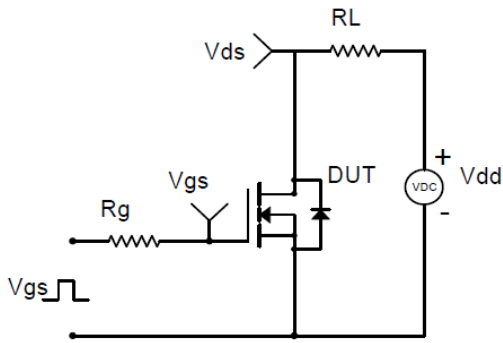
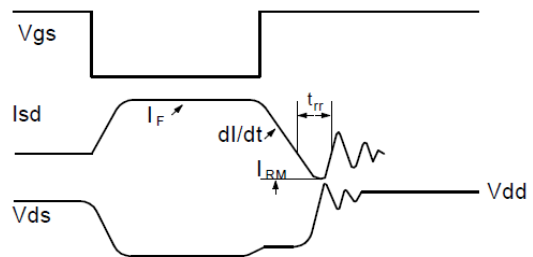
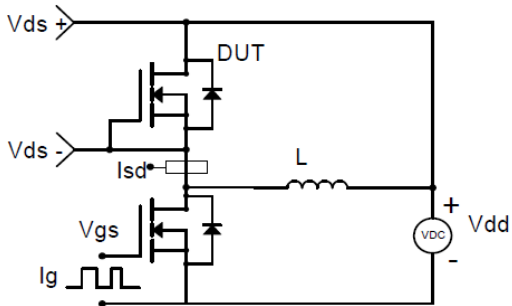


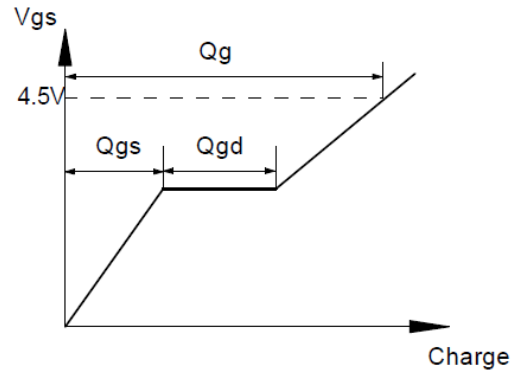
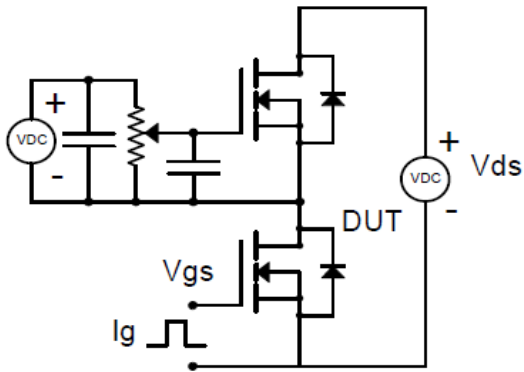
Figure 9. Normalized Maximum Transient Thermal Impedance



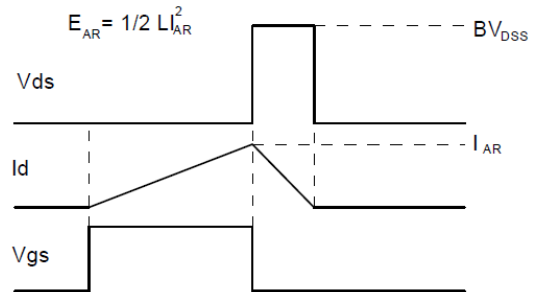
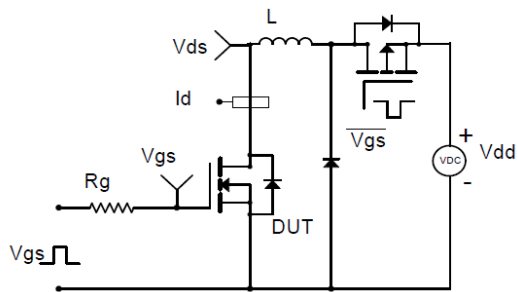
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

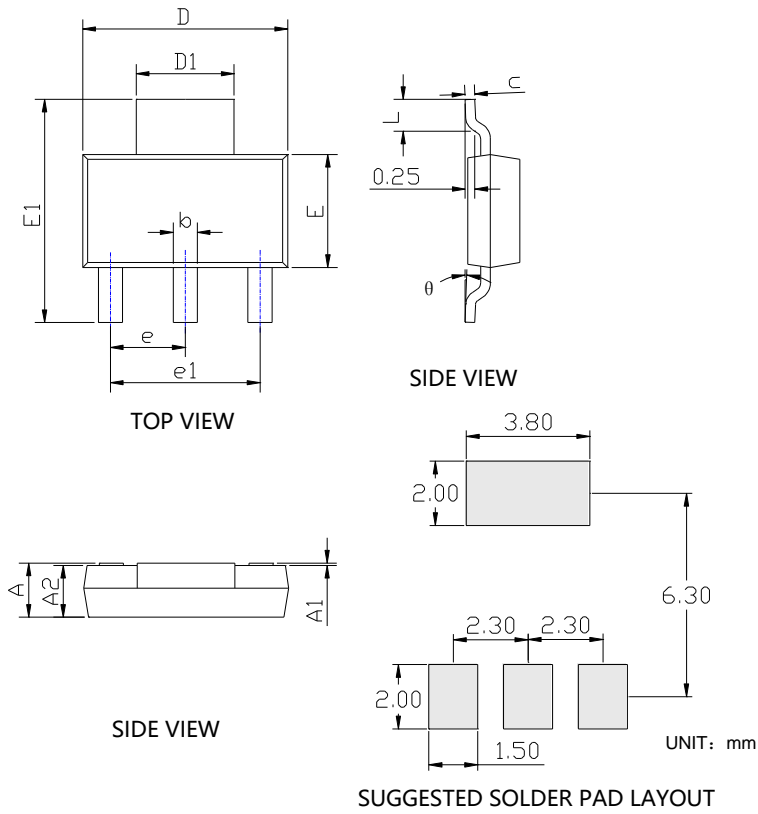


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



YJM05N06A

■SOT-223-B Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.060	0.071	1.520	1.800
A1	0.000	0.004	0.000	0.100
A2	0.059	0.067	1.500	1.700
b	0.026	0.032	0.660	0.820
c	0.010	0.014	0.250	0.350
D	0.244	0.252	6.200	6.400
D1	0.114	0.122	2.900	3.100
E	0.130	0.146	3.300	3.700
E1	0.269	0.278	6.830	7.070
e	0.091BSC		2.300BSC	
e1	0.177	0.185	4.500	4.700
L	0.035	0.045	0.900	1.150
θ	0°	10°	0°	10°

NOTE:
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



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[MCQ7328-TP](#) [SSM3J143TU,LXHF](#) [DMN12M3UCA6-7](#) [PJMF280N65E1_T0_00201](#) [PJMF380N65E1_T0_00201](#)
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