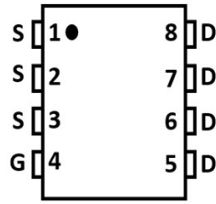
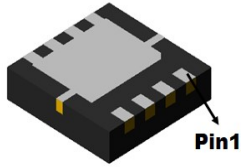
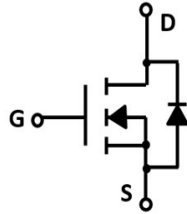


## N-Channel Enhancement Mode Field Effect Transistor



**DFN3.3X3.3**



### Product Summary

- $V_{DS}$  40 V
- $I_D$  20 A
- $R_{DS(ON)}$  (at  $V_{GS}=10V$ ) < 14.0 mohm
- $R_{DS(ON)}$  (at  $V_{GS}=4.5V$ ) < 18.5 mohm
- 100% UIS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$

### Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	40	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_C=25^\circ\text{C}$	$I_D$	20	A
	$T_C=100^\circ\text{C}$		14	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	90	A
Single Pulse Avalanche Energy <sup>B</sup>		$E_{AS}$	70	mJ
Total Power Dissipation	$T_C=25^\circ\text{C}$	$P_D$	21	W
	$T_A=25^\circ\text{C}$		2.34	
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	5.9	$^\circ\text{C}/\text{W}$
		$R_{\theta JA}$	53.4	
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### ■ Ordering Information (Example)

PREFERED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ20N04A	F1	Q20N04	5000	10000	100000	13" reel



# YJQ20N04A

## ■ Electrical Characteristics ( $T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	40			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=40V, V_{GS}=0V$			1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$			$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$		11	14	m $\Omega$
		$V_{GS}=4.5V, I_D=10A$		14.3	18.5	
Diode Forward Voltage	$V_{SD}$	$I_S=10A, V_{GS}=0V$		0.7	1.2	V
Maximum Body-Diode Continuous Current	$I_S$				20	A
<b>Dynamic Parameters</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=20V, V_{GS}=0V, f=1\text{MHz}$		917		pF
Output Capacitance	$C_{oss}$			128		
Reverse Transfer Capacitance	$C_{rss}$			108		
<b>Switching Parameters</b>						
Total Gate Charge	$Q_g$	$V_{GS}=10V, V_{DS}=20V, I_D=20A$		23.6		nC
Gate-Source Charge	$Q_{gs}$			4.4		
Gate-Drain Charge	$Q_{gd}$			6.3		
Reverse Recovery Charge	$Q_{rr}$	$I_F=20A, di/dt=100A/\mu s$		0.4		ns
Reverse Recovery Time	$t_{rr}$			7		
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=10V, V_{DD}=20V, I_D=2A, R_{GEN}=3\Omega$		10		ns
Turn-on Rise Time	$t_r$			56		
Turn-off Delay Time	$t_{D(off)}$			27		
Turn-off fall Time	$t_f$			72		

A. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$ .

B.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



## ■ Typical Performance Characteristics

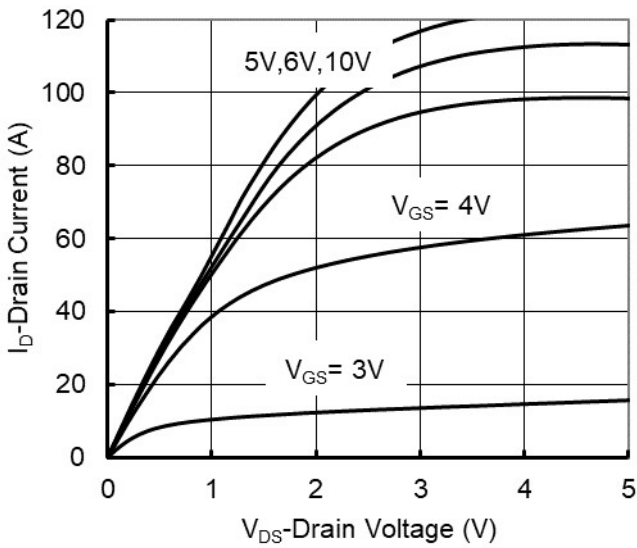


Figure 1. Output Characteristics

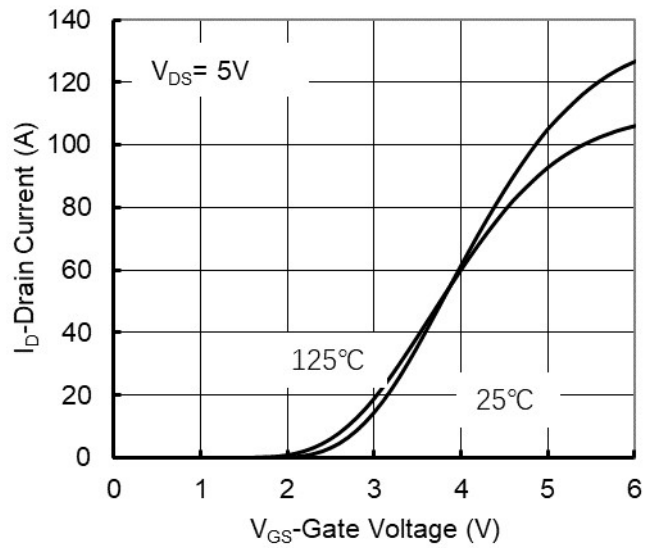


Figure 2. Transfer Characteristics

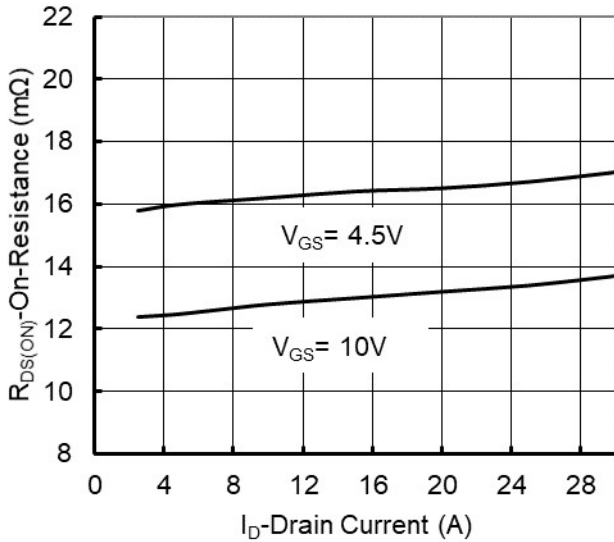


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

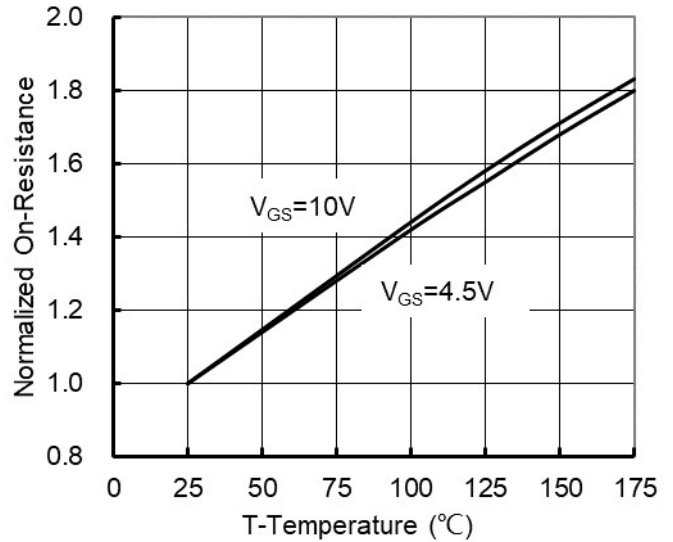


Figure 4. On-Resistance vs. Junction Temperature

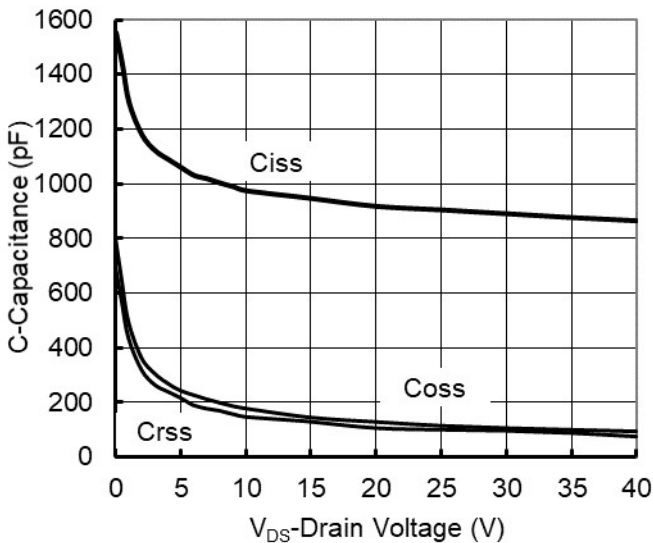


Figure 5. Capacitance Characteristics

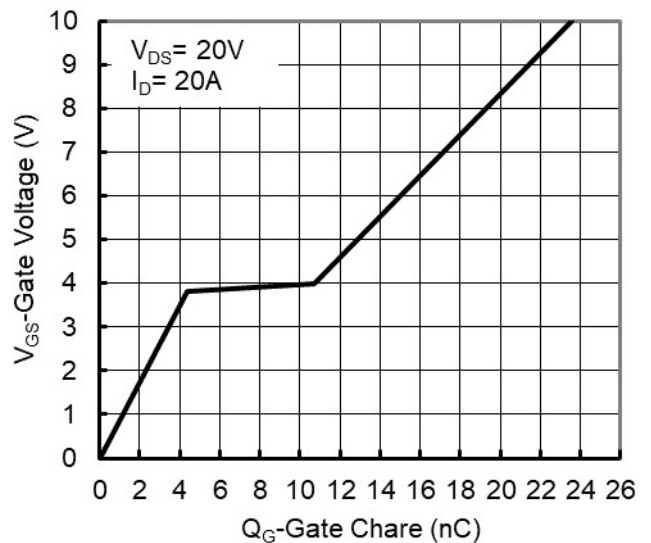


Figure 6. Gate Charge



# YJQ20N04A

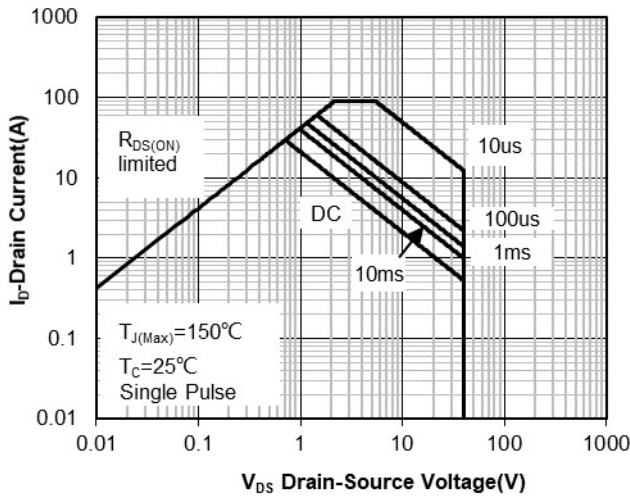


Figure 7. Safe Operation Area

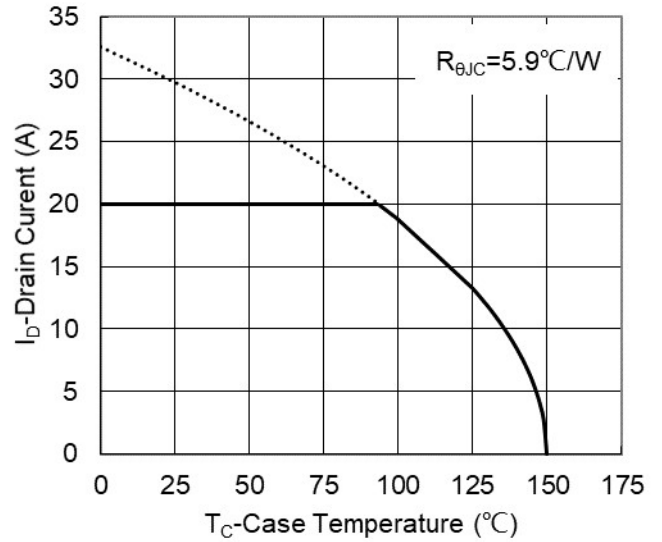


Figure 8. Maximum Continuous Drain Current vs Case Temperature

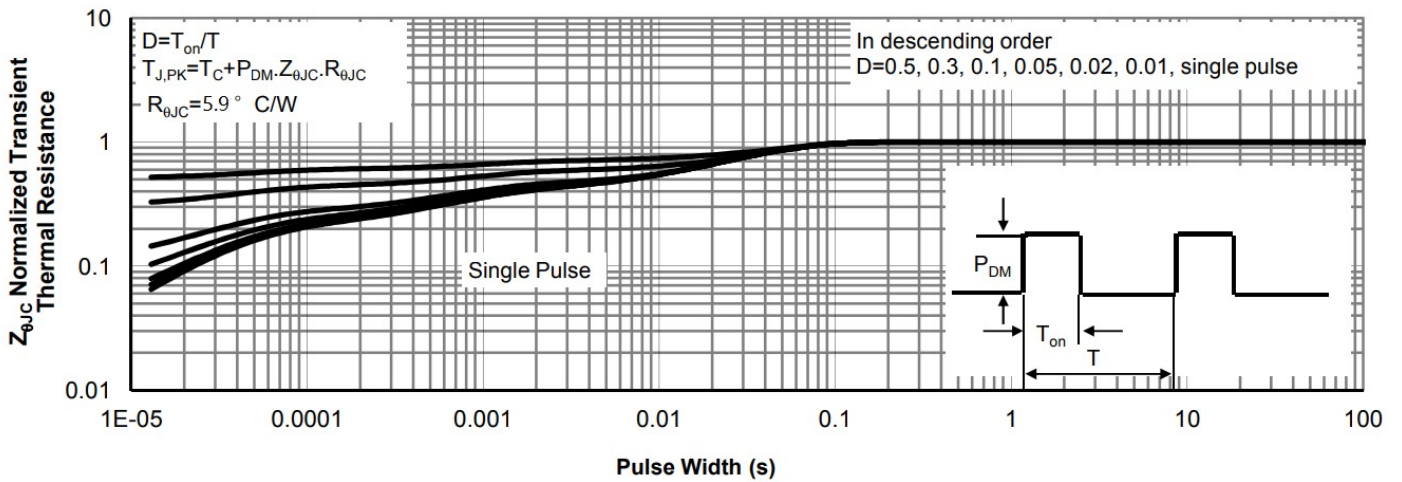
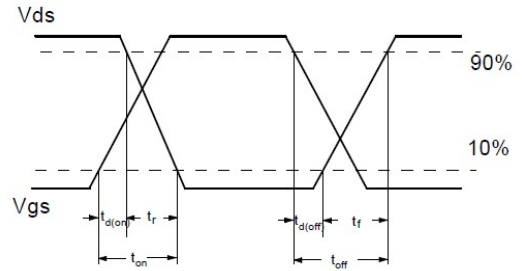
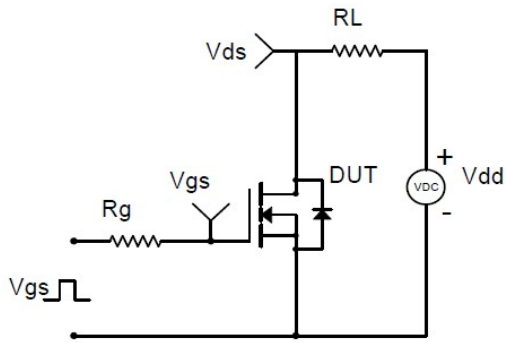
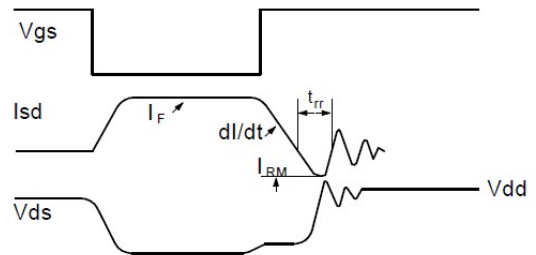
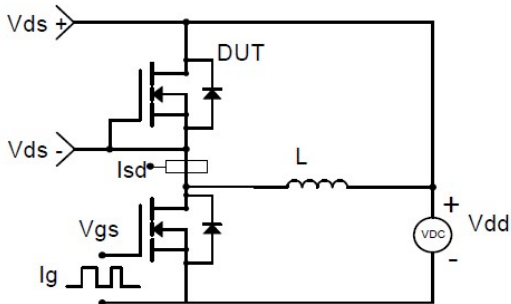


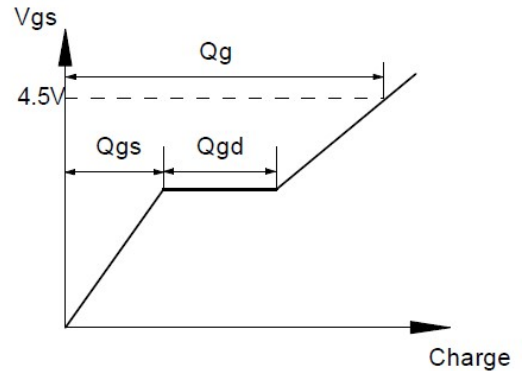
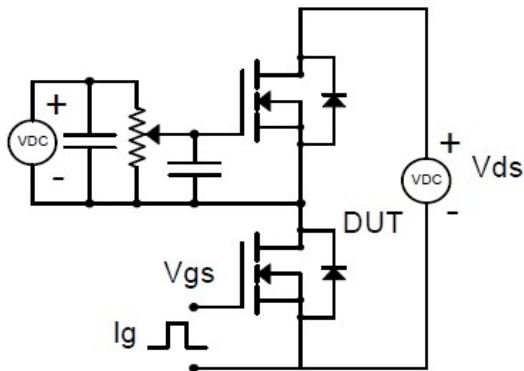
Figure 9. Normalized Maximum Transient Thermal Impedance



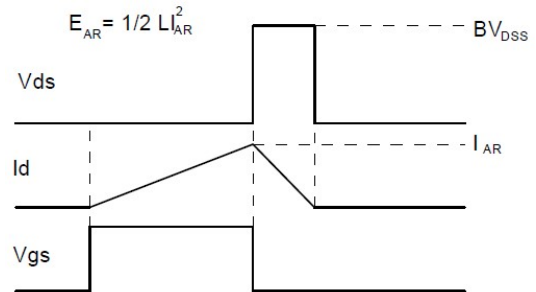
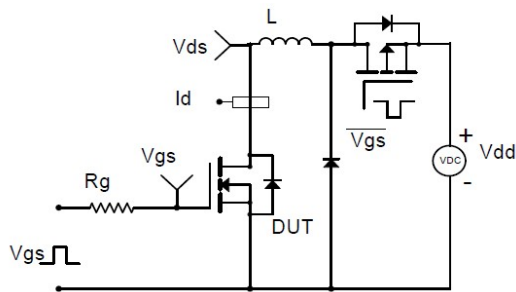
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

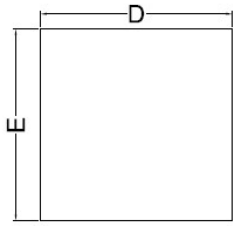


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**

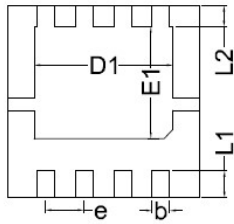


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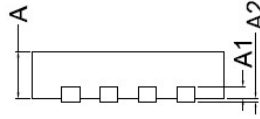
## DFN3.3X3.3 Package information



Top View  
正面视图

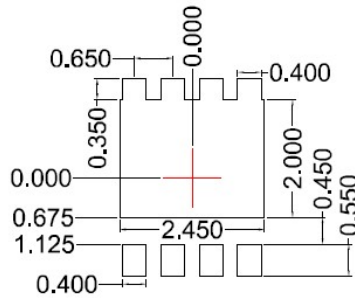


Bottom View  
背面视图



Side View  
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout  
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10\text{mm}$ .
3. The pad layout is for reference purposes only.



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