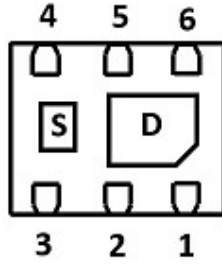
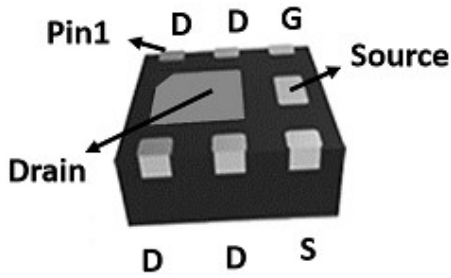
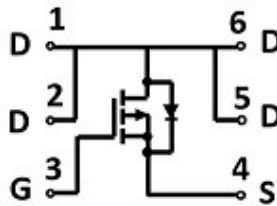


P-Channel Enhancement Mode Field Effect Transistor



DFN2x2-6L



Product Summary

- V_{DS} -30V
- I_D -5.5A
- $R_{DS(ON)}$ (at $V_{GS}=-10V$) <47mohm
- $R_{DS(ON)}$ (at $V_{GS}=-4.5V$) <64mohm
- 100% ∇V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching

Applications

- Battery protection
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-30	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ C$	I_D	-5.5	A
	$T_A=70^\circ C$		-4.4	
Pulsed Drain Current ^A		I_{DM}	-22	A
Total Power Dissipation	$T_A=25^\circ C$	P_D	2.2	W
	$T_A=70^\circ C$		1.4	
Thermal Resistance Junction-to-Ambient ^B		$R_{\theta JA}$	56.8	$^\circ C/W$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ C$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ3407A	F1	Q3407A	3000	30000	120000	7" reel



YJQ3407A

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-30V, V _{GS} =0V			-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-1	-1.5	-2.4	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-4.1A		34	47	mΩ
		V _{GS} =-4.5V, I _D =-3.5A		49	64	
Diode Forward Voltage	V _{SD}	I _S =-5.5A, V _{GS} =0V			-1.2	V
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-15V, V _{GS} =0V, f=1MHZ		572		pF
Output Capacitance	C _{oss}			82		
Reverse Transfer Capacitance	C _{rss}			70		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-15V, I _D =-4.1A		11.65		nC
Gate-Source Charge	Q _{gs}			2.32		
Gate-Drain Charge	Q _{gd}			2.08		
Reverse Recovery Charge	Q _{rr}	I _F =-10A, di/dt=100A/us		0.643		ns
Reverse Recovery Time	t _{rr}			15.7		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V, V _{DS} =-15V, R _L =15Ω R _{GEN} =2.5Ω		3.8		ns
Turn-on Rise Time	t _r			17.6		
Turn-off Delay Time	t _{D(off)}			17.8		
Turn-off fall Time	t _f			21.8		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² FR-4 board with 2oz copper.



■ Typical Performance Characteristics

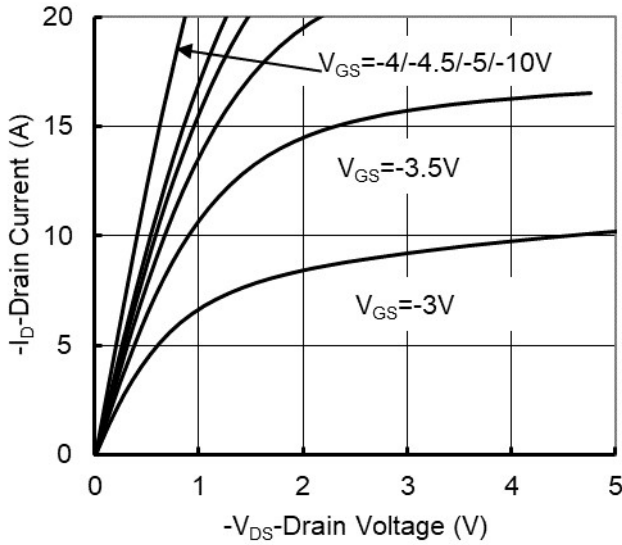


Figure1. Output Characteristics

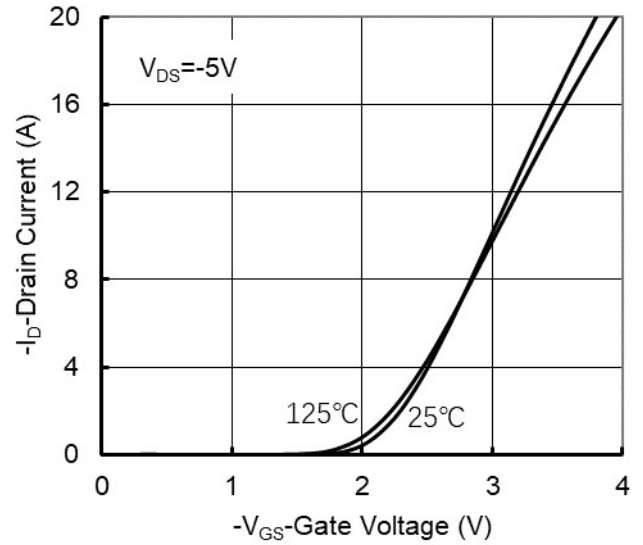


Figure2. Transfer Characteristics

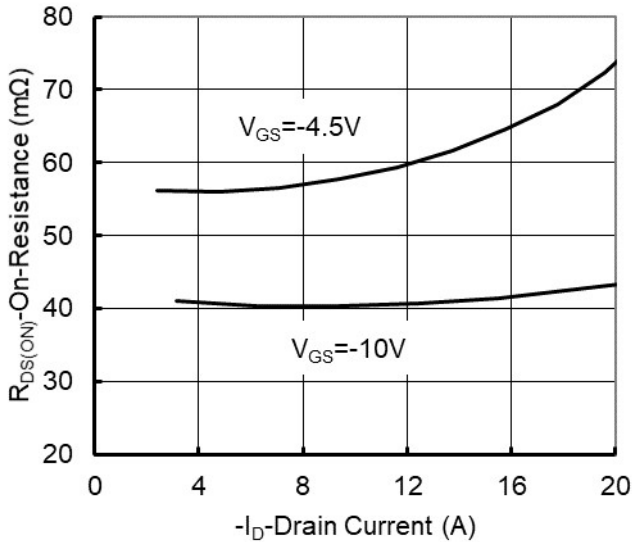


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

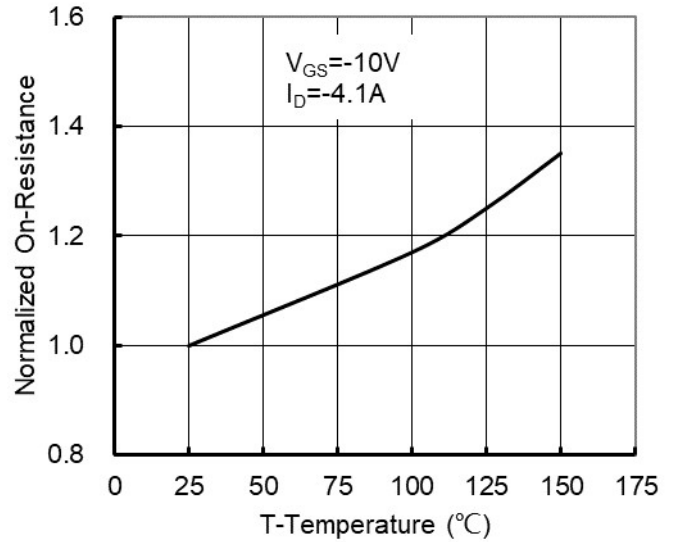


Figure 4: On-Resistance vs. Junction Temperature

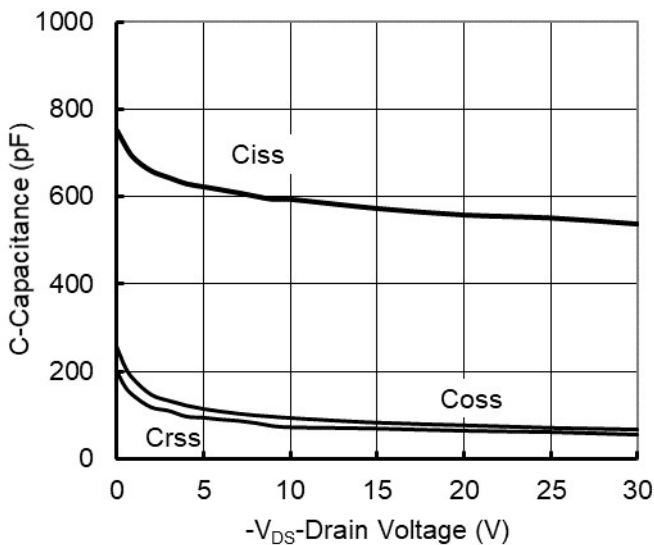


Figure5. Capacitance Characteristics

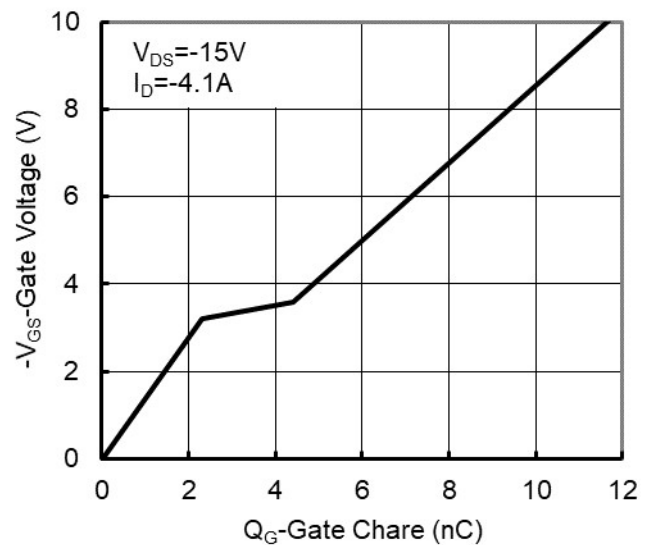


Figure6. Gate Charge

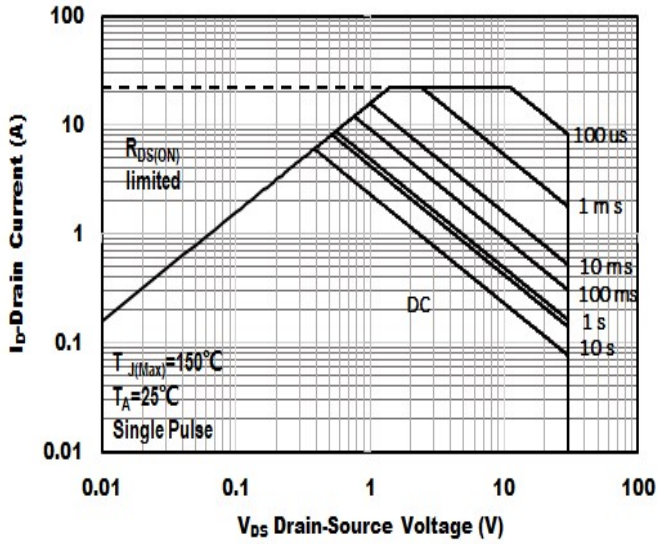


Figure7. Safe Operation Area

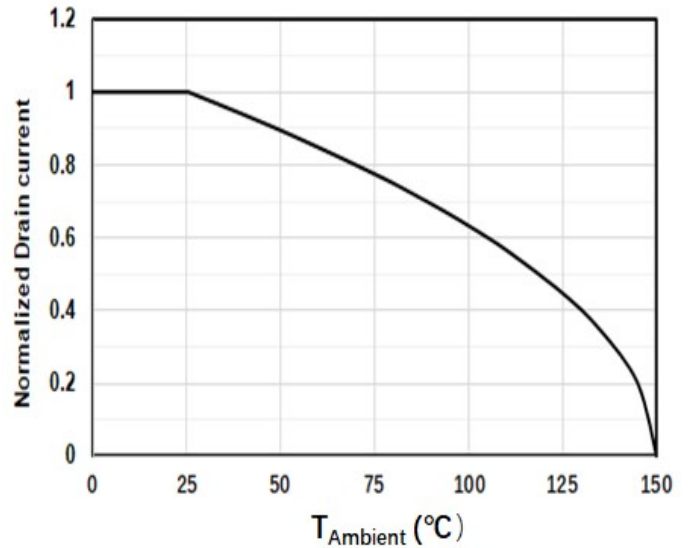


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

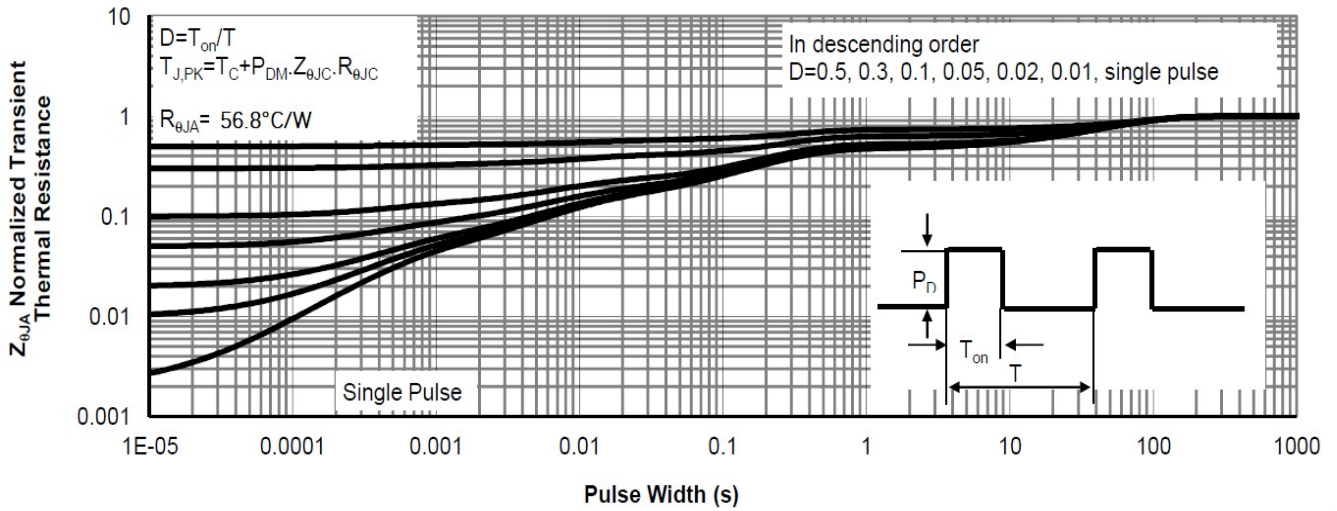
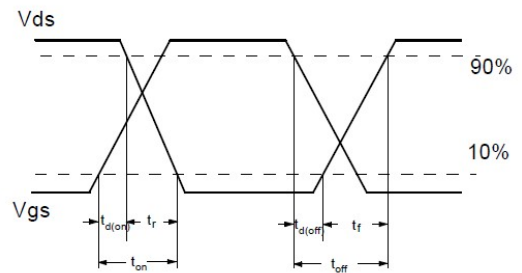
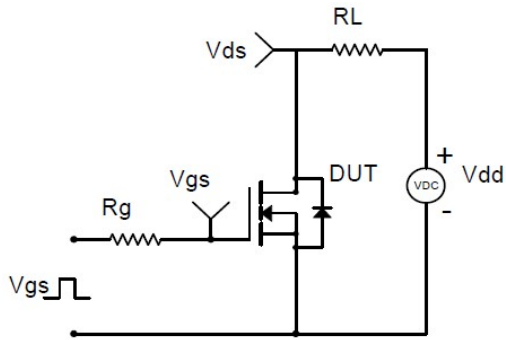
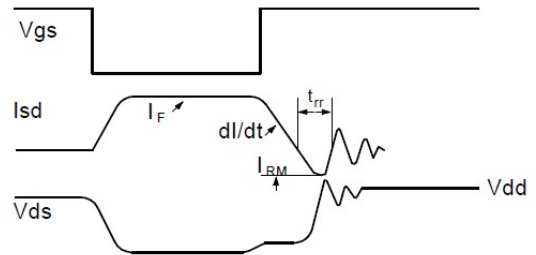
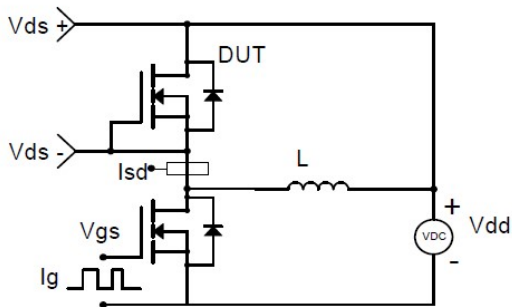


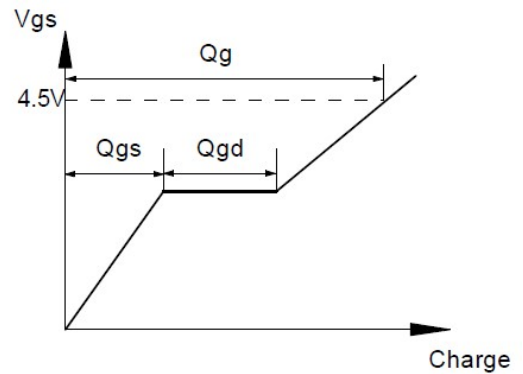
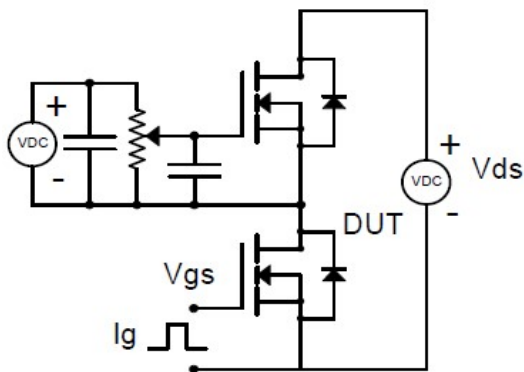
Figure9. Normalized Maximum Transient Thermal Impedance



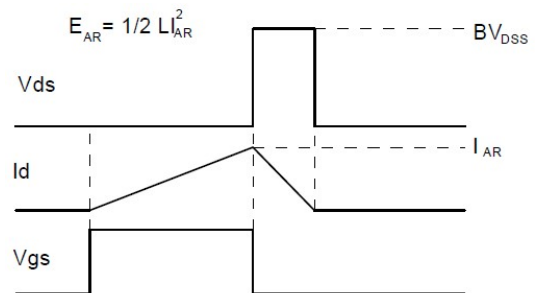
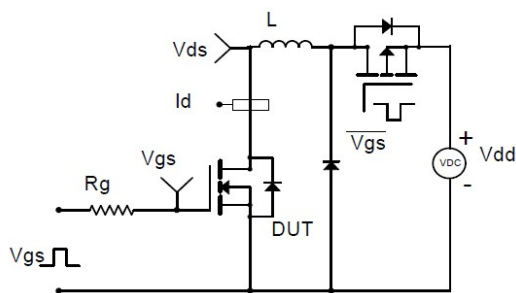
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

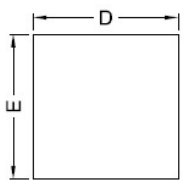


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

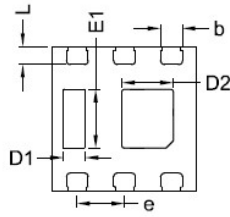


YJQ3407A

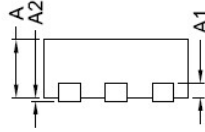
■ DFN2x2-6L Package Information



Top View
正面视图

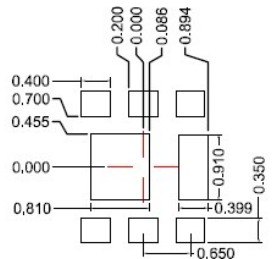


Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	1.90	2.00	2.10
E	1.90	2.00	2.10
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	0.20	0.30	0.40
D2	0.61	0.71	0.81
E1	0.71	0.81	0.91
L	0.15	0.25	0.35
b	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



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