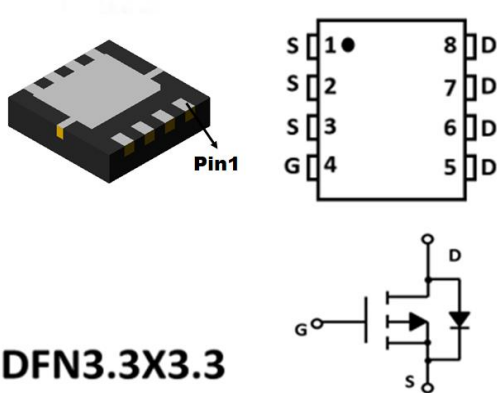


## P-Channel Enhancement Mode Field Effect Transistor



**DFN3.3X3.3**

### Product Summary

- $V_{DS}$  -30V
- $I_D$  -40A
- $R_{DS(ON)}$ ( at  $V_{GS}=-20V$ ) <13mohm
- $R_{DS(ON)}$ ( at  $V_{GS}=-10V$ ) <15mohm
- $R_{DS(ON)}$ ( at  $V_{GS}=-4.5V$ ) <25mohm

### General Description

- Trench Power LV MOSFET technology
- High density cell design for Low  $R_{DS(ON)}$
- High Speed switching

### Applications

- Battery protection
- Power management
- Load switch

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-source Voltage	$V_{DS}$	-30	V
Gate-source Voltage	$V_{GS}$	$\pm 25$	V
Drain Current	$I_D$	$T_A=25^\circ\text{C}$ @ Steady State	-40
		$T_A=70^\circ\text{C}$ @ Steady State	-33
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	-160	A
Single Pulse Avalanche Energy @ $L=0.5\text{mH}$ <sup>B</sup>	$E_{AS}$	72	mJ
Total Power Dissipation @ $T_A=25^\circ\text{C}$ <sup>C</sup>	$P_D$	32	W
Thermal Resistance Junction-to-Ambient @ Steady State <sup>D</sup>	$R_{\theta JC}$	4.0	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ40P03A	F1	Q40P03	5000	10000	100000	13" reel



# YJQ40P03A

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =-250μA	-30			V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V, T <sub>C</sub> =25°C			-1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±25V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.2	-1.8	-2.8	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -20V, I <sub>D</sub> =-20A		8.6	13	mΩ
		V <sub>GS</sub> = -10V, I <sub>D</sub> =-15A		9.8	15	
		V <sub>GS</sub> = -6.0V, I <sub>D</sub> =-12A		12.1	22	
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> =-10A		15.5	25	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-20A, V <sub>GS</sub> =0V			-1.2	V
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHZ		2152		pF
Output Capacitance	C <sub>oss</sub>			308		
Reverse Transfer Capacitance	C <sub>rss</sub>			242		
Gate Resistance	R <sub>g</sub>	f= 1MHZ			20	Ω
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-15V, I <sub>D</sub> =-12A		40.1		nC
Gate Source Charge	Q <sub>gs</sub>			8.4		
Gate Drain Charge	Q <sub>gd</sub>			8.6		
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = -12A, di/dt=100A/us		7.8		ns
Reverse Recovery Time	t <sub>rr</sub>			18		
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =-10V, V <sub>DD</sub> =-15V, I <sub>D</sub> =-1A, R <sub>GEN</sub> =2.5Ω		8		ns
Turn-on Rise Time	t <sub>r</sub>			19		
Turn-off Delay Time	t <sub>D(off)</sub>			75		
Turn-off Fall Time	t <sub>f</sub>			46		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

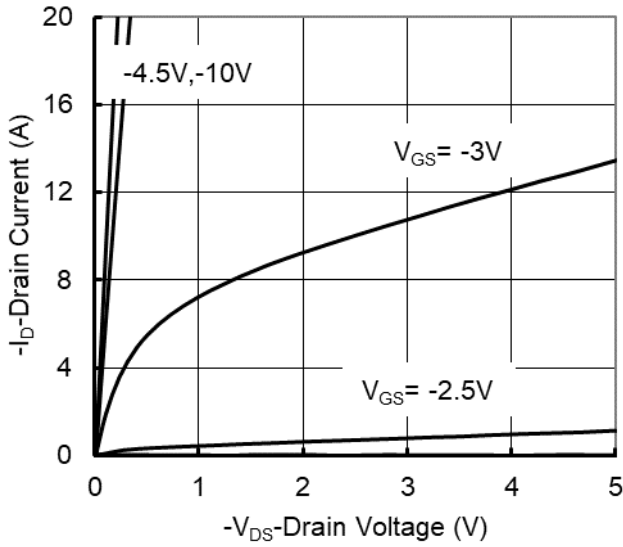


Figure 1. Output Characteristics

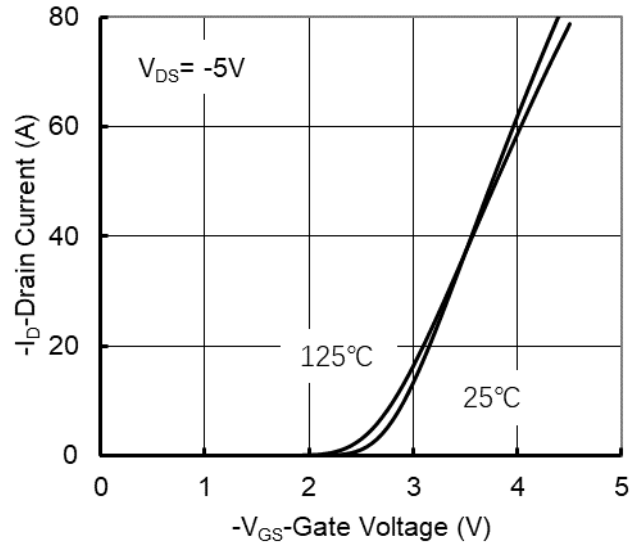


Figure 2. Transfer Characteristics

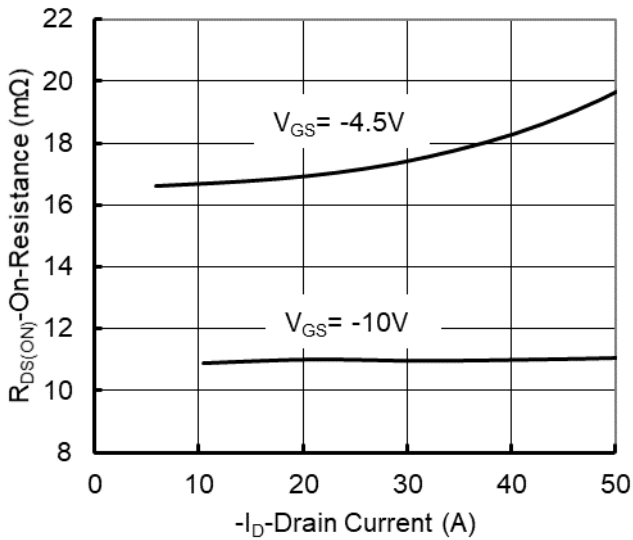


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

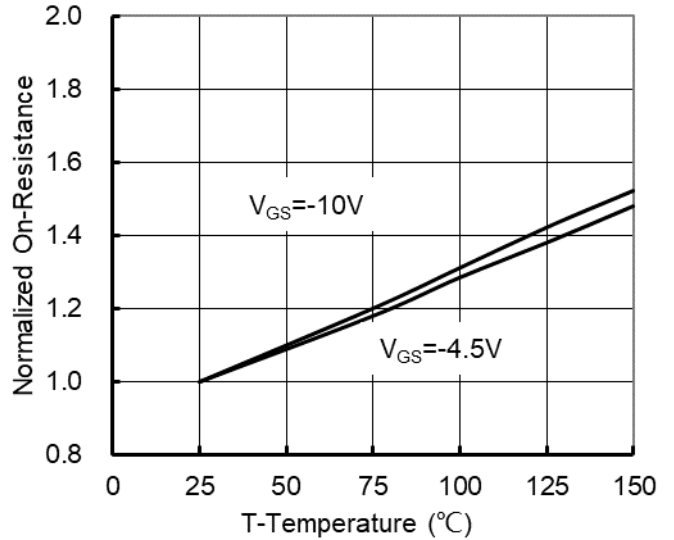


Figure 4. On-Resistance vs. Junction Temperature

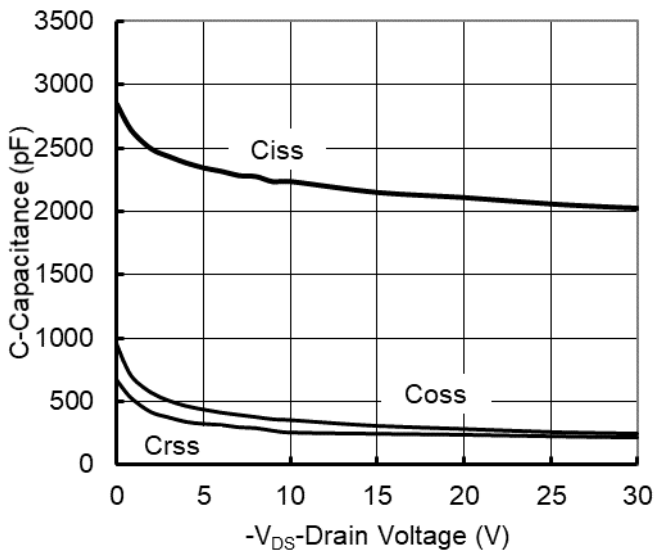


Figure 5. Capacitance Characteristics

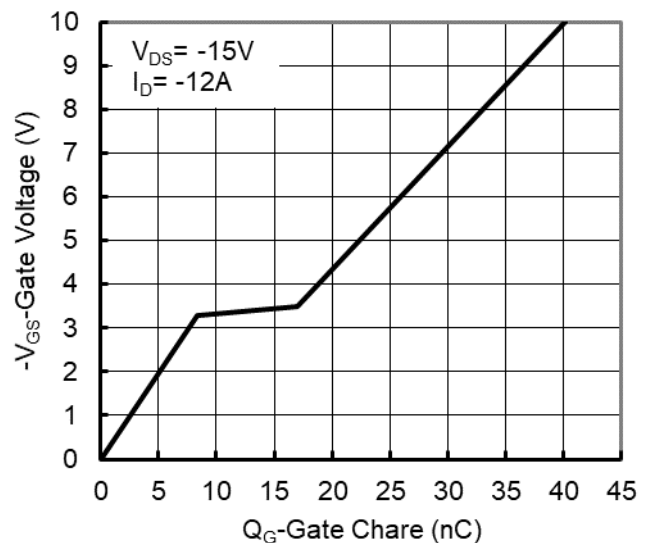


Figure 6. Gate Charge



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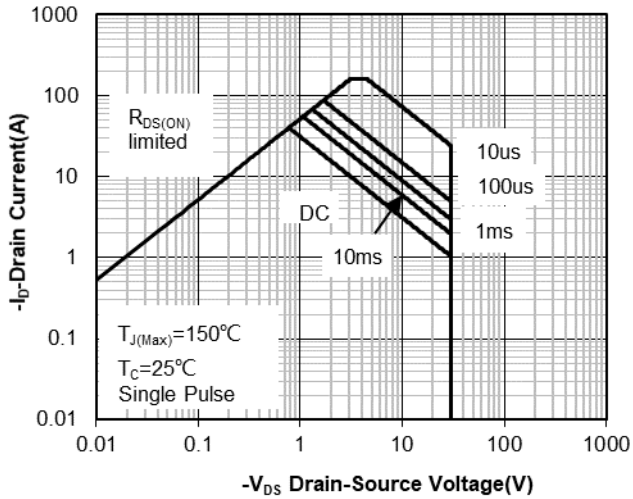


Figure 7. Safe Operation Area

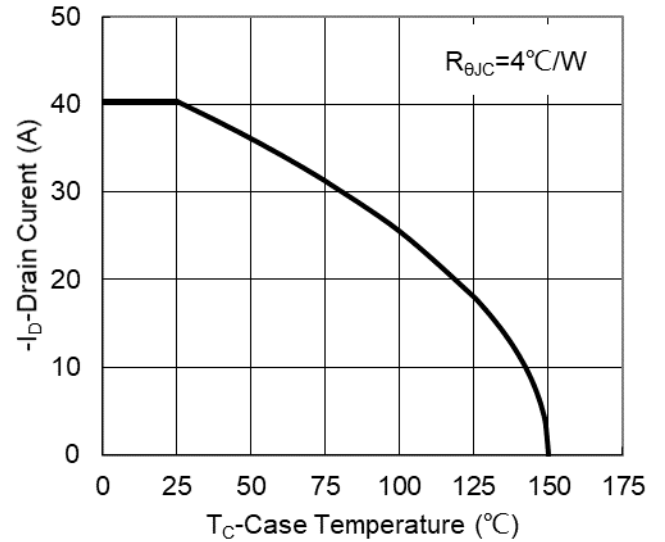


Figure 8. Maximum Continuous Drain Current vs Case Temperature

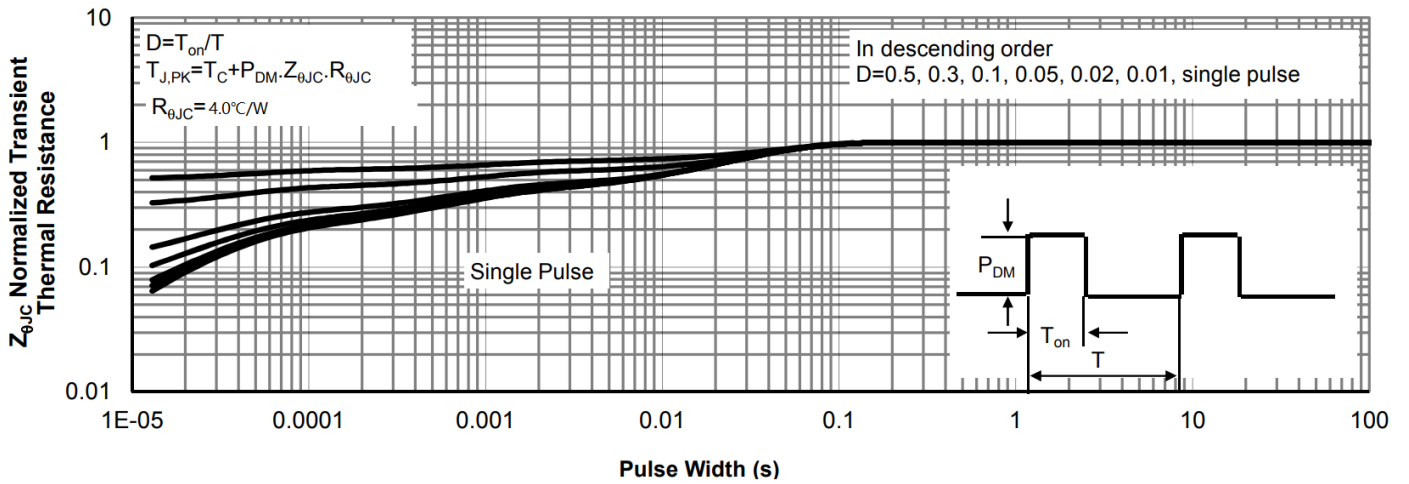
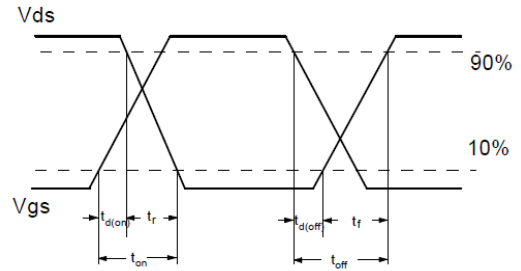
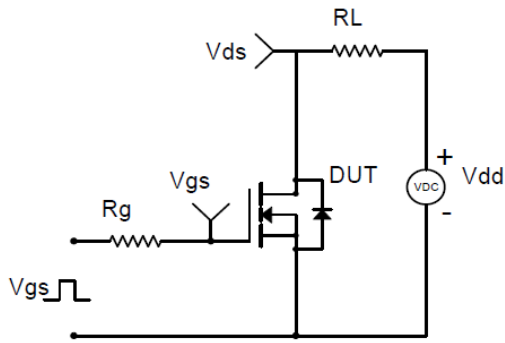
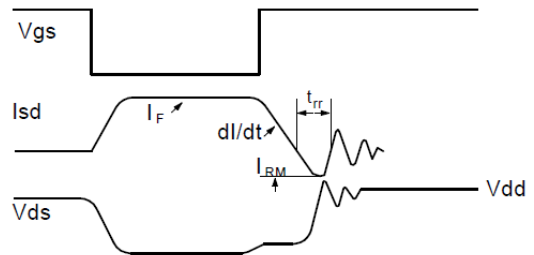
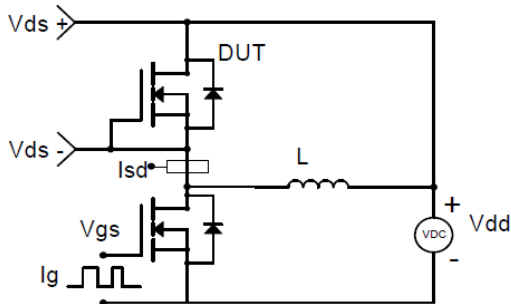


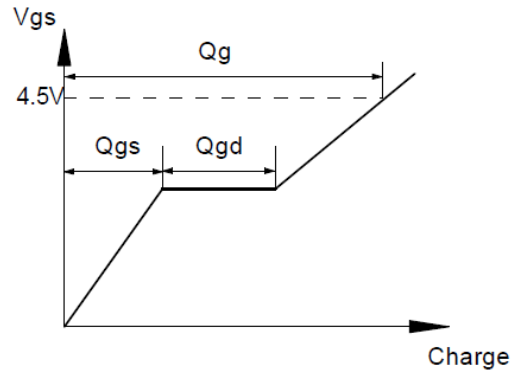
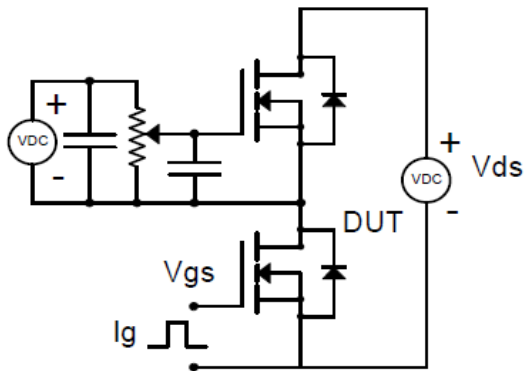
Figure 9. Normalized Maximum Transient Thermal Impedance



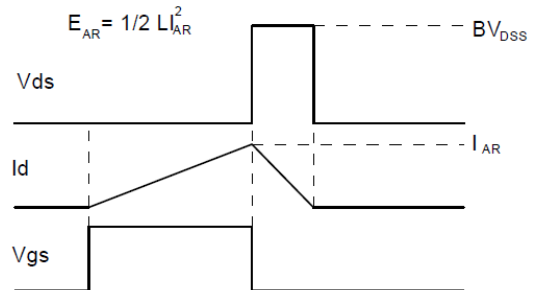
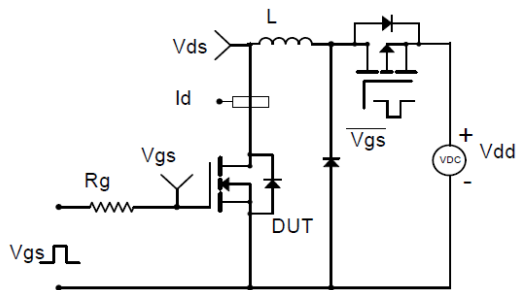
**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

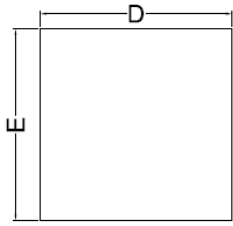


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**

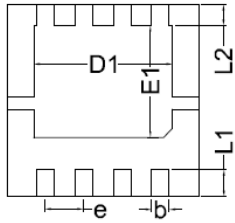


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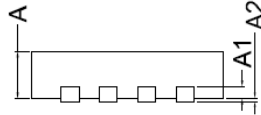
## ■ DFN3.3×3.3 Package information



Top View  
正面视图

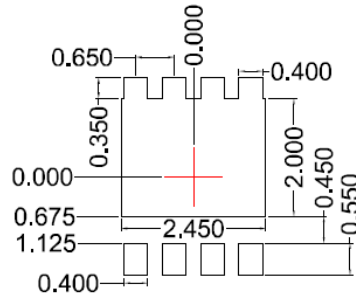


Bottom View  
背面视图



Side View  
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3,15	3,25	3,35
E	3,15	3,25	3,35
A	0,70	0,80	0,90
A1	0,20 BSC		
A2			0,10
D1	2,20	2,35	2,50
E1	1,80	1,90	2,00
L1	0,35	0,45	0,55
L2	0,35 BSC		
b	0,20	0,30	0,40
e	0,65 BSC		



Suggested Solder Pad Layout  
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0,10\text{mm}$ .
3. The pad layout is for reference purposes only.



## YJQ40P03A

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