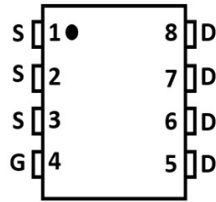
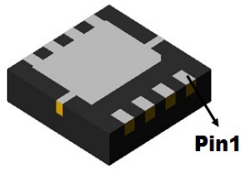
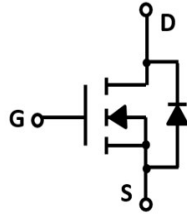


## N-Channel Enhancement Mode Field Effect Transistor



**DFN3.3X3.3**



### Product Summary

- $V_{DS}$  30V
- $I_D$  50A
- $R_{DS(ON)}$  (at  $V_{GS}=10V$ ) <6.0mohm
- $R_{DS(ON)}$  (at  $V_{GS}=4.5V$ ) <8.0mohm
- 100% UIS Tested
- 100%  $\nabla V_{DS}$  Tested

### General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$

### Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

| Parameter  |                         | Symbol          | Limit    | Unit                      |
|--|-------------------------|-----------------|----------|---------------------------|
| Drain-source Voltage                             |                         | $V_{DS}$        | 30       | V                         |
| Gate-source Voltage                              |                         | $V_{GS}$        | $\pm 20$ | V                         |
| Drain Current                                    | $T_C=25^\circ\text{C}$  | $I_D$           | 50       | A                         |
|  | $T_C=100^\circ\text{C}$ |                 | 35       |                           |
| Pulsed Drain Current <sup>A</sup>                |                         | $I_{DM}$        | 190      | A                         |
| Total Power Dissipation                          | $T_C=25^\circ\text{C}$  | $P_D$           | 30       | W                         |
|  | $T_C=100^\circ\text{C}$ |                 | 15       | W                         |
| Single Pulse Avalanche Energy <sup>B</sup>       |                         | $E_{AS}$        | 225      | mJ                        |
| Thermal Resistance Junction-to-Case <sup>C</sup> |                         | $R_{\theta JC}$ | 5        | $^\circ\text{C}/\text{W}$ |
| Junction and Storage Temperature Range           |                         | $T_J, T_{STG}$  | -55~+175 | $^\circ\text{C}$          |

### ■ Ordering Information (Example)

| PREFERRED P/N | PACKING CODE | Marking | MINIMUM PACKAGE(pcs) | INNER BOX QUANTITY(pcs) | OUTER CARTON QUANTITY(pcs) | DELIVERY MODE |
|---------------|--------------|---------|----------------------|-------------------------|----------------------------|---------------|
| YJQ50N03B     | F1           | Q50N03B | 5000                 | 10000                   | 100000                     | 13" reel      |



# YJQ50N03B

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

| Parameter                             | Symbol              | Conditions  | Min | Typ  | Max  | Units |
|---------------------------------------|---------------------|---|-----|------|------|-------|
| <b>Static Parameter</b>               |                     |   |     |      |      |       |
| Drain-Source Breakdown Voltage        | BV <sub>DSS</sub>   | V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA   | 30  |      |      | V     |
| Zero Gate Voltage Drain Current       | I <sub>DSS</sub>    | V <sub>DS</sub> =30V, V <sub>GS</sub> =0V   |     |      | 1    | μA    |
| Gate-Body Leakage Current             | I <sub>GSS</sub>    | V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V   |     |      | ±100 | nA    |
| Gate Threshold Voltage                | V <sub>GS(th)</sub> | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA                                 | 1.0 | 1.5  | 2.5  | V     |
| Static Drain-Source On-Resistance     | R <sub>DS(on)</sub> | V <sub>GS</sub> = 10V, I <sub>D</sub> =15A  |     | 3.9  | 6.0  | mΩ    |
|                                       |                     | V <sub>GS</sub> = 4.5V, I <sub>D</sub> =15A   |     | 6.0  | 8.0  |       |
| Diode Forward Voltage                 | V <sub>SD</sub>     | I <sub>S</sub> =20A, V <sub>GS</sub> =0V  |     |      | 1.2  | V     |
| Maximum Body-Diode Continuous Current | I <sub>S</sub>      |   |     |      | 50   | A     |
| <b>Dynamic Parameters</b>             |                     |   |     |      |      |       |
| Input Capacitance                     | C <sub>iss</sub>    | V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHZ   |     | 2191 |      | pF    |
| Output Capacitance                    | C <sub>oss</sub>    |   |     | 300  |      |       |
| Reverse Transfer Capacitance          | C <sub>rss</sub>    |   |     | 247  |      |       |
| <b>Switching Parameters</b>           |                     |   |     |      |      |       |
| Total Gate Charge                     | Q <sub>g</sub>      | V <sub>GS</sub> =10V, V <sub>DS</sub> =15V, I <sub>D</sub> =20A                           |     | 46.3 |      | nC    |
| Gate-Source Charge                    | Q <sub>gs</sub>     |   |     | 8.8  |      |       |
| Gate-Drain Charge                     | Q <sub>gd</sub>     |   |     | 9.2  |      |       |
| Reverse Recovery Charge               | Q <sub>rr</sub>     | I <sub>F</sub> =20A, di/dt=500A/us  |     | 1.6  |      | ns    |
| Reverse Recovery Time                 | t <sub>rr</sub>     |   |     | 11   |      |       |
| Turn-on Delay Time                    | t <sub>D(on)</sub>  | V <sub>GS</sub> =10V, V <sub>DD</sub> =15V, R <sub>L</sub> =0.75Ω<br>R <sub>GEN</sub> =3Ω |     | 11   |      | ns    |
| Turn-on Rise Time                     | t <sub>r</sub>      |   |     | 80   |      |       |
| Turn-off Delay Time                   | t <sub>D(off)</sub> |   |     | 39   |      |       |
| Turn-off fall Time                    | t <sub>f</sub>      |   |     | 92   |      |       |

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R<sub>θJA</sub> is the sum of the junction-to-Case and Case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design, while R<sub>θJA</sub> is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



## ■ Typical Performance Characteristics

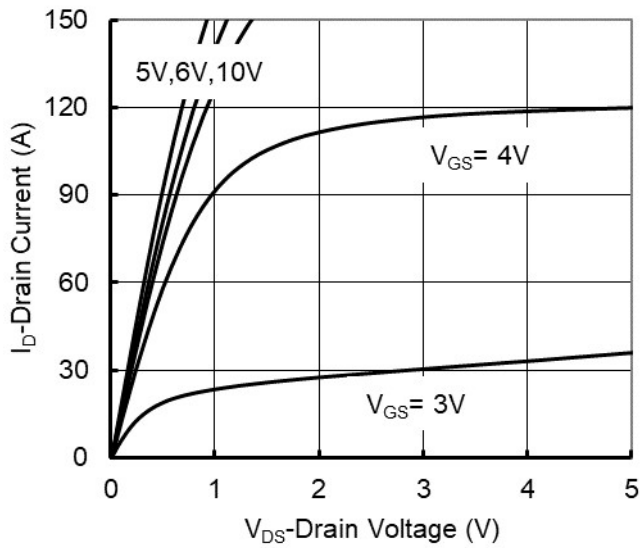


Figure 1. Output Characteristics

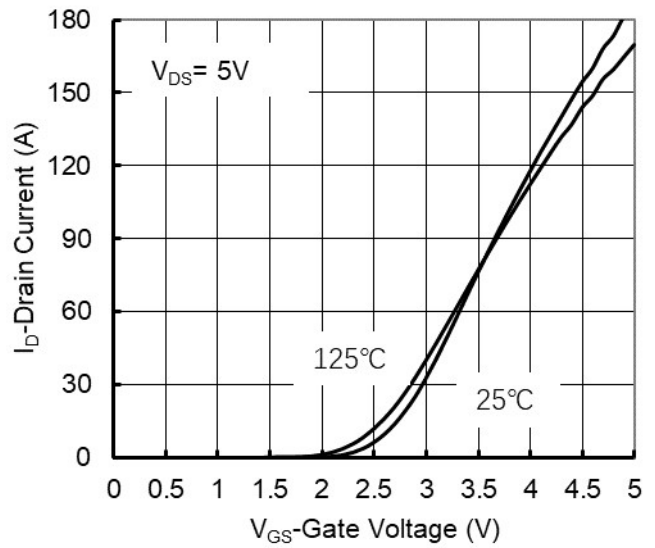


Figure 2. Transfer Characteristics

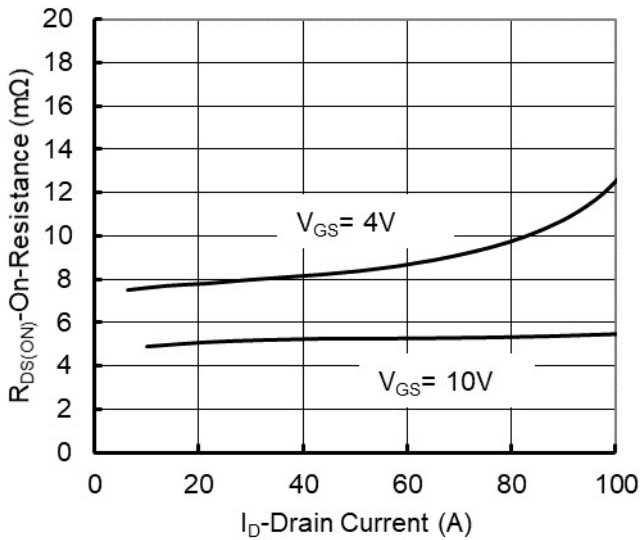


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

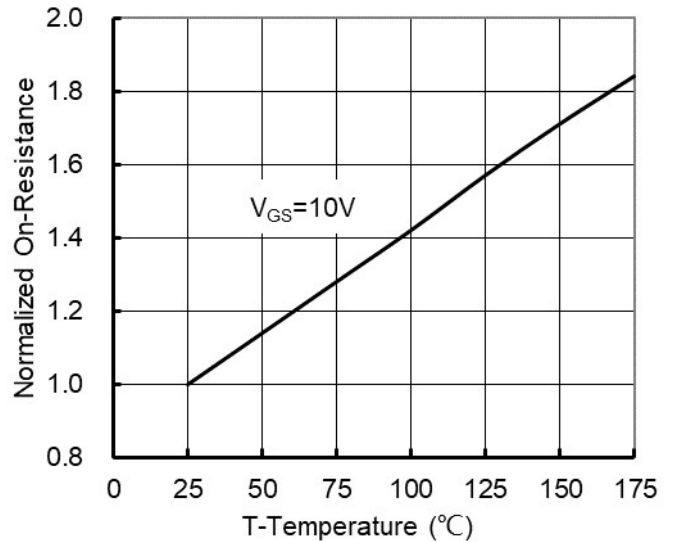


Figure 4. On-Resistance vs. Junction Temperature

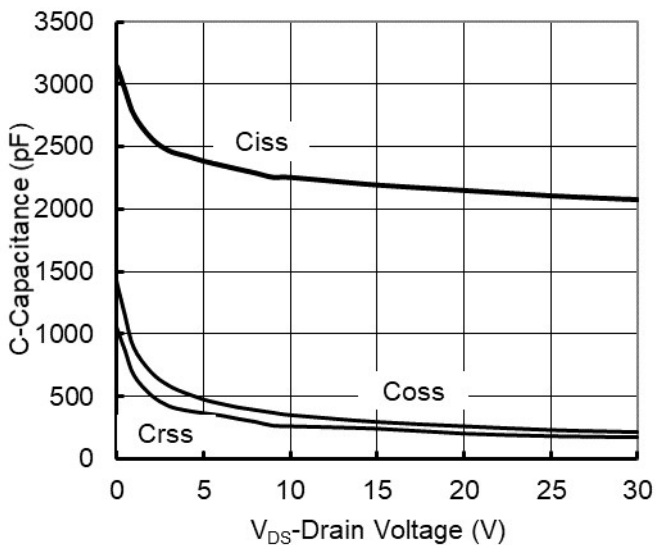


Figure 5. Capacitance Characteristics

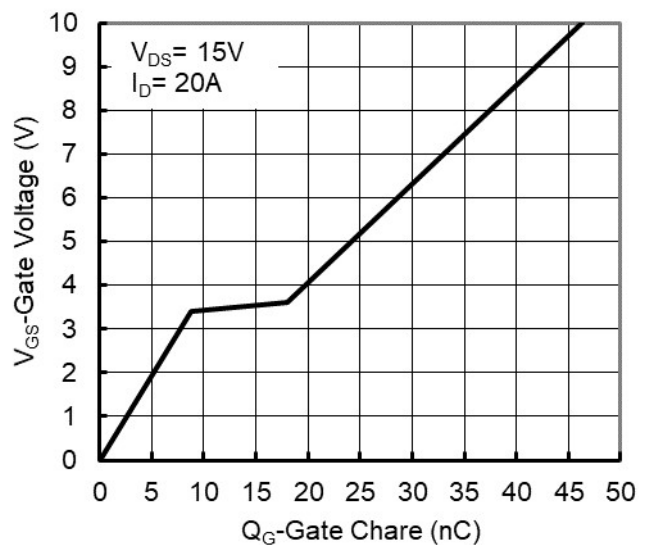


Figure 6. Gate Charge



# YJQ50N03B

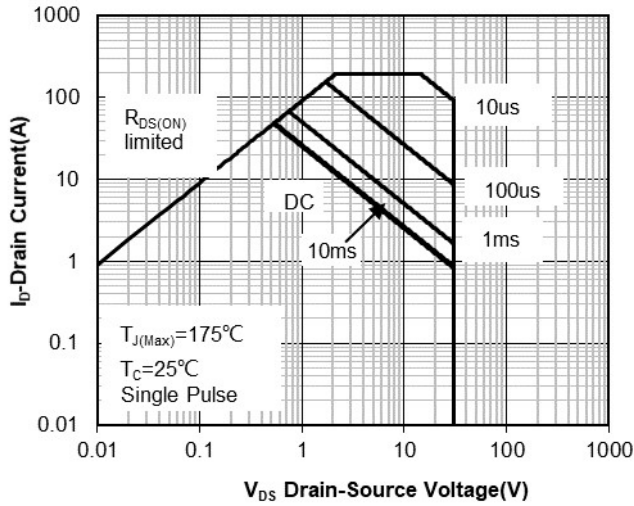


Figure 7. Safe Operation Area

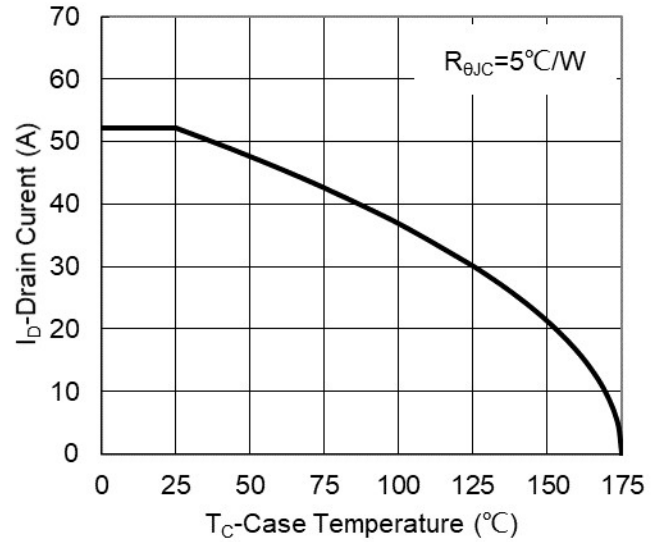


Figure 8. Maximum Continuous Drain Current vs Case Temperature

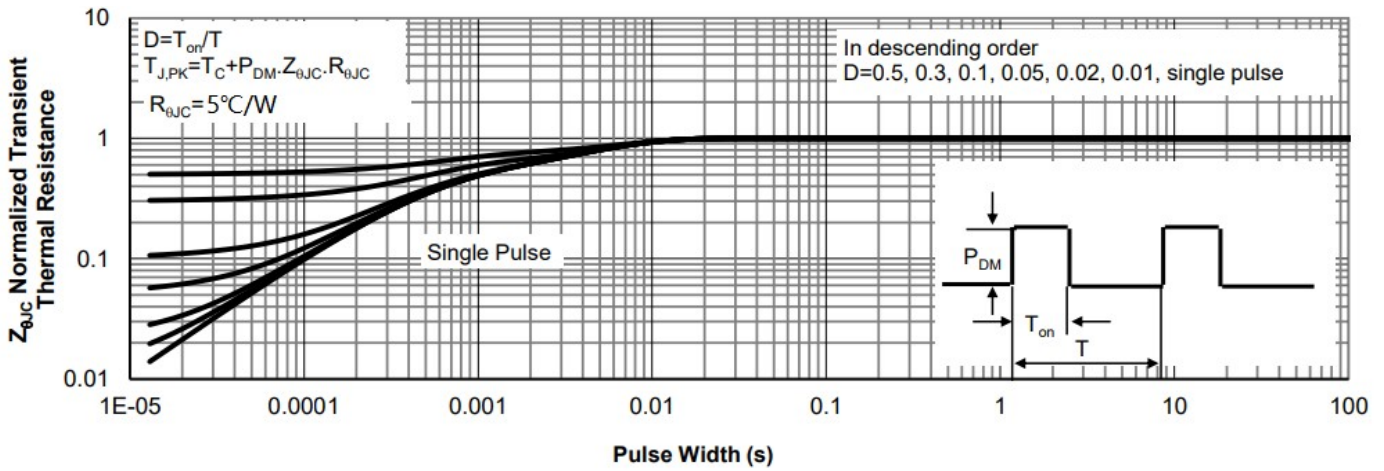


Figure 9. Normalized Maximum Transient Thermal Impedance



**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**

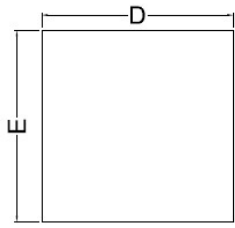


**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**

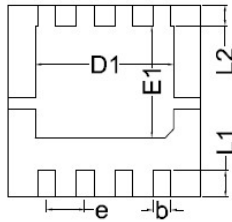


# YJQ50N03B

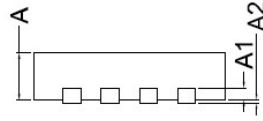
## ■ DFN3.3X3.3 Package information



Top View  
正面视图

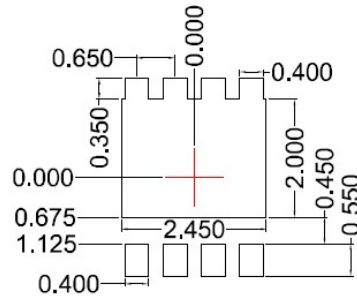


Bottom View  
背面视图



Side View  
侧面视图

| SYMBOL | MILLIMETER |      |      |
|--------|------------|------|------|
|        | MIN        | NOM  | MAX  |
| D      | 3.15       | 3.25 | 3.35 |
| E      | 3.15       | 3.25 | 3.35 |
| A      | 0.70       | 0.80 | 0.90 |
| A1     | 0.20 BSC   |      |      |
| A2     |            |      | 0.10 |
| D1     | 2.20       | 2.35 | 2.50 |
| E1     | 1.80       | 1.90 | 2.00 |
| L1     | 0.35       | 0.45 | 0.55 |
| L2     | 0.35 BSC   |      |      |
| b      | 0.20       | 0.30 | 0.40 |
| e      | 0.65 BSC   |      |      |



Suggested Solder Pad Layout  
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.10\text{mm}$ .
3. The pad layout is for reference purposes only.



## YJQ50N03B

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