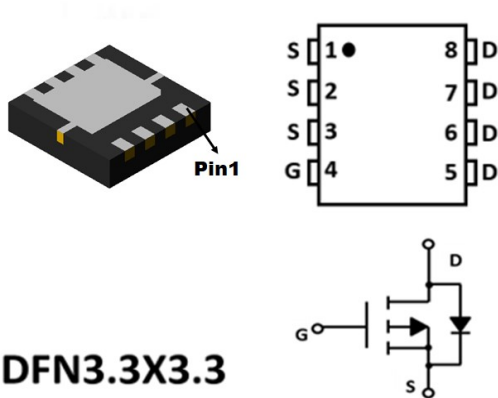


P-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} -20V
- I_D -55A
- $R_{DS(ON)}$ (at $V_{GS} = -4.5V$) < 8.3mohm
- $R_{DS(ON)}$ (at $V_{GS} = -2.5V$) < 10mohm
- $R_{DS(ON)}$ (at $V_{GS} = -1.8V$) < 15mohm
- 100% UIS Tested
- 100% ∇V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$

Applications

- High current load applications
- Load switching
- Hard switched and high frequency Circuits
- Uninterruptible power supply

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	-20	V
Gate-source Voltage		V_{GS}	± 10	V
Drain Current	$T_A=25^\circ\text{C}$	I_D	55	A
	$T_A=100^\circ\text{C}$		35	
Pulsed Drain Current ^A		I_{DM}	160	A
Single Pulse Avalanche Energy ^B		E_{AS}	75	mJ
Total Power Dissipation	$T_C=25^\circ\text{C}$	P_D	38	W
	$T_A=25^\circ\text{C}$		3.2	
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	3.3	$^\circ\text{C}/\text{W}$
		$R_{\theta JA}$	39	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ55P02A	F1	Q55P02A	5000	10000	100000	13" reel



YJQ55P02A

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	-20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±10V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =-250μA	-0.4	-0.62	-1.0	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = -4.5V, I _D =-15A		6.5	8.3	mΩ
		V _{GS} = -2.5V, I _D =-10A		8.0	10.0	
		V _{GS} = -1.8V, I _D =-8.0A		10.3	15	
Diode Forward Voltage	V _{SD}	I _S =-20A, V _{GS} =0V		-0.7	-1.2	V
Maximum Body-Diode Continuous Current	I _S				-55	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =-10V, V _{GS} =0V, f=1MHZ		6358		pF
Output Capacitance	C _{oss}			690		
Reverse Transfer Capacitance	C _{rss}			477		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =-10V, V _{DS} =-15V, I _D =-9.1A		12.7		nC
Gate-Source Charge	Q _{gs}			21		
Gate-Drain Charge	Q _{gd}			149		
Reverse Recovery Charge	Q _{rr}	I _F =-6A, di/dt=100A/us		25.2		
Reverse Recovery Time	t _{rr}			46		
Turn-on Delay Time	t _{D(on)}	V _{GS} =-10V, V _{DD} =-15V, I _D =-6A R _{GEN} =2.5Ω		11		ns
Turn-on Rise Time	t _r			36		
Turn-off Delay Time	t _{D(off)}			182		
Turn-off fall Time	t _f			191		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

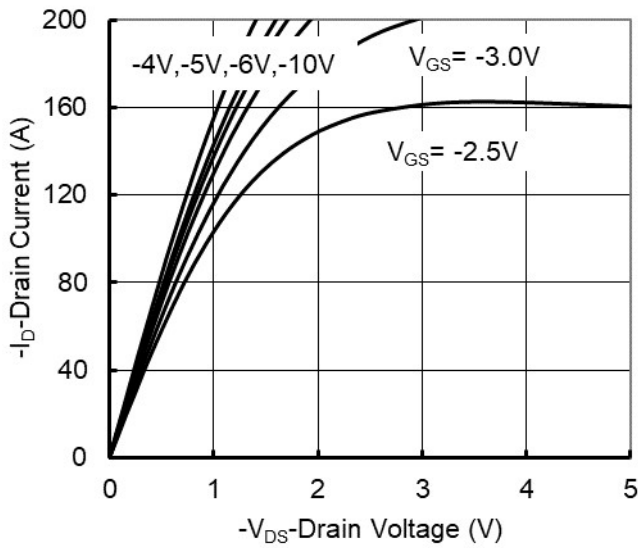


Figure 1. Output Characteristics

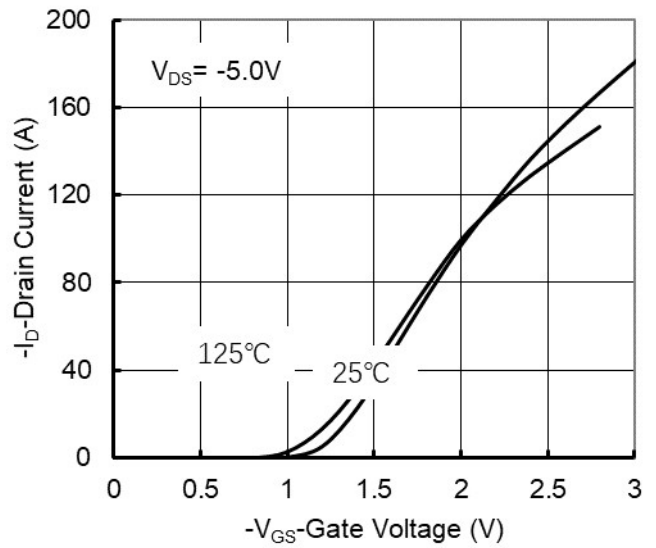


Figure 2. Transfer Characteristics

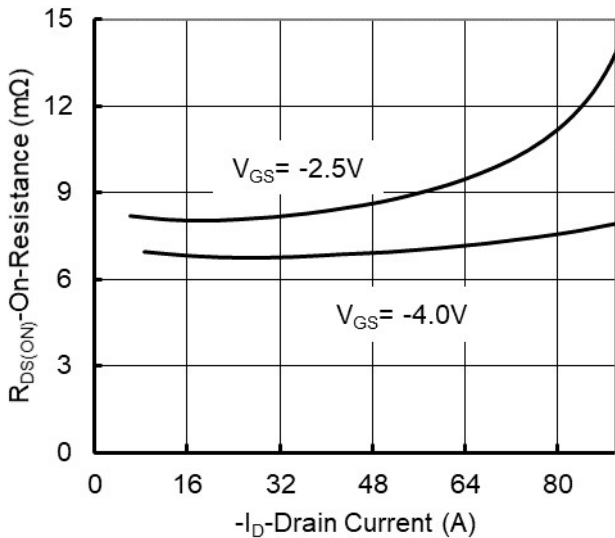


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

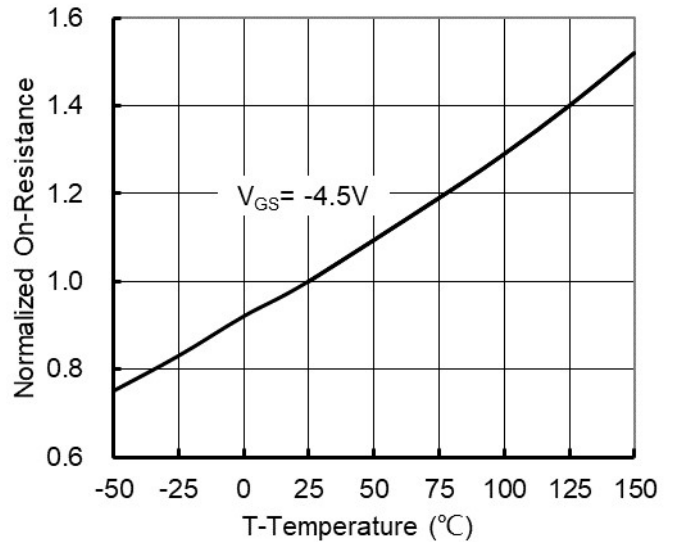


Figure 4. On-Resistance vs. Junction Temperature

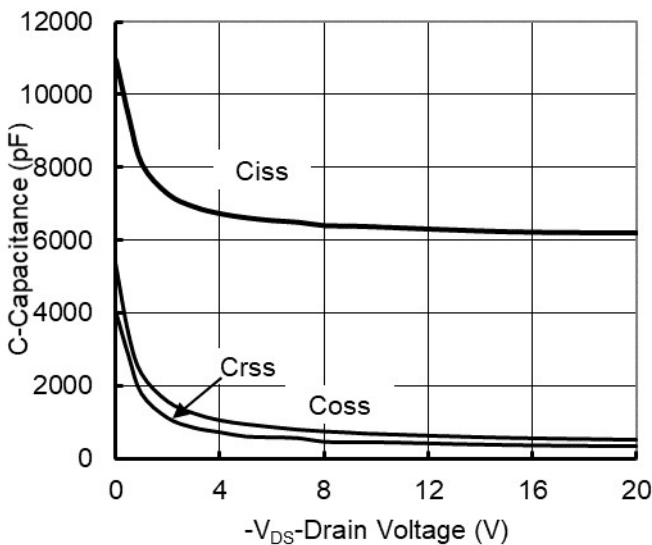


Figure 5. Capacitance Characteristics

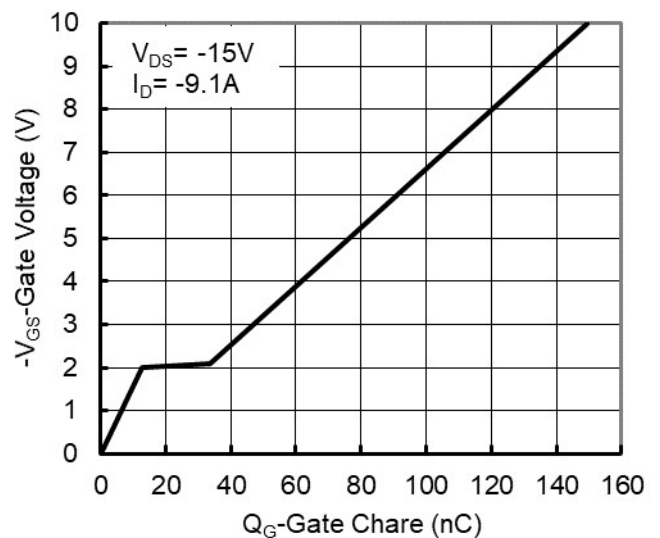


Figure 6. Gate Charge



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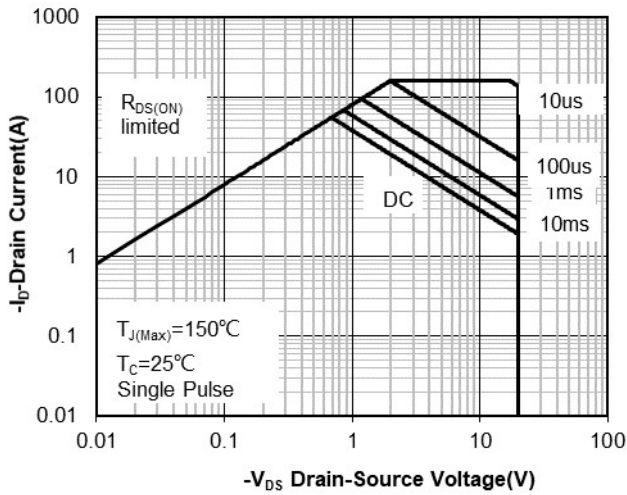


Figure 7. Safe Operation Area

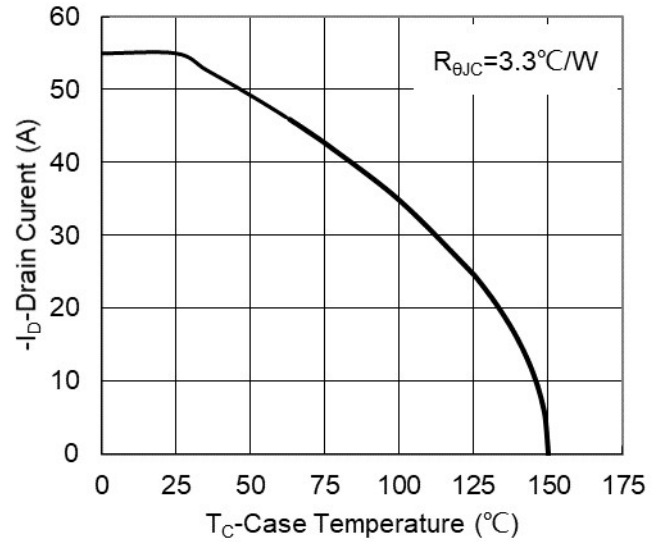


Figure 8. Maximum Continuous Drain Current vs Case Temperature

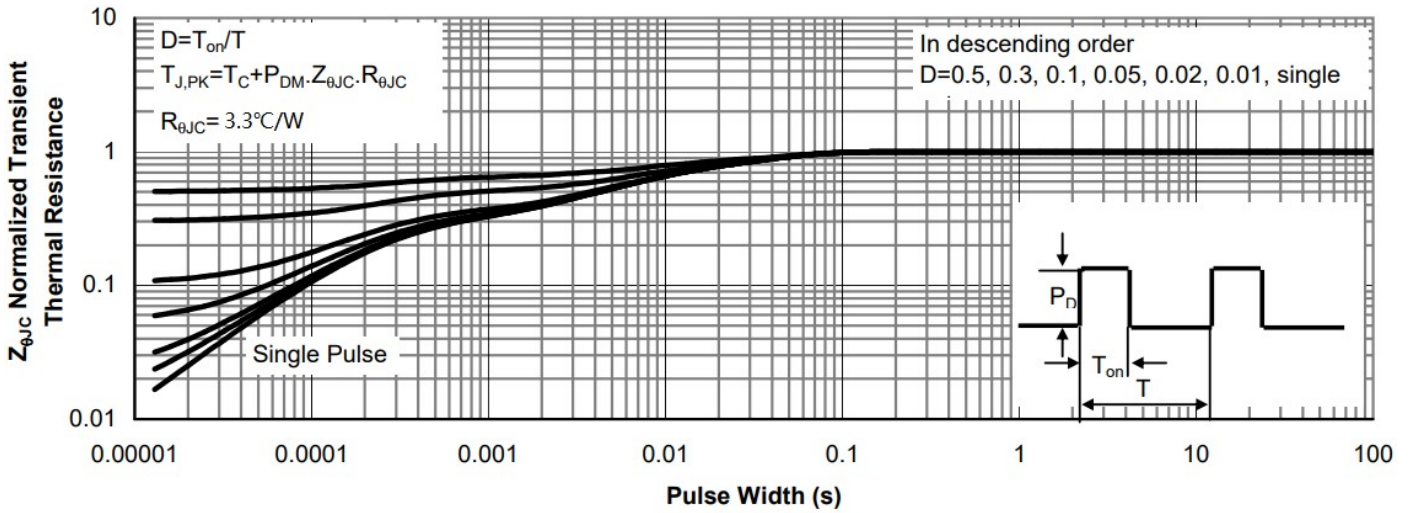
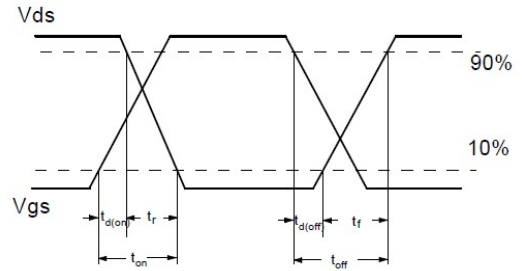
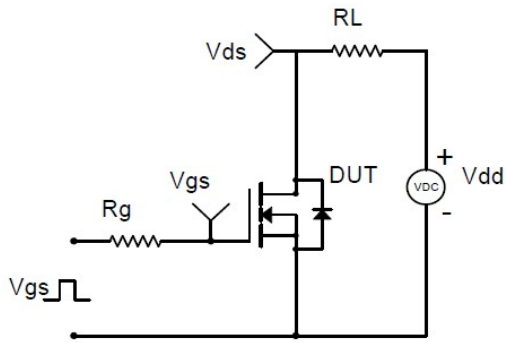
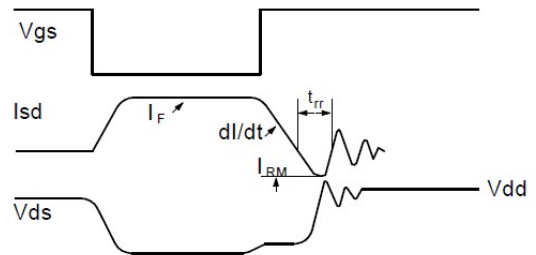
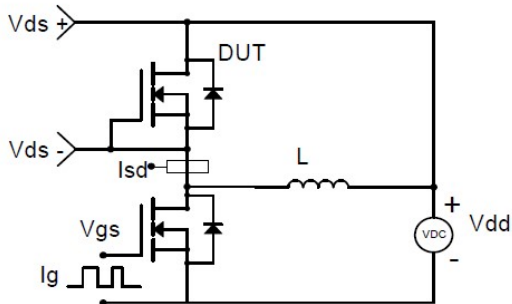


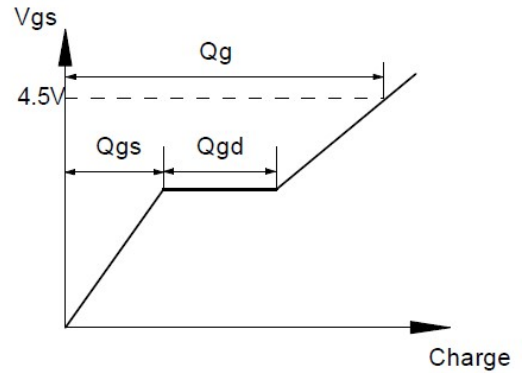
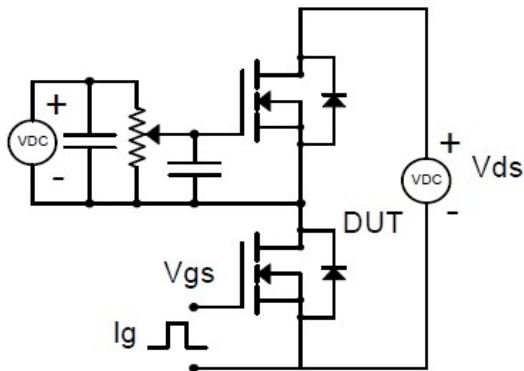
Figure 9. Normalized Maximum Transient Thermal Impedance



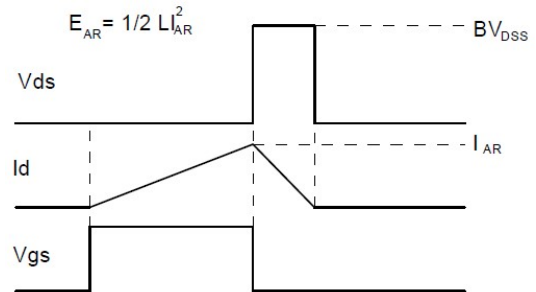
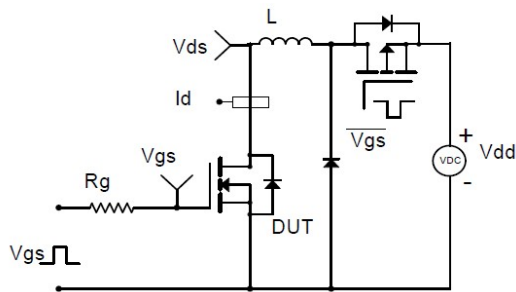
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

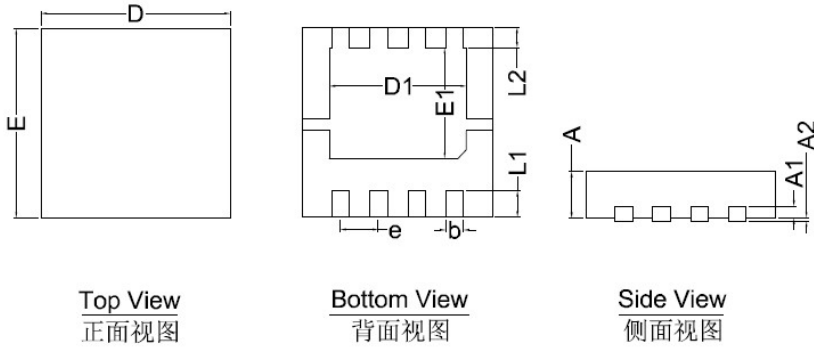


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

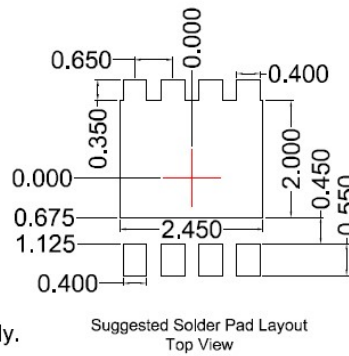


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DFN3.3X3.3 Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



- Note:
1. Controlling dimension: in millimeters.
 2. General tolerance: $\pm 0.10\text{mm}$.
 3. The pad layout is for reference purposes only.



YJQ55P02A

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