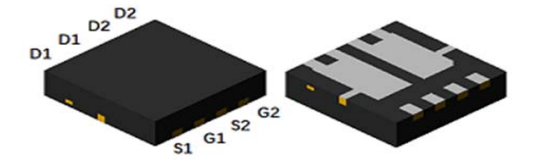
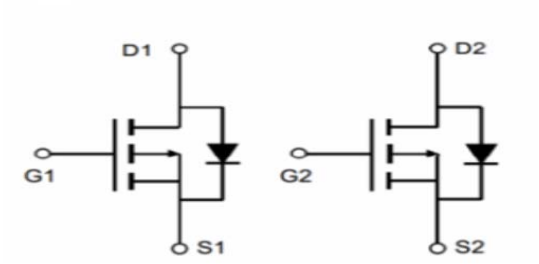
# P-Channel Enhancement Mode Field Effect Transistor

## DFN3.3X3.3




## Product Summary

- $V_{DS}$ -20V
- $I_D$ -30A
- $R_{DS(ON)}$( at $V_{GS}$= -4.5V) ＜19mohm
- $R_{DS(ON)}$( at $V_{GS}$= -2.5V) ＜22mohm
- $R_{DS(ON)}$( at $V_{GS}$= -1.8V) ＜30mohm

## General Description

- Trench Power MV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching

## Applications

- Battery protection
- Load switch
- Power management

## ■ Absolute Maximum Ratings ($T_A$=25℃unless otherwise noted)

| Parameter | | Symbol | Maximum | Unit |
|---|---|---|---|---|
| Drain-source Voltage | | $V_{DS}$ | -20 | V |
| Gate-source Voltage | | $V_{GS}$ | ±10 | V |
| Drain Current [B] | $T_A$=25℃ @ Steady State | $I_D$ | -30 | A |
| | $T_A$=100℃ @ Steady State | | -19 | |
| Drain Current [B] | $T_A$=25℃ @ Steady State | $I_D$ | -10 | A |
| | $T_A$=70℃ @ Steady State | | -8 | |
| Pulsed Drain Current [A] | | $I_{DM}$ | -55 | A |
| Single Pulse Avalanche Energy[B] | | $E_{AS}$ | 31 | mJ |
| Total Power Dissipation [B] | $T_A$=25℃ @ Steady State | $P_D$ | 32 | W |
| | $T_A$=100℃ @ Steady State | | 12.8 | |
| Total Power Dissipation [B] | $T_A$=25℃ @ Steady State | $P_D$ | 3 | W |
| | $T_A$=70℃ @ Steady State | | 1.9 | |
| Thermal Resistance Junction-to-Ambient @ Steady State [B] | | $R_{\theta JC}$ | 3.9 | ℃/ W |
| Thermal Resistance Junction-to-Case @ Steady State [C] | | $R_{\theta JA}$ | 42 | ℃/ W |
| Junction and Storage Temperature Range | | $T_J$ ,$T_{STG}$ | -55～+150 | ℃ |

## ■ Ordering Information (Example)

| PREFERED P/N | PACKING CODE | Marking | MINIMUM PACKAGE(pcs) | INNER BOX QUANTITY(pcs) | OUTER CARTON QUANTITY(pcs) | DELIVERY MODE |
|---|---|---|---|---|---|---|
| YJQ30P02A | F1 | Q30P02 | 5000 | 10000 | 100000 | 13“ reel |

## ■ Electrical Characteristics ($T_J$=25℃ unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Static Parameter** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$= 0V, $I_D$=-250μA | -20 | | | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$=-20V,$V_{GS}$=0V,$T_C$=25℃ | | | -1 | μA |
| Gate-Body Leakage Current | $I_{GSS}$ | $V_{GS}$= ±10V, $V_{DS}$=0V | | | ±100 | nA |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$= $V_{GS}$, $I_D$=-250μA | -0.4 | -0.62 | -1.0 | V |
| Static Drain-Source On-Resistance | $R_{DS(ON)}$ | $V_{GS}$= -4.5V, $I_D$=-15A | | 11 | 19 | mΩ |
| | | $V_{GS}$= -2.5V, $I_D$=-8A | | 14 | 22 | |
| | | $V_{GS}$= -1.8V, $I_D$=-6.0A | | 20 | 30 | |
| Diode Forward Voltage | $V_{SD}$ | $I_S$=-30A,$V_{GS}$=0V | | -0.8 | -1.2 | V |
| Maximum Body-Diode Continuous Current | $I_S$ | | | | -30 | A |
| **Dynamic Parameters** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$=-10V,$V_{GS}$=0V,f=1MHZ | | 2992 | | pF |
| Output Capacitance | $C_{oss}$ | | | 330 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 272 | | |
| **Switching Parameters** | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{GS}$=-10V,$V_{DS}$=-15V,$I_D$=-9.1A | | 72.8 | | nC |
| Gate Source Charge | $Q_{gs}$ | | | 6.6 | | |
| Gate Drain Charge | $Q_{gd}$ | | | 10.1 | | |
| Reverse Recovery Charge | $Q_{rr}$ | $I_F$=-6A, di/dt=100A/us | | 34 | | |
| Reverse Recovery Time | $t_{rr}$ | | | 67 | | ns |
| Turn-on Delay Time | $t_{D(on)}$ | $V_{GS}$=-10V,$V_{DS}$=-15V, $I_D$=-6A, $R_{GEN}$=2.5Ω | | 7 | | |
| Turn-on Rise Time | $t_r$ | | | 33 | | |
| Turn-off Delay Time | $t_{D(off)}$ | | | 130 | | |
| Turn-off Fall Time | $t_f$ | | | 132 | | |

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.

B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

## ■ Typical Performance Characteristics

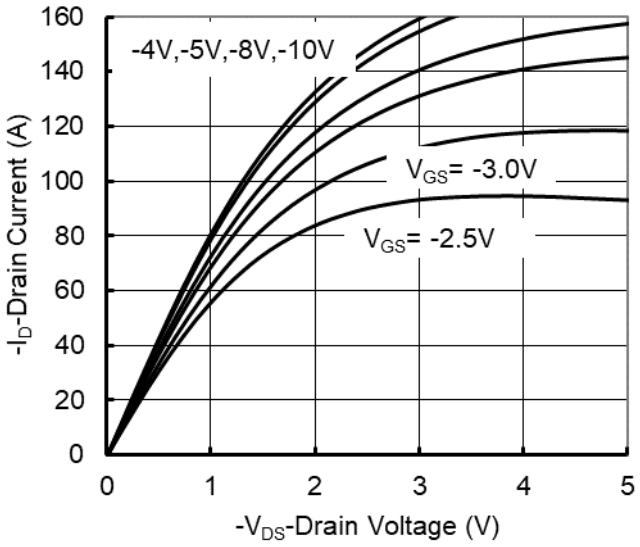



**Figure 1. Output Characteristics**

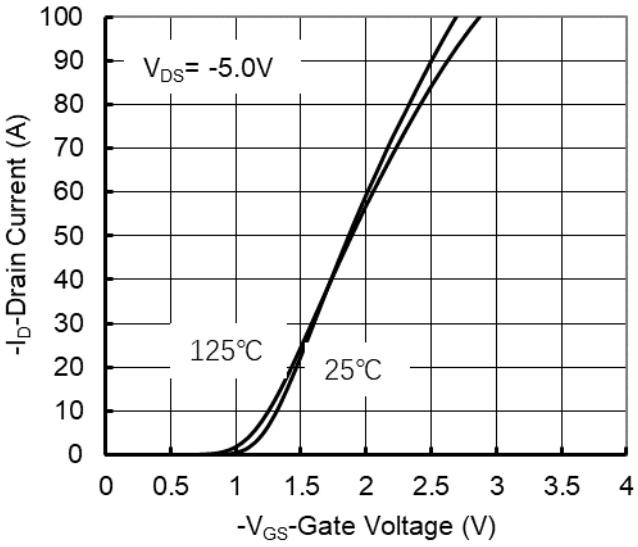



**Figure 2. Transfer Characteristics**

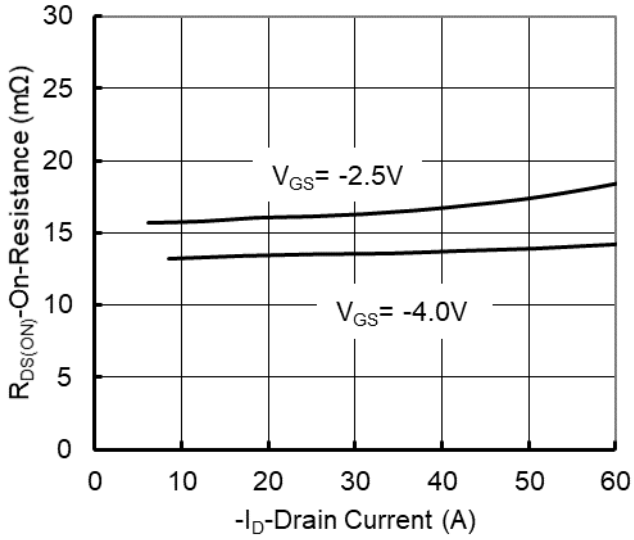



**Figure 3. On-Resistance vs. Drain Current and Gate Voltage**

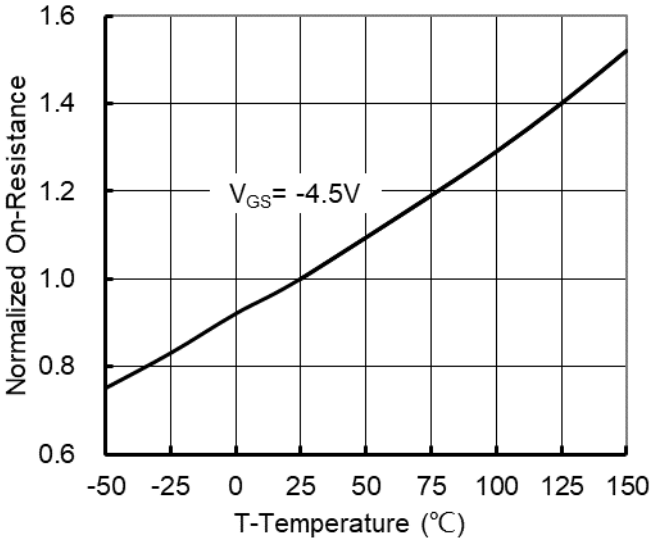



**Figure 4. On-Resistance vs. Junction Temperature**

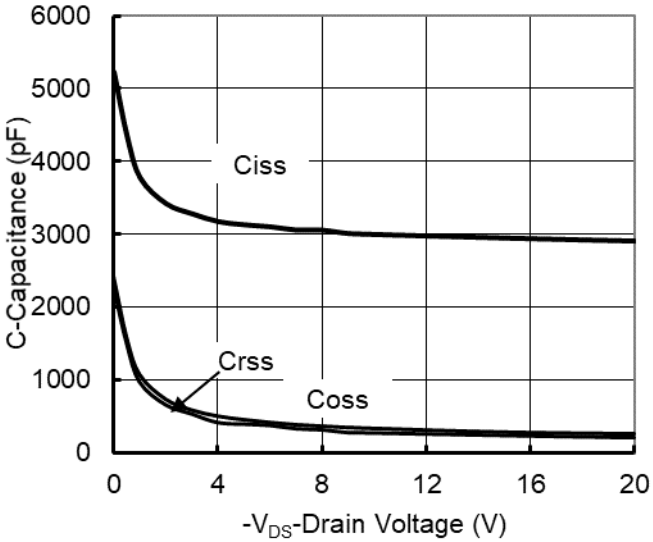



**Figure 5. Capacitance Characteristics**

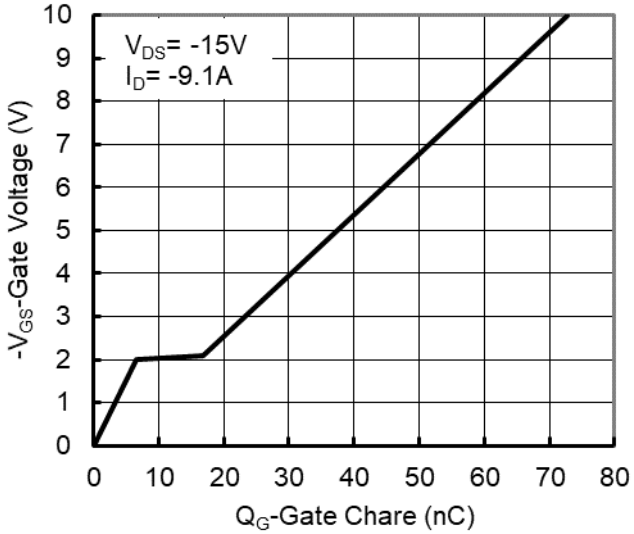



**Figure 6. Gate Charge**

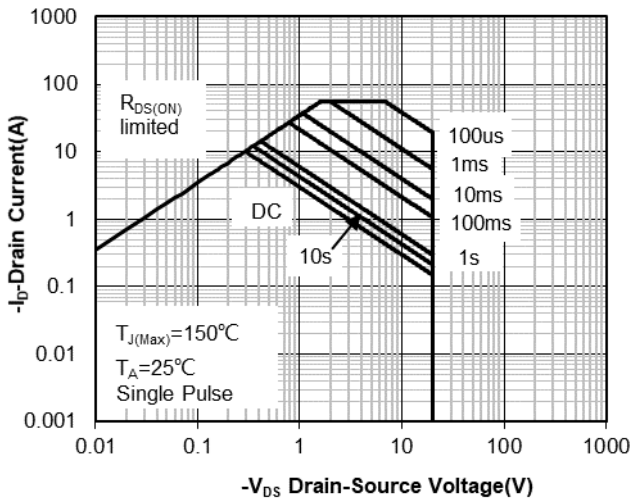



**Figure 7. Safe Operation Area**

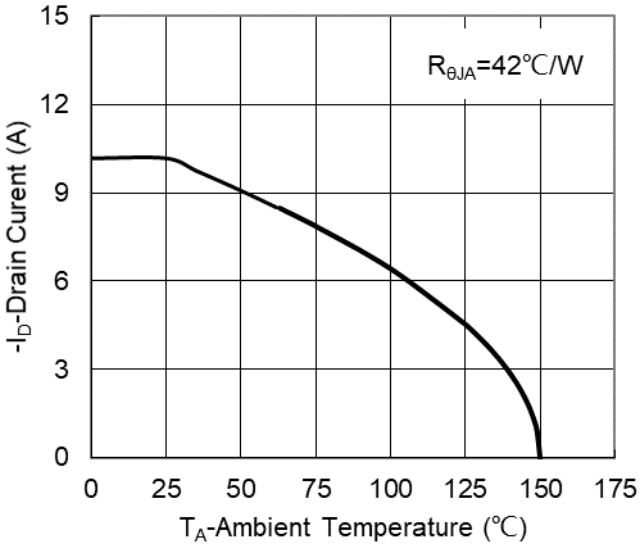



**Figure 8. Maximum Continuous Drain Current vs Ambient Temperature**

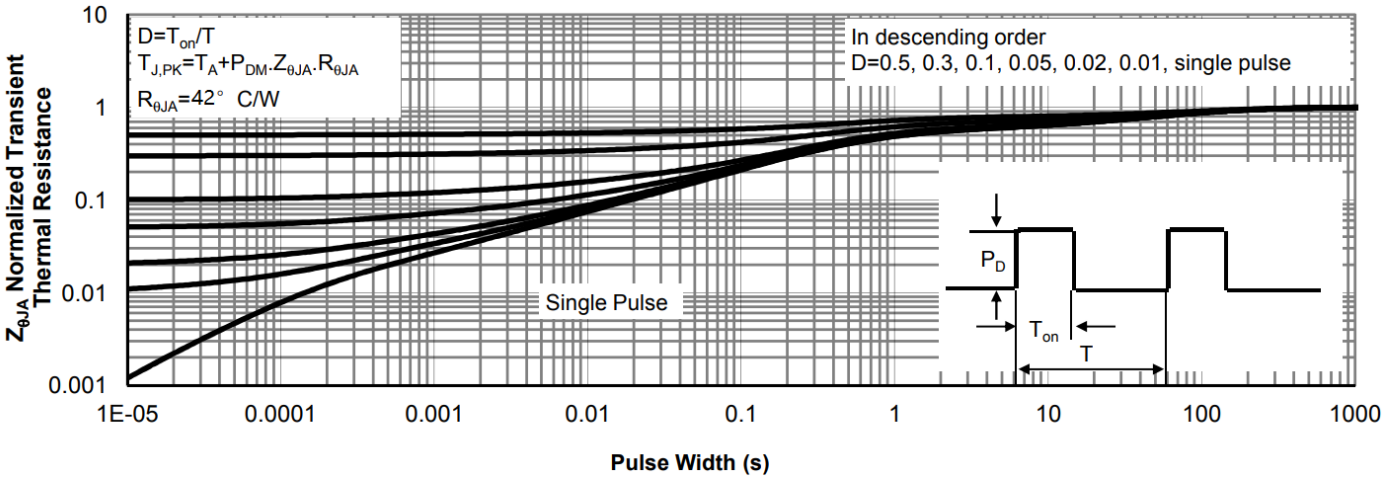
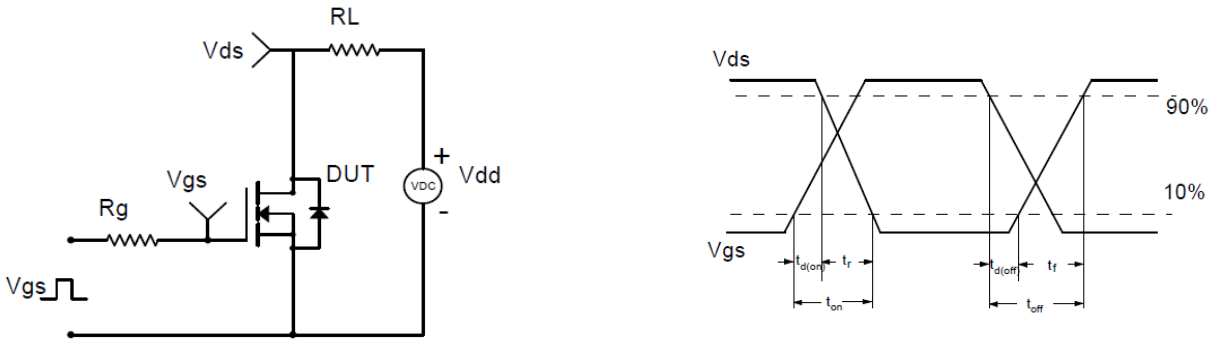
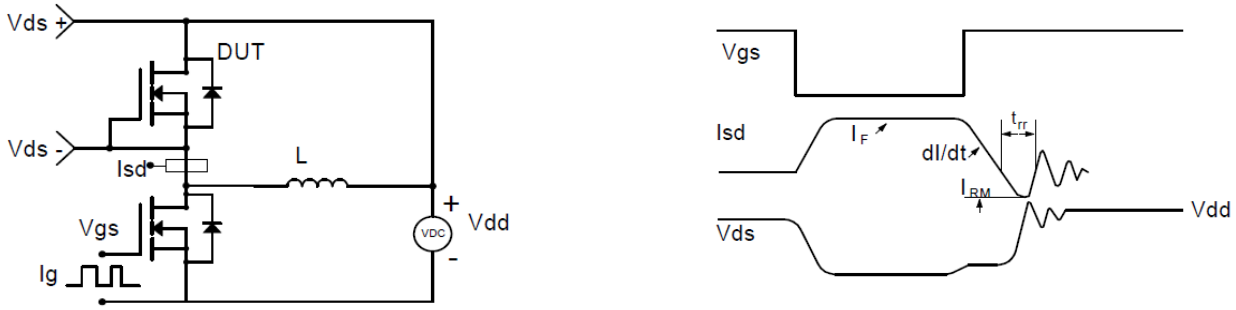


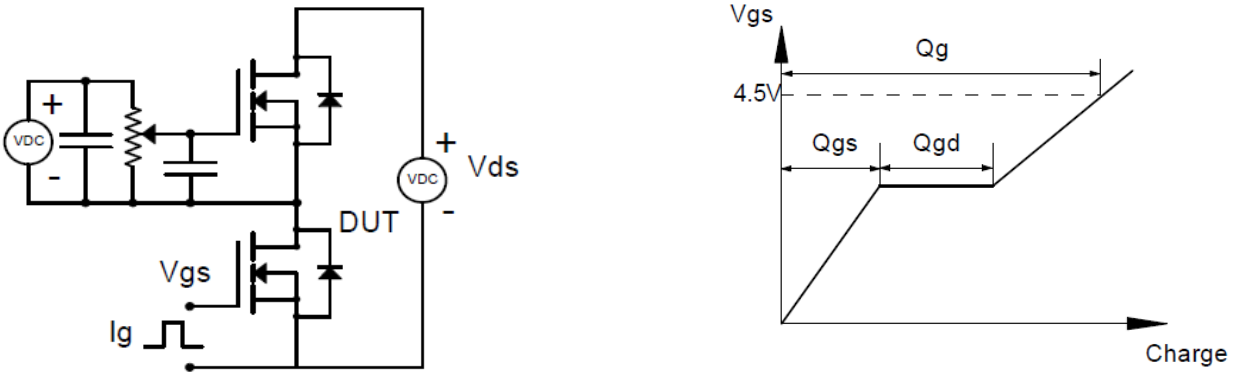

**Figure 9. Normalized Maximum Transient Thermal Impedance**



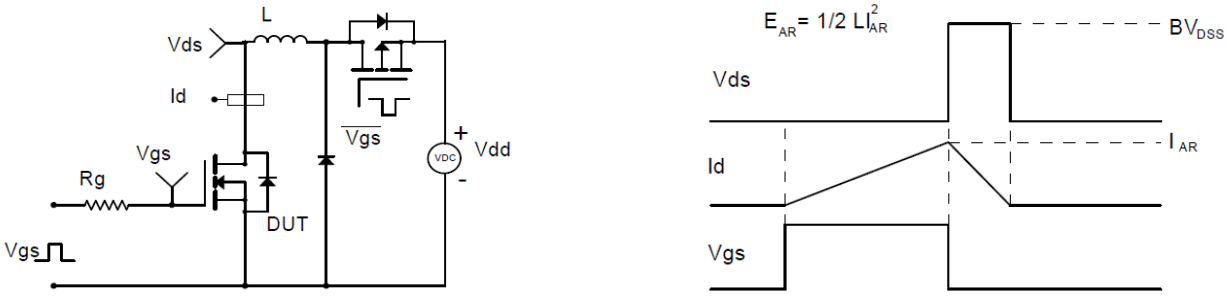

**Resistive Switching Test Circuit & Waveforms**




**Diode Recovery Test Circuit & Waveforms**

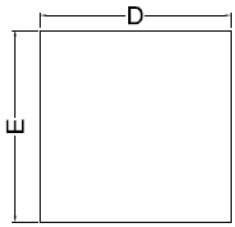



**Gate Charge Test Circuit & Waveform**

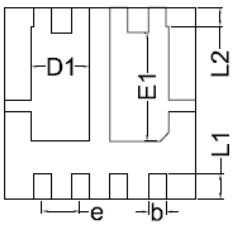



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**

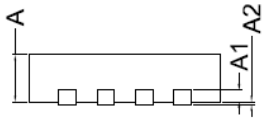
## ■DFN3.3X3.3 Package information




Top View
正面视图

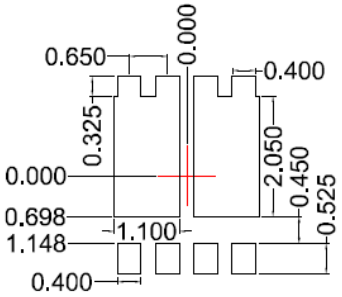



Bottom View
背面视图




Side View
侧面视图

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| D | 3.15 | 3.25 | 3.35 |
| E | 3.15 | 3.25 | 3.35 |
| A | 0.70 | 0.80 | 0.90 |
| A1 | | 0.20 BSC | |
| A2 | | | 0.10 |
| D1 | 0.90 | 1.00 | 1.10 |
| E1 | 1.75 | 1.85 | 1.95 |
| L1 | 0.325 | 0.425 | 0.525 |
| L2 | | 0.325 BSC | |
| b | 0.20 | 0.30 | 0.40 |
| e | | 0.65 BSC | |




Suggested Solder Pad Layout
Top View

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.10mm.
3.The pad layout is for reference purposes only.

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