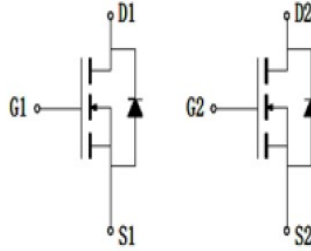
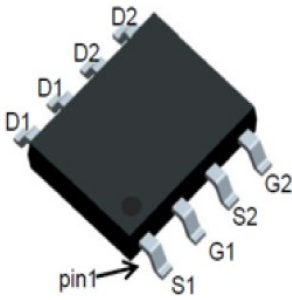


N-Channel Enhancement Mode Field Effect Transistor



Product Summary

- V_{DS} 30V
- I_D 8.5A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <21mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <35mohm
- 100% ∇V_{DS} Tested

General Description

- Trench Power LV MOSFET technology
- High density cell design for low $R_{DS(ON)}$
- High Speed switching

SOP-8

Applications

- Battery protection
- Load switch
- Power management

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ\text{C}$	I_D	8.5	A
	$T_A=70^\circ\text{C}$		6.8	
Pulsed Drain Current ^A		I_{DM}	34	A
Total Power Dissipation	$T_A=25^\circ\text{C}$	P_D	2.5	W
	$T_A=70^\circ\text{C}$		1.6	
Thermal Resistance Junction-to-Ambient ^B		$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJS3404A	F2	Q3404.	4000	8000	64000	13" reel



YJS3404A

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS1}	V _{GS} =±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1	1.5	2.2	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =8.5A		14	21	mΩ
		V _{GS} =4.5V, I _D =6A		23	35	
Diode Forward Voltage	V _{SD}	I _S =8.5A, V _{GS} =0V			1.2	V
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHZ		526		pF
Output Capacitance	C _{oss}			78		
Reverse Transfer Capacitance	C _{rss}			69		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =15V, I _D =5.6A		12.22		nC
Gate-Source Charge	Q _{gs}			2.37		
Gate-Drain Charge	Q _{gd}			2.31		
Reverse Recovery Charge	Q _{rr}	I _F =5.6A, di/dt=100A/us		1.28		ns
Reverse Recovery Time	t _{rr}			16.5		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DS} =15V, I _D =5.6A R _{GEN} =3Ω		5		ns
Turn-on Rise Time	t _r			28.2		
Turn-off Delay Time	t _{D(off)}			12.8		
Turn-off fall Time	t _f			21.6		

A. Pulse Test: Pulse Width ≤ 300us, Duty cycle ≤ 2%.

B. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

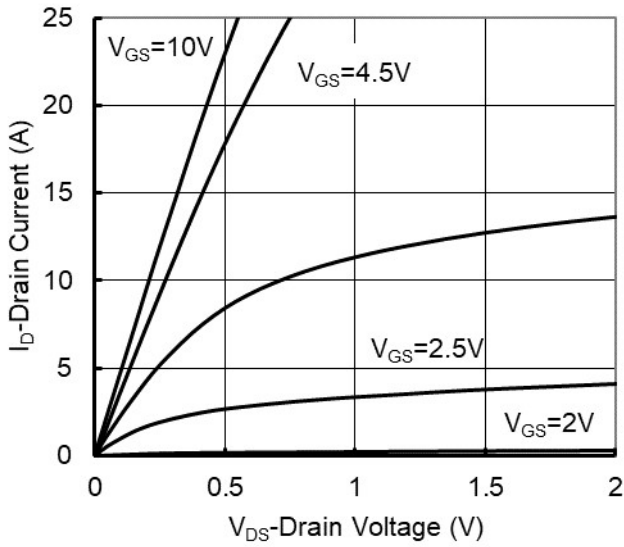


Figure1. Output Characteristics

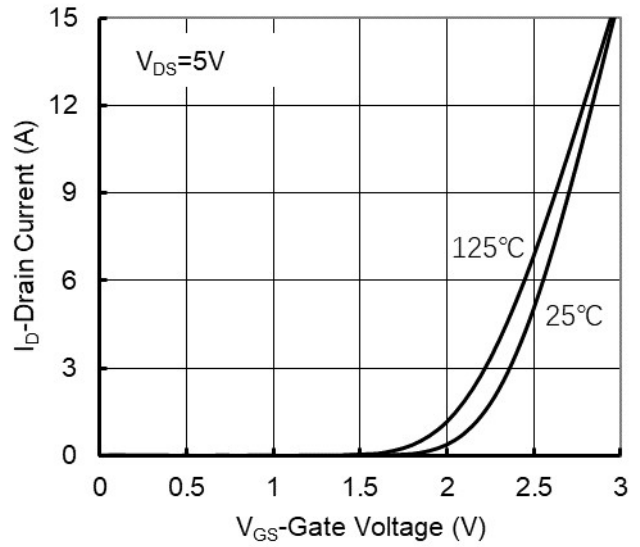


Figure2. Transfer Characteristics

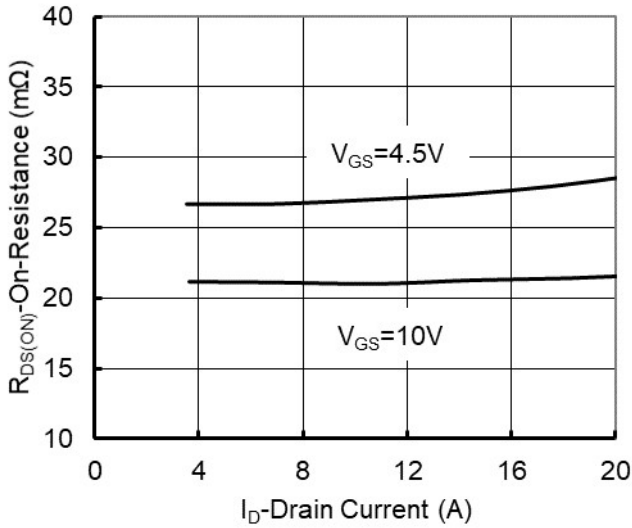


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

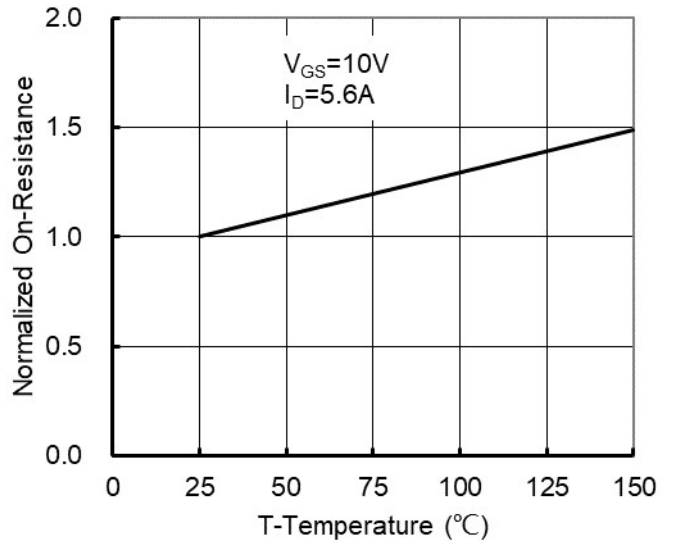


Figure 4: On-Resistance vs. Junction Temperature

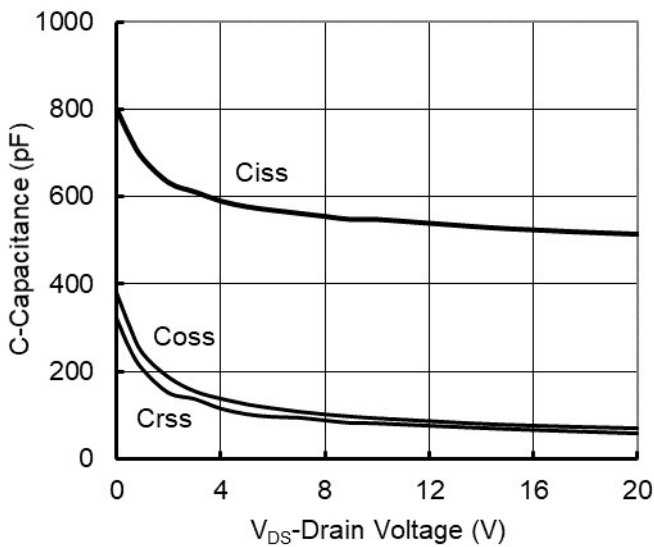


Figure5. Capacitance Characteristics

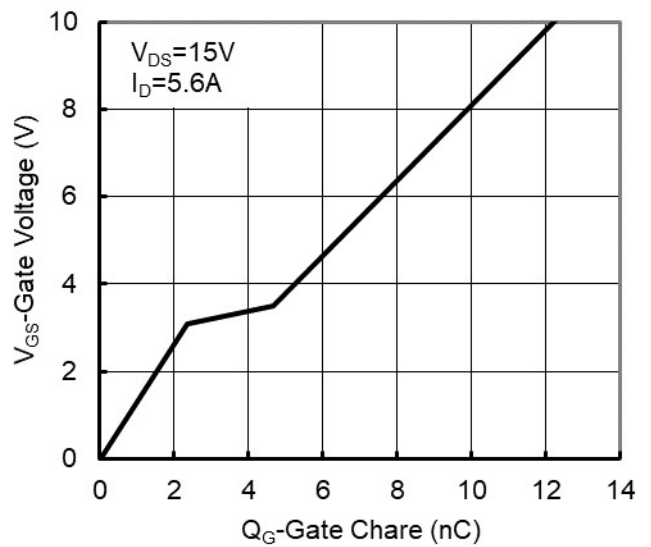


Figure6. Gate Charge

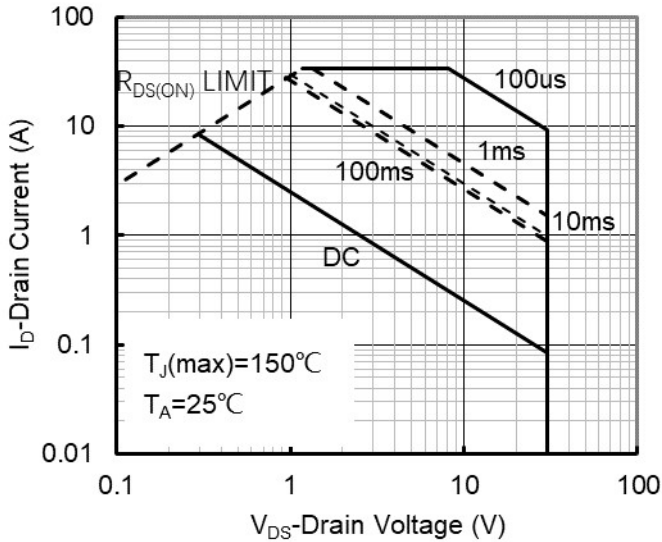


Figure7. Safe Operation Area

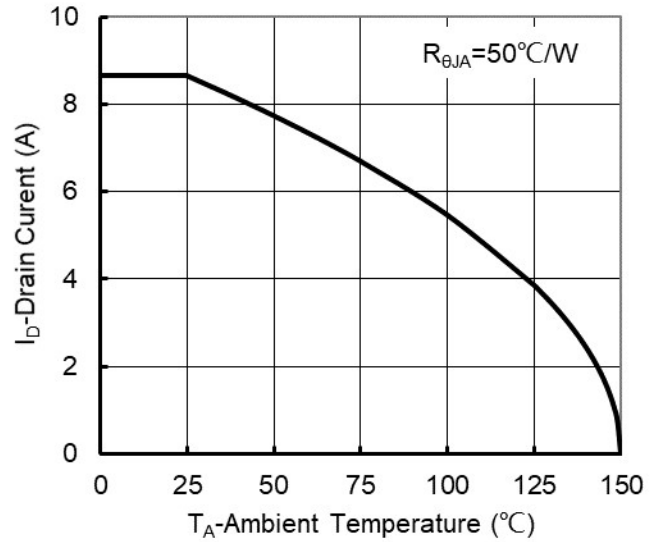


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

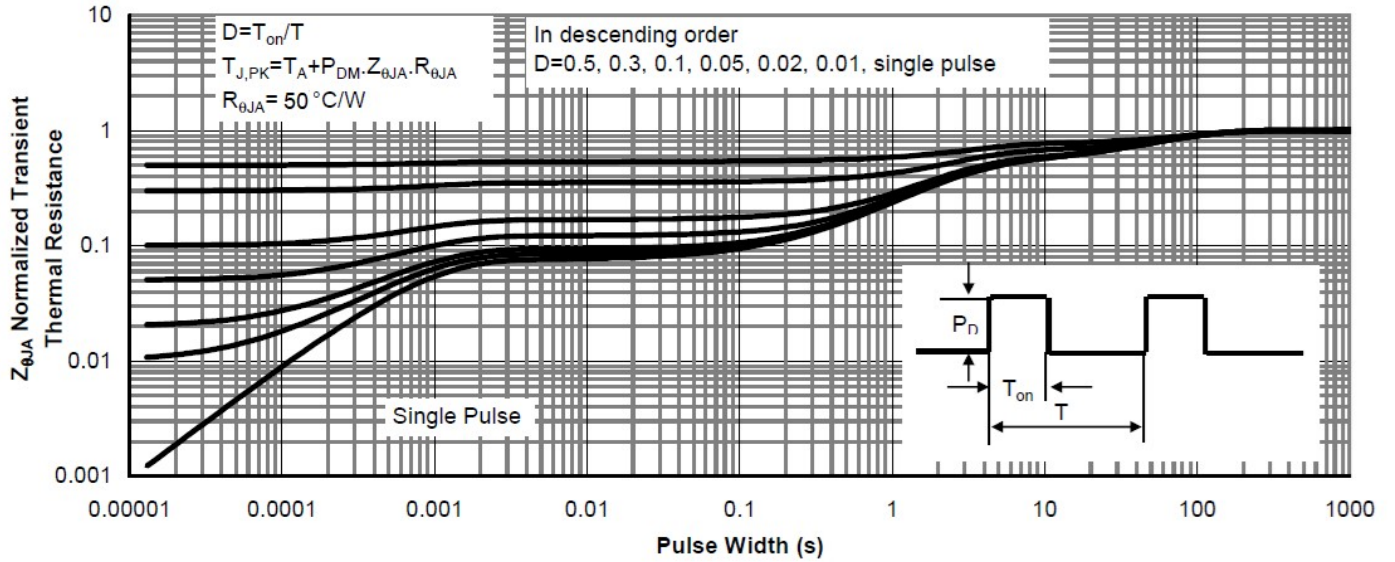
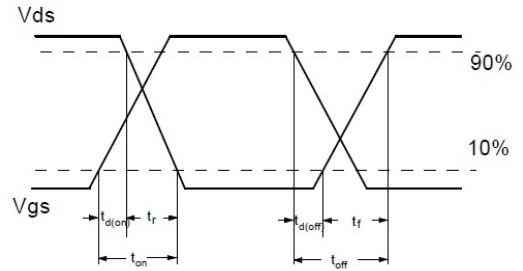


Figure9. Normalized Maximum Transient Thermal Impedance



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform

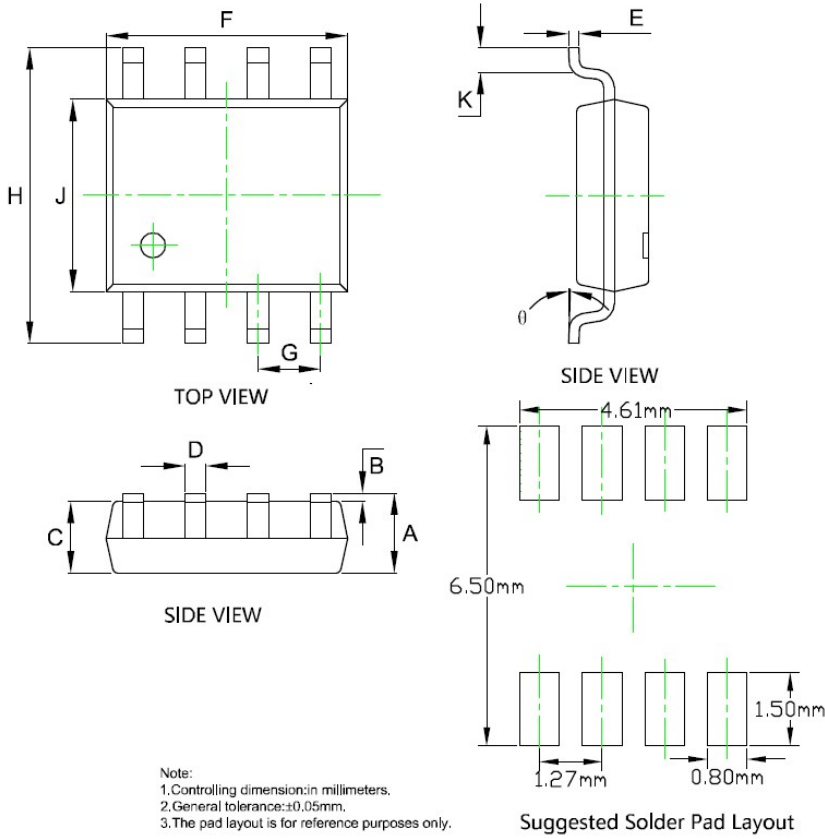


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



YJS3404A

■ SOP-8 Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.350	1.750
B	0.004	0.010	0.100	0.250
C	0.053	0.061	1.350	1.550
D	0.013	0.020	0.330	0.510
E	0.007	0.010	0.170	0.250
F	0.189	0.197	4.800	5.000
G	0.050BSC		1.270BSC	
H	0.228	0.244	5.800	6.200
J	0.150	0.157	3.800	4.000
K	0.016	0.050	0.400	1.270
θ	0°	8°	0°	8°



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