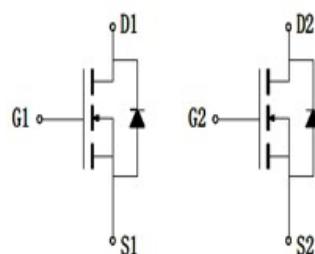
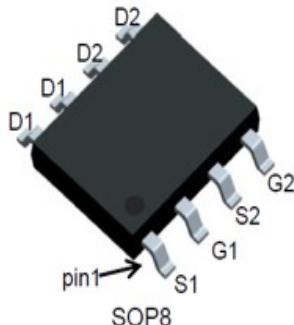




## N-Channel Enhancement Mode Field Effect Transistor



### Product Summary

- $V_{DS}$  30V
- $I_D$  12A
- $R_{DS(ON)}$  (at  $V_{GS}=10V$ ) <12 mohm
- $R_{DS(ON)}$  (at  $V_{GS}=4.5V$ ) <15 mohm

### General Description

- Trench Power LV MOSFET technology
- High density cell design for low  $R_{DS(ON)}$
- High Speed switching

**SOP-8**

### Applications

- Battery protection
- Load switch
- Power management

**■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$  unless otherwise noted)**

Parameter		Symbol	Limit	Unit
Drain-source Voltage		$V_{DS}$	30	V
Gate-source Voltage		$V_{GS}$	$\pm 20$	V
Drain Current	$T_A=25^\circ\text{C}$ @ Steady State	$I_D$	12	A
	$T_A=70^\circ\text{C}$ @ Steady State		9.6	
Pulsed Drain Current <sup>A</sup>		$I_{DM}$	50	A
Total Power Dissipation @ $T_A=25^\circ\text{C}$		$P_D$	2.5	W
Thermal Resistance Junction-to-Ambient @ Steady State <sup>B</sup>		$R_{\theta JA}$	50	$^\circ\text{C} / \text{W}$
Junction and Storage Temperature Range		$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

**■ Ordering Information (Example)**

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJSD12N03A	F2	Q12N03..	4000	8000	64000	13" reel



# YJSD12N03A

## ■ Electrical Characteristics ( $T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{\text{DSS}}$	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	30			V
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{DS}}=30\text{V}, V_{\text{GS}}=0\text{V}$			1	$\mu\text{A}$
Gate-Body Leakage Current	$I_{\text{GSS}}$	$V_{\text{GS}}= \pm 20\text{V}, V_{\text{DS}}=0\text{V}$			$\pm 100$	nA
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	1	1.5	2.5	V
Static Drain-Source On-Resistance	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=8.0\text{A}$		7	12	$\text{m}\Omega$
		$V_{\text{GS}}= 4.5\text{V}, I_{\text{D}}=6.0\text{A}$		11	15	
Diode Forward Voltage	$V_{\text{SD}}$	$I_{\text{S}}=12\text{A}, V_{\text{GS}}=0\text{V}$		0.85	1.2	V
Maximum Body-Diode Continuous Current	$I_{\text{S}}$				12	A
<b>Dynamic Parameters</b>						
Input Capacitance	$C_{\text{iss}}$	$V_{\text{DS}}=15\text{V}, V_{\text{GS}}=0\text{V}, f=1\text{MHz}$		1015		$\text{pF}$
Output Capacitance	$C_{\text{oss}}$			201		
Reverse Transfer Capacitance	$C_{\text{rss}}$			164		
<b>Switching Parameters</b>						
Total Gate Charge	$Q_{\text{g}}$	$V_{\text{GS}}=10\text{V}, V_{\text{DS}}=20\text{V}, I_{\text{D}}=20\text{A}$		23.6		$\text{nC}$
Gate Source Charge	$Q_{\text{gs}}$			3.9		
Gate Drain Charge	$Q_{\text{gd}}$			7.0		
Reverse Recovery Charge	$Q_{\text{rr}}$	$I_{\text{F}}=15\text{A}, dI/dt=100\text{A/us}$		0.2		$\text{ns}$
Reverse Recovery Time	$t_{\text{rr}}$			5		
Turn-on Delay Time	$t_{\text{D(on)}}$			7		
Turn-on Rise Time	$t_{\text{r}}$	$V_{\text{GS}}=10\text{V}, V_{\text{DD}}=20\text{V}, I_{\text{D}}=2\text{A}, R_{\text{GEN}}=3\Omega$		20		$\text{ns}$
Turn-off Delay Time	$t_{\text{D(off)}}$			24		
Turn-off Fall Time	$t_{\text{f}}$			24		

A. Pulse Test: Pulse Width  $\leq 300\text{us}$ , Duty cycle  $\leq 2\%$ .

B.  $R_{\theta JA}$  is the sum of the junction-to-lead and lead-to-ambient thermal resistance, where the lead thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta UL}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

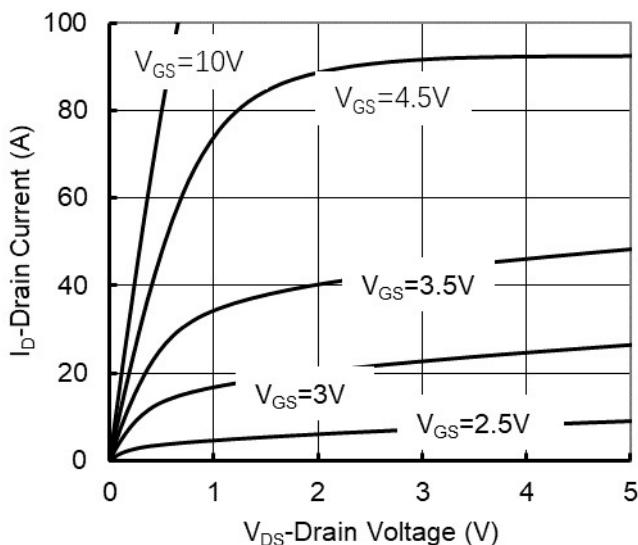
**■ Typical Performance Characteristics**

Figure 1. Output Characteristics

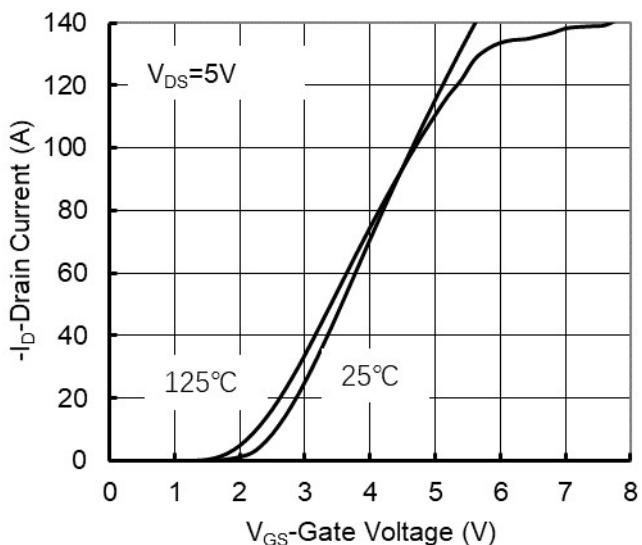


Figure 2. Transfer Characteristics

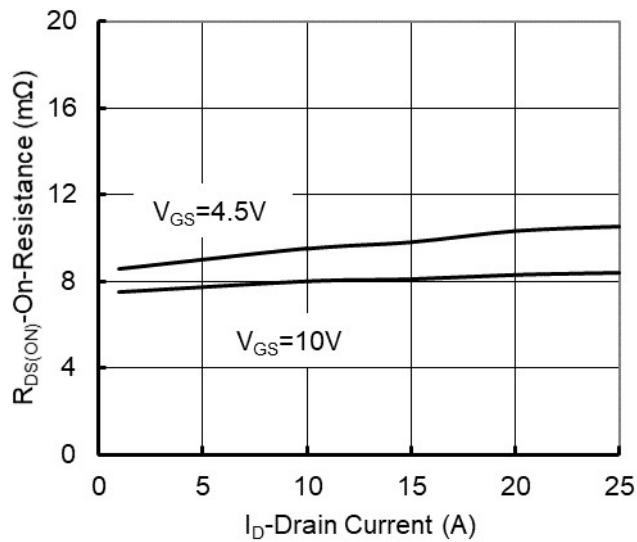


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

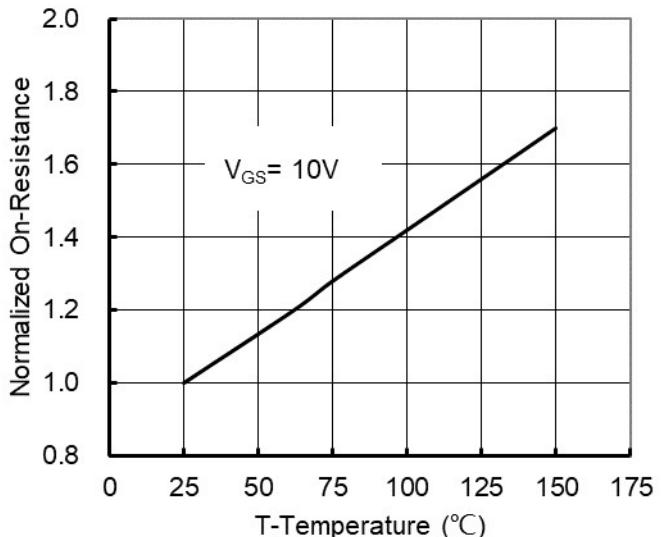


Figure 4: On-Resistance vs. Junction Temperature

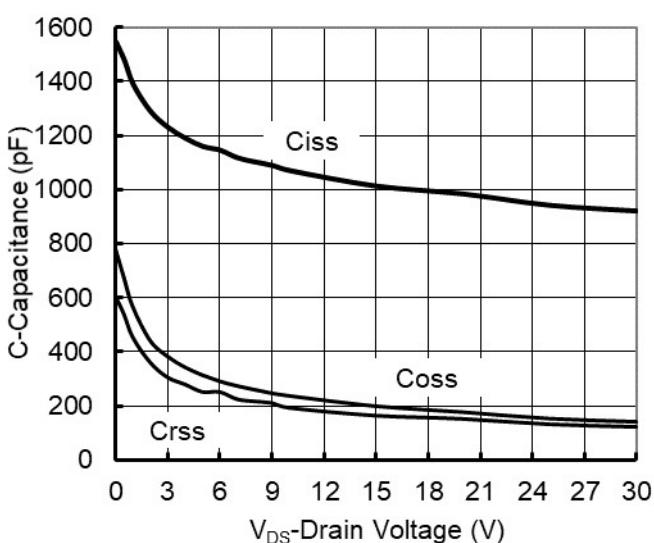


Figure 5. Capacitance Characteristics

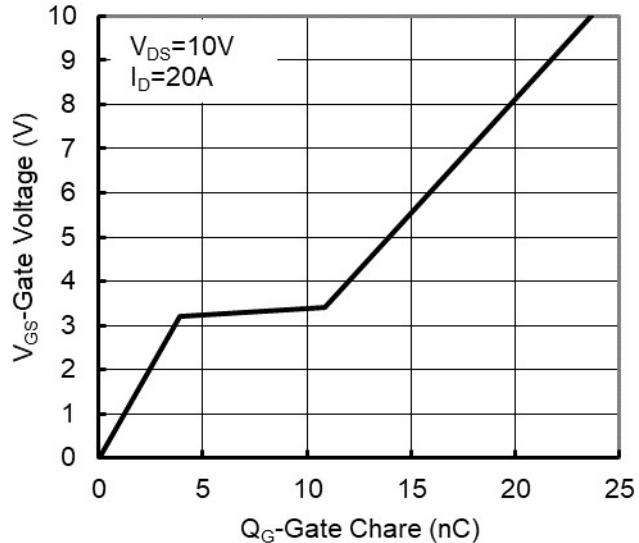
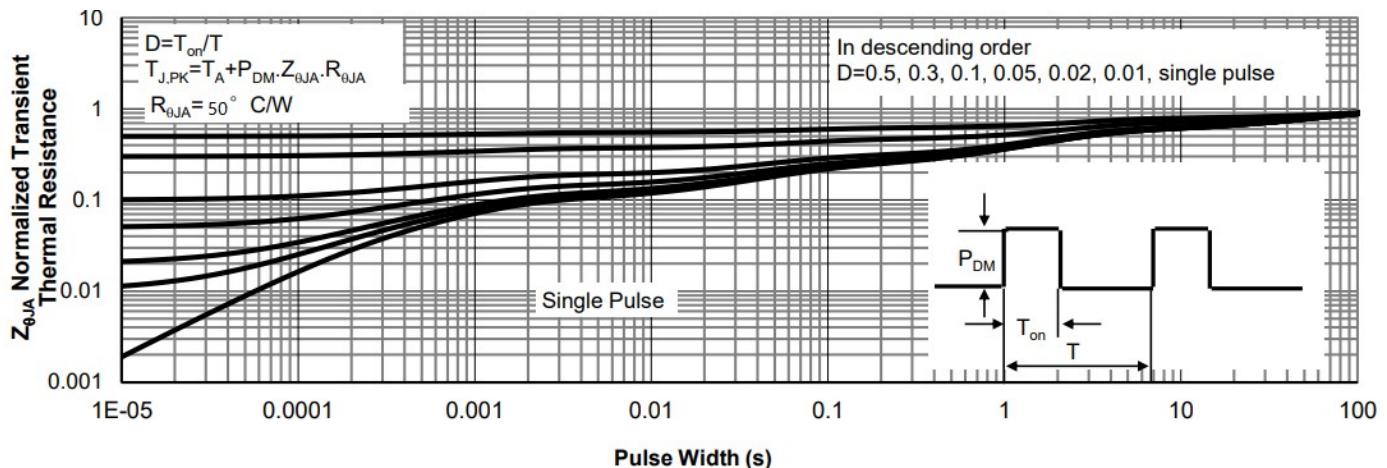
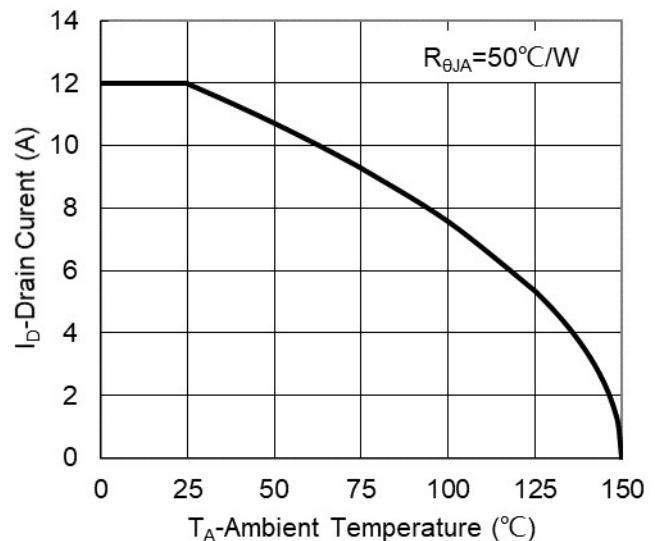
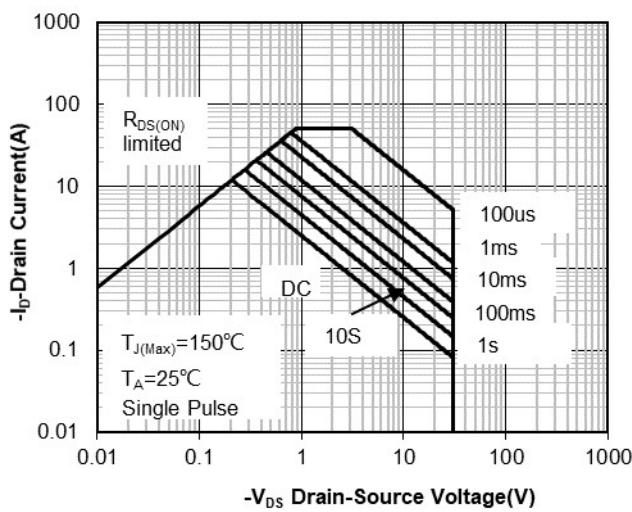
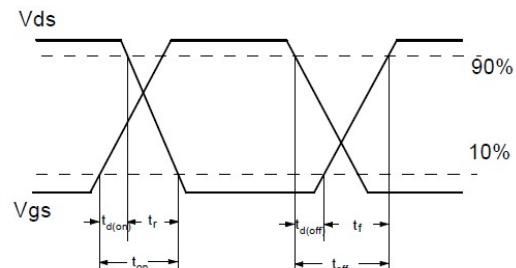
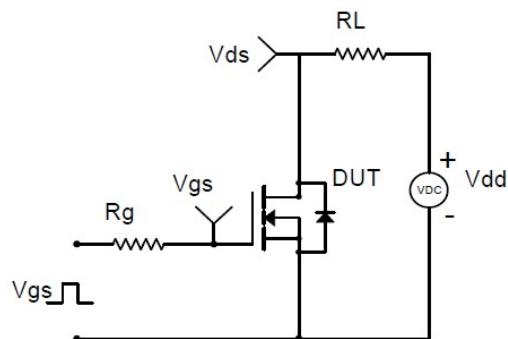
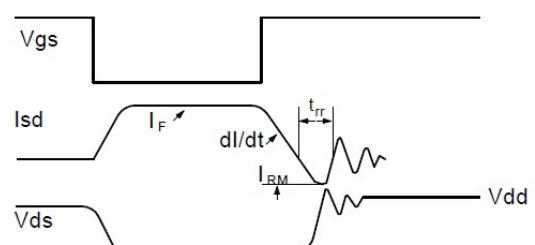
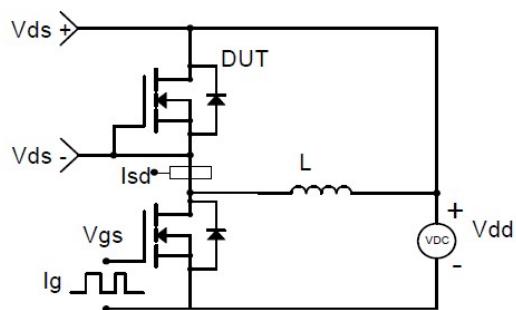


Figure 6. Gate Charge

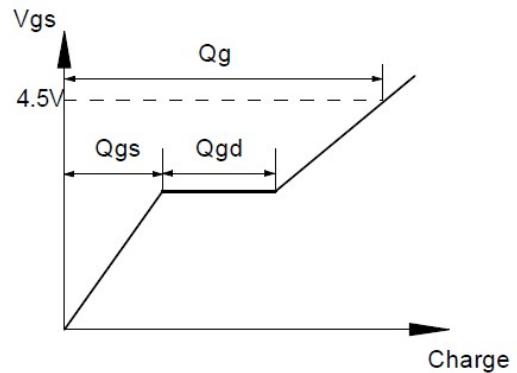
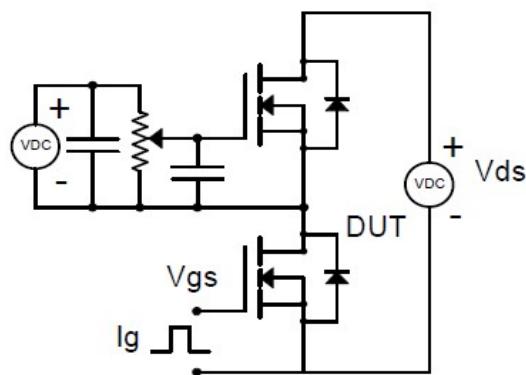




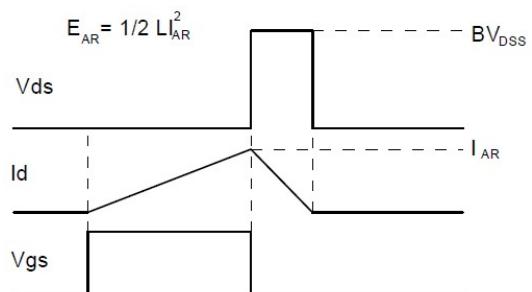
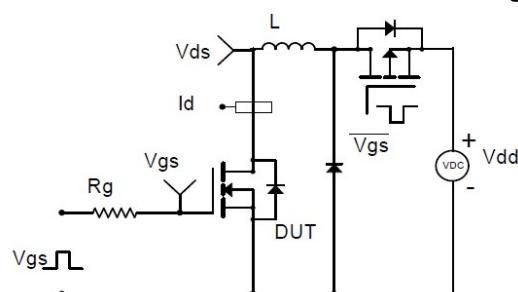
Resistive Switching Test Circuit &amp; Waveforms



Diode Recovery Test Circuit &amp; Waveforms



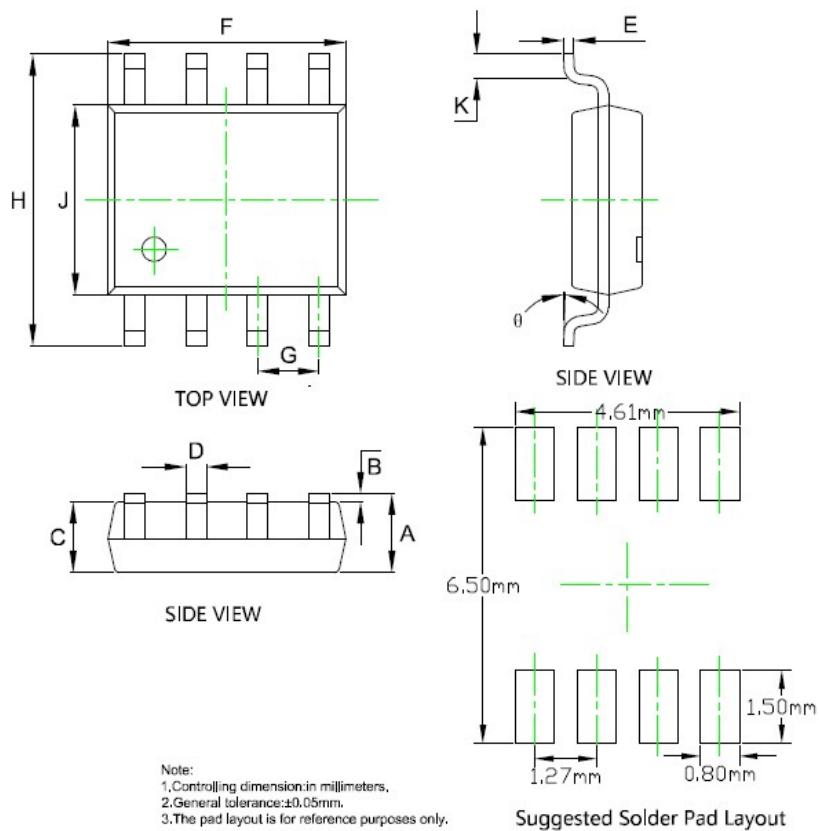
Gate Charge Test Circuit &amp; Waveform



Unclamped Inductive Switching (UIS) Test Circuit &amp; Waveforms



## ■ SOP-8 Package information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.053	0.069	1.350	1.750
B	0.004	0.010	0.100	0.250
C	0.053	0.061	1.350	1.550
D	0.013	0.020	0.330	0.510
E	0.007	0.010	0.170	0.250
F	0.189	0.197	4.800	5.000
G	0.050BSC		1.270BSC	
H	0.228	0.244	5.800	6.200
J	0.150	0.157	3.800	4.000
K	0.016	0.050	0.400	1.270
θ	0°	8°	0°	8°



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