

Differential Oscillator

YSO230LR



Applications

- 10 GB Ethernet,
SONET, SATA, SAS,
Fibre Channel

Features

- Freq range:13.5MHz-200MHz.
- Output LVPECL or LVDS.

- Package Size: 2.5*2.0, 3.2*2.5, 5.0*3.2
7.0*5.0mm.

Specifications

Item/Type	LVPECL		LVDS		Remarks		
	7050/5032	3225/2520	7050/5032	3225/2520			
Output Frequency Range	13.5~200MHZ	13.5~156.25MHZ	13.5~200MHZ	13.5~156.25MHZ			
Supply Voltage	2.5V~3.3V		1.8V, 2.5V~3.3V				
Operating Temperature Range	-40~+85°C, or specify						
Storage Temperature Range	-55~+125°C						
Total Stability	±50ppm						
Current Consumption	80mA Max	50mA Max	60mA Max	40mA Max	OE=Vcc, LVPECL=(50)Ω or LVDS=(100)Ω		
Disable Current	10uA Max				OE=GND		
Output Voltage (LVPECL)	VOH=Vcc-1.03 Min		--		DC characteristics		
	VOL=Vcc-1.6 Max		--				
Output Voltage (LVDS)	--		VOD= 247~454mV		VOD1, VOD2		
	--		dVOD=50mV Max.		dVOD= VOD1-VOD2		
	--		VOS= 1.125~1.375V		VOS1, VOS2		
	--		dVOS=50mV Max.		dVOS= VOD1-VOD2		
Output Load Condition	L_PECL=50Ω		--		Terminated to Vcc-2.0V		
	--		L_LVDS=100Ω		Connected between OUT to OUT		
Input Voltage	VIH=70% VccMin, VIL=30%Vcc Max				OE terminal		
Output Symmetry	45~55%						
Rise Time/Fall Time	0.8nS Max				LVPECL: Between 20% and 80% of (VOH-VOL), LVDS: Between 20% and 80% Differential Output peak to peak voltage		
Start-up time	10mS				Time at minimum supply voltage to be 0 s		
Aging	±3ppm				25°C First year, Vcc=2.5V, 3.3V		
Phase Jitter(12KHZ~20MHZ)	100MHZ	125MHZ	148.5MHZ	156.25MHZ	180MHZ	200MHZ	
	0.3ps Typ.		0.1ps Typ.				

Pin Dimension

Pin	#1	#2	#3	#4	#5	#6
FUNCTION	OE	NC	GND	OUT+	OUT-	VDD

Notes: To maintain stable operation provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc-GND).

Top View

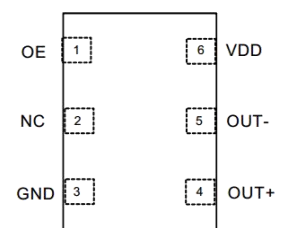


Figure 1. Pin Assignments

YSO230LR

Dimensions and Patterns [unit:mm]

Package Size – Dimensions (Unit: mm)	Recommended Land Pattern (Unit: mm)
<p>2.5*2.0mm</p>	
<p>3.2*2.5mm</p>	
<p>5.0*3.2mm</p>	
<p>7.0*5.0mm</p>	

Notes:

1.A capacitor of value 0.01uf~0.1uf or higher between Vdd and GND is required.

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Reflow Soldering Profile

Pre Heating Temperature $T_{p1} \sim T_{p2} = +170\text{ }^{\circ}\text{C}$

Heating Temperature

$T_{Mlt} = +220\text{ }^{\circ}\text{C}$

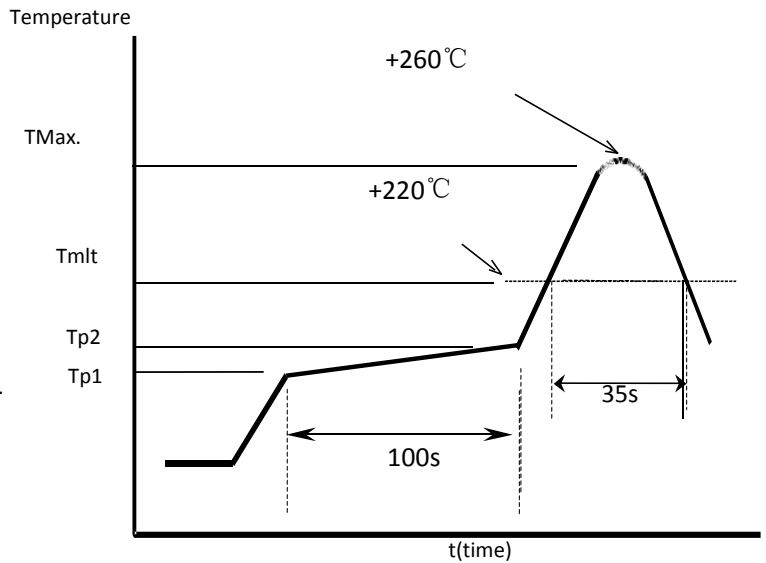
Peek Temperature

$T_{Max.} = +260\text{ }^{\circ}\text{C}$

Point of measuring

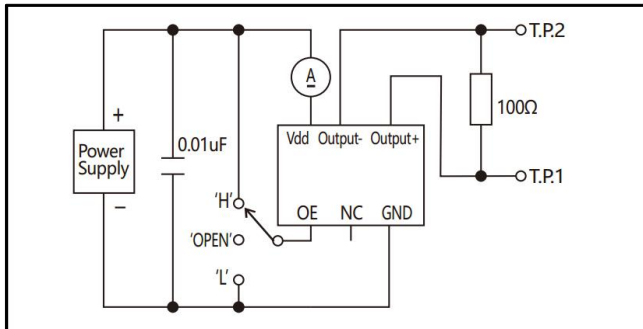
In case of Solder ability Terminal.

In case of Resistance to soldering heat Surface.

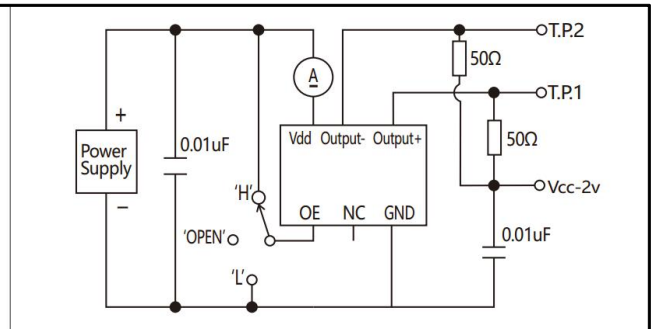


Test Circuit

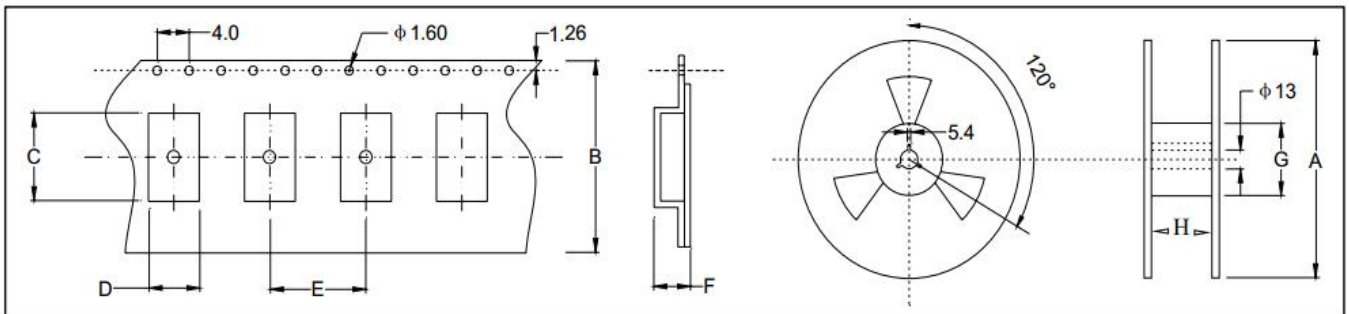
LVDS



LVPECL



Taping Specification(Unit: mm)



Size(OSC)	A	B	C	D	E	F	G	H
SMD-7050	180±2.0	16.0±0.3	7.50±0.1	5.50±0.1	8.0±0.1	2.00±0.1	61.0±1.0	16.0±1.0
SMD-5032	180±2.0	12.0±0.3	5.40±0.1	3.60±0.1	8.0±0.1	1.70±0.1	61.0±1.0	12.0±1.0
SMD-3225	180±2.0	8.0±0.3	3.40±0.1	2.70±0.1	4.0±0.1	1.50±0.1	61.0±1.0	8.0±1.0
SMD-2520	180±2.0	8.0±0.3	2.90±0.1	2.40±0.1	4.0±0.1	1.20±0.1	61.0±1.0	8.0±1.0

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