

# Differential Oscillator

## YSO230LR



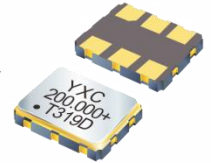
### Applications

- 10 GB Ethernet,  
SONET, SATA, SAS,  
Fibre Channel

### Features

- Frequency range: 13.5MHz-200MHz.  
- Output LVPECL, HCSL or LVDS.

- Package Size: 2.5\*2.0, 3.2\*2.5, 5.0\*3.2  
7.0\*5.0mm.



## Specifications (规格参数)

Item/Type	LVPECL		LVDS		HCSL		Remarks
	7050/5032	3225/2520	7050/5032	3225/2520	7050/5032	3225/2520	
Output Frequency Range	13.5~200MHZ	13.5~156.25 MHZ	13.5~200 MHZ	13.5~156.25 MHZ	13.5~200 MHZ	13.5~156.25 MHZ	
Supply Voltage	2.5V~3.3V		1.8V, 2.5V~3.3V		2.5V~3.3V		
Operating Temperature Range	-40~+85°C, or specify						
Storage Temperature Range	-55~+125°C						
Total Stability	±25ppm, ±50ppm, or specify						
Current Consumption	80mA Max	50mA Max	60mA Max	40mA Max	50mA Max		OE=Vdd, LVPECL=(50)Ω, HCSL=(50)Ω or LVDS=(100)Ω
Disable Current	10uA Max						OE=GND
Output Voltage (LVPECL)	VOH=Vdd-1.03 Min		--		--		DC characteristics
	VOL=Vdd-1.6 Max		--		--		
Output Voltage (LVDS)	--		VOD= 247~454mV		--		VOD1, VOD2
	--		dVOD=50mV Max.		--		dVOD= VOD1-VOD2
	--		VOS= 1.125~1.375V		--		VOS1, VOS2
Output Voltage (HCSL)	--		--		VOH= 0.9V Max		DC characteristics
	--		--		VOL= Vcc-0.15V Min		
	L_PECL=50Ω		--		--		
Output Load Condition	--		L_LVDS=100Ω		--		Connected between OUT to OUT
	--		--		L_HCSL=50Ω		--
	--		--		--		--
Input Voltage	VIH=70% VddMin, VIL=30%Vdd Max						OE terminal
Output Symmetry	45~55%						
Rise Time/Fall Time	0.8nS Max				0.7nS Max		LVPECL: Between 20% and 80% of (VOH-VOL), LVDS: Between 20% and 80% Differential Output peak to peak voltage
Start-up time	10mS						Time at minimum supply voltage to be 0 s
Aging	±3ppm						25°C First year, Vdd=2.5V, 3.3V
Phase Jitter(12KHZ~20MHZ)	100MHZ	125MHZ	148.5MHZ	156.25MHZ	180MHZ	200MHZ	
	0.3ps Typ.						0.1ps Typ.

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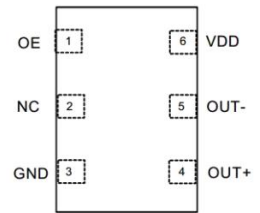
## YSO230LR



### Pin Dimension (脚位尺寸)

Pin	#1	#2	#3	#4	#5	#6
FUNCTION	OE	NC	GND	OUT+	OUT-	VDD

Top View



**Notes:** To maintain stable operation provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc-GND).

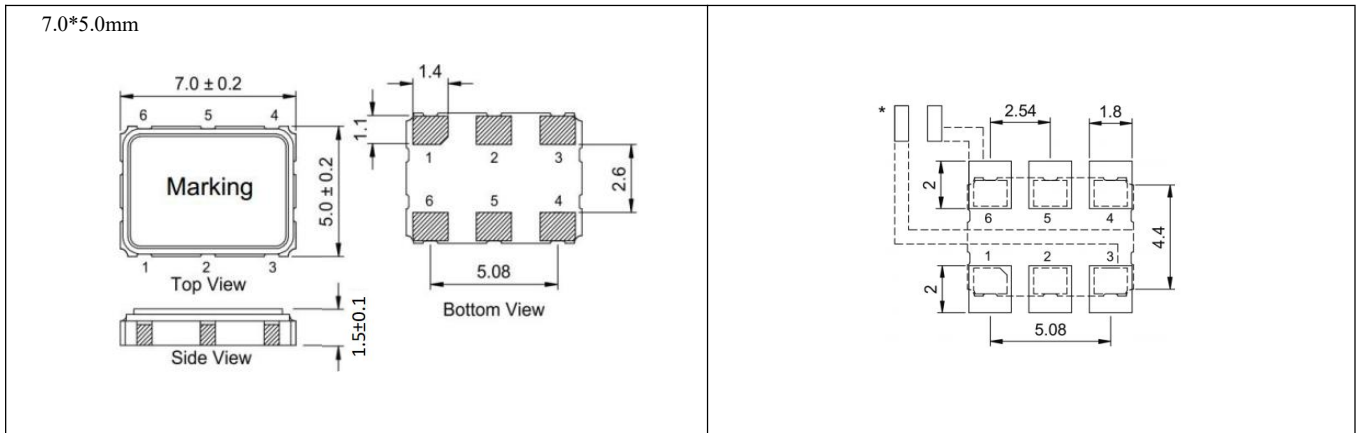
Figure 1. Pin Assignments

### Dimensions and Recommended land pattern (外观尺寸及推荐焊盘)

Package Size – Dimensions (Unit: mm)	Recommended Land Pattern (Unit: mm)
<p>2.5*2.0mm</p>	
<p>3.2*2.5mm</p>	
<p>5.0*3.2mm</p>	

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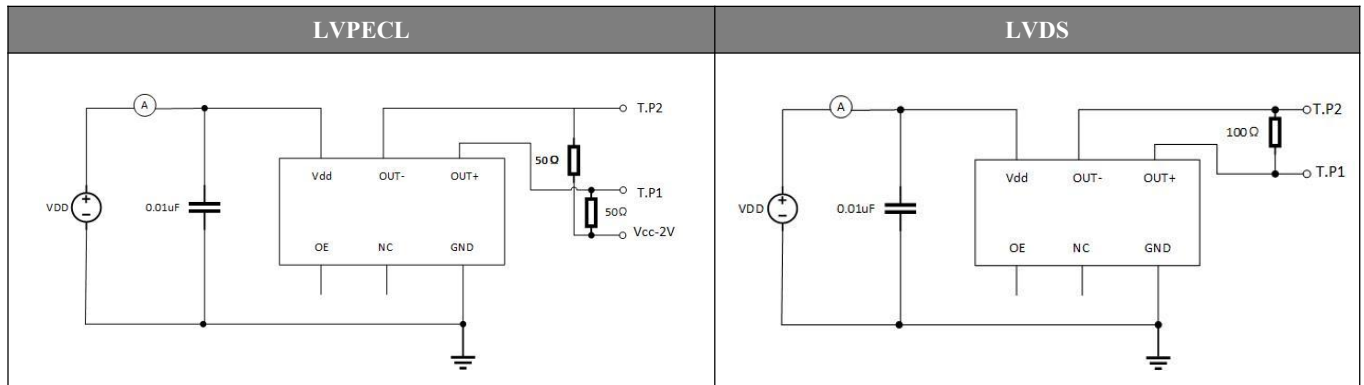
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**Notes:**

1.A capacitor of value 0.01uf~0.1uf or higher between Vdd and GND is required.

### Test Circuit (测试电路)



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