Temperature Compensated Crystal Oscillator

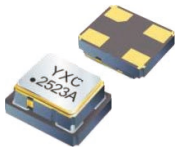
YSO510TP TCXO

Applications

- Networking
- Industrial

Features

- Frequency Stability as Tight as ± 1.0 ppm Over -40°C to 85°C
- Ultra Small SMD Seam Sealed Crystal Oscillator
- Package Size : 2.0*1.6, 2.5*2.0, 3.2*2.5, 5.0*3.2, 7.0*5.0mm



Specifications（规格参数）

Item/Type			Clipped Sine Wave or CMOS				
Package Size 封装尺寸			2.0 x 1.6	2.5 x 2.0	3.2 x 2.5	5.0 x 3.2	7.0 x 5.0
Frequency Range 额定频率范围			26 ~ 52MHz	13 ~ 52MHz	13 ~ 52MHz	6.4 ~ 52MHz	6.4 ~ 52MHz
Supply Voltage 电源电压			1.8V, 2.5V, 3V, 3.3V				
Operating Temperature Range 工作温度			-30 ~ +85°C, or specify				
Storage Temperature Range 储存温度			-40°C to +85°C				
Output Type 输出方式			Clipped Sine wave or CMOS				
Current Consumption (max.) 消耗电流			10~15MHz: 1.5mA ; 15.1~26MHz: 2mA ; 26.1~52MHz: 3.5mA				
Duty Cycle 占空比			45~55%				
Output Voltage Level (peak to peak) 峰峰值			0.8 Vp-p (min.) (CMOS)				
Start-up Time 启动时间			2.0msec(typ.), 5.0msec(max.) (reach 90% amplitude and at +25°C ± 2°C)				
Initial Calibration Tolerance 初始校准公差			±2.0 ppm (max.) at +25°C±2°C (at the shipment)				
Output Load 输出负载			10KΩ // 10pF ± 10% or 15pF				
Frequency Stability 频率偏差	vs Aging at Ta = +25°C		± 1.0 ppm / year (max.)				
	vs Voltage Change		± 0.2 ppm (max.) , for a ±5% input voltage change				
	vs Load Change		± 0.2 ppm (max.) , for a ±10% load condition change				
	vs Reflow		± 2.5 ppm (max.)				
	vs Temperature Change		±0.28ppm / ±0.5ppm / ±1.5ppm / ±2.5ppm				
Phase Noise [dBc / Hz ; (typ.)] 相位噪声	Offset	10 Hz	100 Hz	1 KHz	10 KHz	10 KHz	
	13.0 MHz	-80 (max)	-115	-135	-148	-148(min)	

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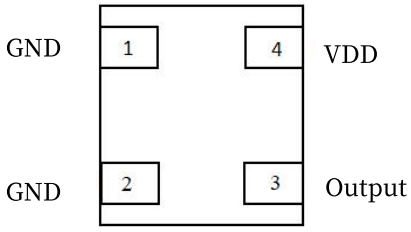
Pin Dimension（脚位尺寸）

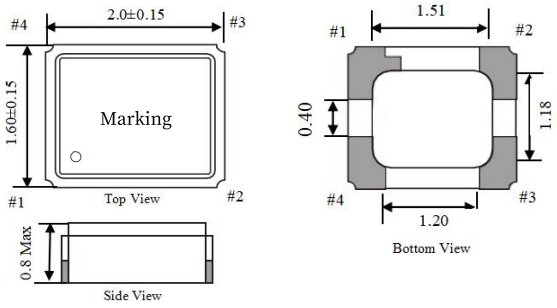
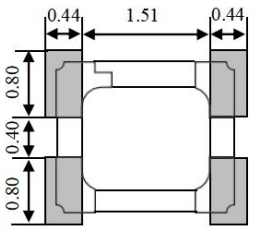
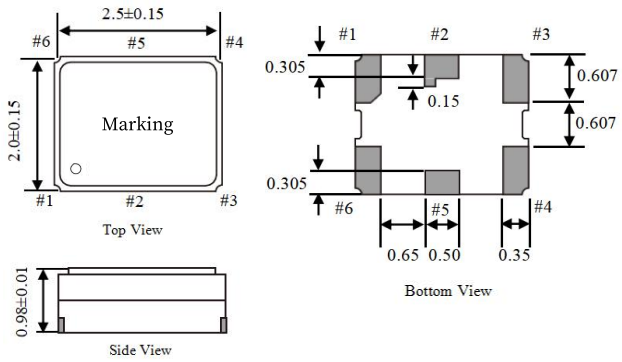
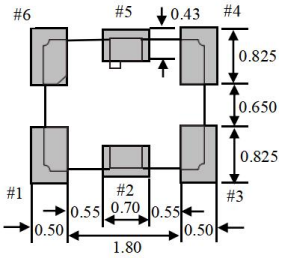
Pin	#1	#2	#3	#4
Function	Ground	Ground	Output	Supply Voltage

Pin Assignments



Top View

Dimensions and Recommended Land Pattern（外观尺寸及推荐焊盘）

Dimensions (Unit: mm)	Recommended Land Pattern (Unit: mm)
2.0*1.6mm 	
2.5*2.0mm 	 Pad Connections： Pad 2、Pad 5 : N.C

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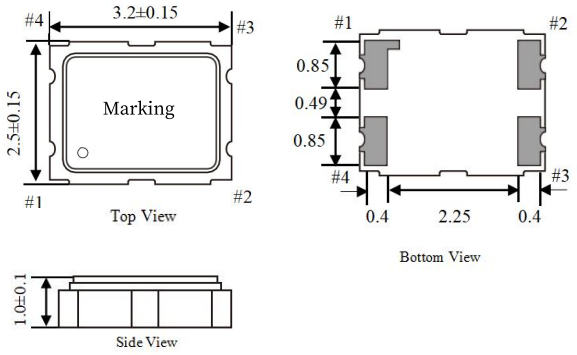
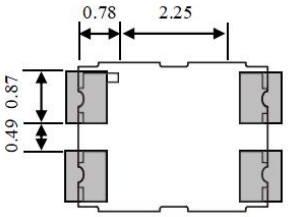
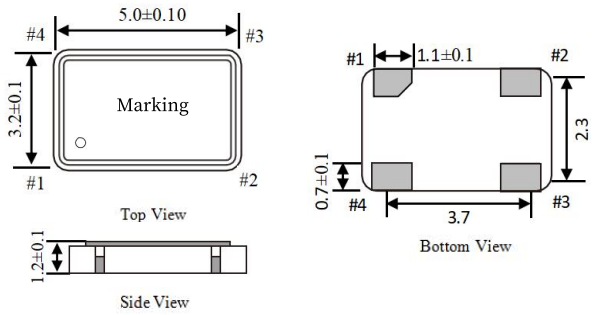
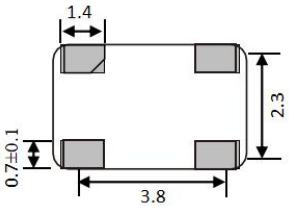
3.2*2.5mm



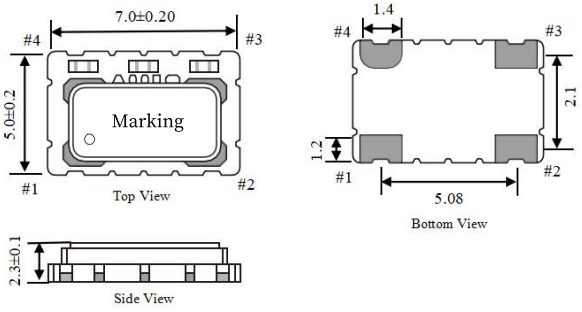


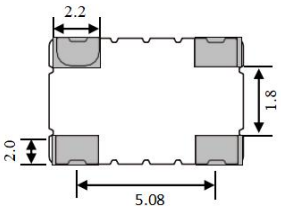
5.0*3.2mm





7.0*5.0mm





Notes:

1.A capacitor of value 0.01uf~0.1uf or higher between Vdd and GND is required.

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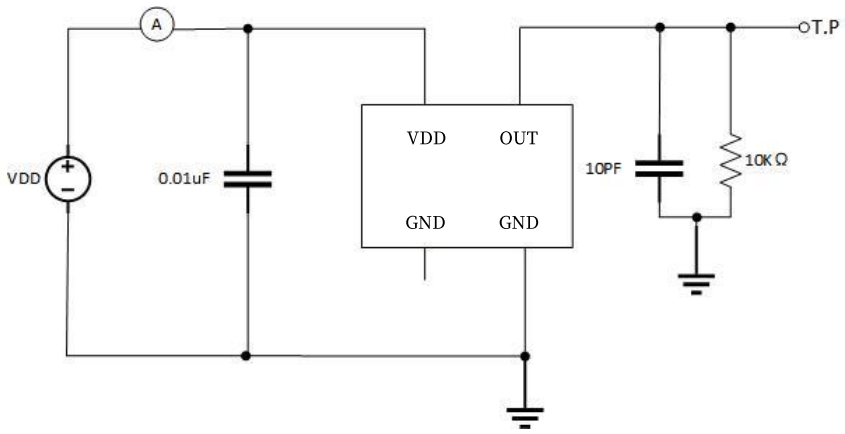
Test Circuit（测试电路）

CMOS


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