

Single Channel, High Speed 1MBit/s Transistor Optocoupler

Description

The UMW6N135/6N136 optocoupler consists of an 850nm AlGaAs LED optically coupled to a high speed photodetector transistor. A separate connection for the bias of the photodiode improves the speed by several orders of magnitude over conventional phototransistor optocouplers by reducing the base-collector capacitance of the input transistor. The devices are packaged in an 8-pin DIP package and available in wide-lead spacing (M-type) and SMD option.

Features

- Open-Collector Output
- TTL Compatible
- High bit rate: 1 MBit/s
- Superior CMR-10 kV/μs
- CTR guaranteed: 0-70°C
- RoHS compliant

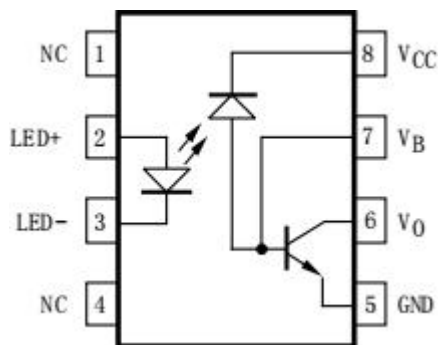
Applications

- Output interface to CMOS-LSTTL-TTL
- Telecommunication equipment
- Power transistor isolation in motor drives
- Replacement for low speed phototransistor photo couplers
- Home appliance WXW

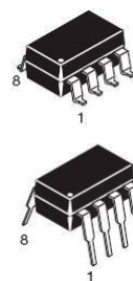
Truth Table (Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H	NC	L
L	NC	H

Schematics



Package Outlines



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Absolute Maximum Ratings (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Value	Units
Storage temperature	T _{STG}	-55 to +125	°C
Operating temperature	T _{OPR}	-55 to +100	°C
Lead solder temperature	T _{SOL}	260 for 10 sec	°C
Emitter			
DC/Average forward input current (Note 1)	I _{F (avg)}	25	mA
Peak forward input current (50% duty cycle, 1 ms p.w.) (Note 2)	I _{F (pk)}	50	mA
Peak transient input current (≤1 μs p.w., 300 pps)	I _{F (trans)}	1	A
Reverse input voltage	V _R	5	V
Input power dissipation (Note 3)	P _{D (i)}	100	mW
Detector			
Average output current	I _{O (avg)}	8	mA
Peak output current	I _{O (pk)}	16	mA
Emitter-base reverse voltage	V _{EBR}	5	V
Supply voltage	V _{CC}	-0.5 to 30	V
Output voltage	V _O	-0.5 to 20	V
Base current	I _B	5	mA
Output power dissipation (Note 4)	P _{D (o)}	100	mW

Notes

1. Derate linearly above 70°C free -air temperature at a rate of 0.8 mA/°C.
2. Derate linearly above 70°C free -air temperature at a rate of 1.6 mA/°C.
3. Derate linearly above 70°C free -air temperature at a rate of 0.9 mW/°C.
4. Derate linearly above 70°C free -air temperature at a rate of 2.0 mW/°C.

Electro-optical Characteristics (T_A = 0 to 70°C unless otherwise specified)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Emitter						
Input forward voltage	(I _F =16mA, T _A =25°C)	V _F		1.45	1.7	V
	(I _F =16mA)				1.8	
Input reverse breakdown voltage	(I _R =10μA)	BV _R	5			V
Temperature coefficient of forward voltage	(I _F =16mA)	(ΔV _F /ΔT _A)		-1.6		mV/°C
Detector						
Logic high output current	(I _F =0mA, V _O =V _{CC} =5.5V) (T _A =25°C)	IOH		0.001	0.5	μA
	(I _F =0mA, V _O =V _{CC} =15V) (T _A =25°C)			0.005	1	
	(I _F =0mA, V _O =V _{CC} =15V)				50	

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Logic low supply current		($I_F=16\text{mA}$, $V_O=\text{Open}$) ($V_{CC}=15\text{V}$)	ICCL		120	200	μA
Logic high supply current		($I_F=0\text{mA}$, $V_O=\text{Open}$, $V_{CC}=15\text{V}$) ($T_A=25^\circ\text{C}$)	ICCH			1	μA
		($I_F=0\text{mA}$, $V_O=\text{Open}$) ($V_{CC}=15\text{V}$)				2	
Coupled							
Current transfer ratio (Note 1)	WXW6N135	($I_F=16\text{mA}$, $V_{CC}=4.5\text{V}$) ($V_O=0.4\text{V}$), ($T_A=25^\circ\text{C}$)	CTR	7	18	50	%
		($I_F=16\text{mA}$, $V_{CC}=4.5\text{V}$) ($V_O=0.5\text{V}$)		5	19		
	WXW6N136	($I_F=16\text{mA}$, $V_{CC}=4.5\text{V}$) ($V_O=0.4\text{V}$), ($T_A=25^\circ\text{C}$)		19	24	50	
		($I_F=16\text{mA}$, $V_{CC}=4.5\text{V}$) ($V_O=0.5\text{V}$)		15	25		
Logic low output voltage output voltage	WXW6N135	($I_F=16\text{mA}$, $V_{CC}=4.5\text{V}$) ($I_O=1.1\text{mA}$, $T_A=25^\circ\text{C}$)	VOL		0.18	0.4	V
		($I_F=16\text{mA}$, $V_{CC}=4.5\text{V}$) ($I_O=0.8\text{mA}$)				0.5	
	WXW6N136	($I_F=16\text{mA}$, $V_{CC}=4.5\text{V}$) ($I_O=3.0\text{mA}$, $T_A=25^\circ\text{C}$)			0.1	0.4	
		($I_F=16\text{mA}$, $V_{CC}=4.5\text{V}$) ($I_O=2.4\text{mA}$)			0.1	0.5	
Switching ($V_{CC} = 5\text{V}$)							
Propagation delay time to logic low	WXW6N135	$T_A=25^\circ\text{C}$, ($R_L=4.1\text{k}\Omega$, $I_F=16\text{mA}$) (Note 2)	TPHL		0.45	1.5	μs
		($R_L=4.1\text{k}\Omega$, $I_F=16\text{mA}$) (Note 3)				2	
	WXW6N136	$T_A=25^\circ\text{C}$, ($R_L=1.9\text{k}\Omega$, $I_F=16\text{mA}$) (Note 2)			0.2	0.8	
		($R_L=1.9\text{k}\Omega$, $I_F=16\text{mA}$) (Note 3)				1	
Propagation delay time to logic high	WXW6N135	$T_A=25^\circ\text{C}$, ($R_L=4.1\text{k}\Omega$, $I_F=16\text{mA}$) (Note 2)	TPLH		0.5	1.5	μs
		($R_L=4.1\text{k}\Omega$, $I_F=16\text{mA}$) (Note 3)				2	
	WXW6N136	$T_A=25^\circ\text{C}$, ($R_L=4.1\text{k}\Omega$, $I_F=16\text{mA}$) (Note 2)			0.6	0.8	
		($R_L=4.1\text{k}\Omega$, $I_F=16\text{mA}$) (Note 3)				1	
Common mode transient immunity at logic high	WXW6N135	($I_F=0\text{mA}$, $V_{CM}=10\text{V}_{P-P}$, $R_L=4.1\text{k}\Omega$) (Note 4) $T_A=25^\circ\text{C}$	CMH		10,000		V/ μs
	WXW6N136	($I_F=0\text{mA}$, $V_{CM}=10\text{V}_{P-P}$, $R_L=1.9\text{k}\Omega$) (Note 4) $T_A=25^\circ\text{C}$			10,000		
Common mode transient immunity at logic low	WXW6N135	($I_F=16\text{mA}$, $V_{CM}=10\text{V}_{P-P}$, $R_L=4.1\text{k}\Omega$) (Note 4) $T_A=25^\circ\text{C}$	CML		10,000		V/ μs
	WXW6N136	($I_F=0\text{mA}$, $V_{CM}=10\text{V}_{P-P}$, $R_L=1.9\text{k}\Omega$) (Note 4) $T_A=25^\circ\text{C}$			10,000		
Isolation							
Input-output insulation leakage current		(Relative humidity=45%) ($T_A=25^\circ\text{C}$, $t=5\text{s}$) (V_{I-O} $=3000\text{VDC}$) (Note 5)	II-O			1	μA
Withstand insulation test voltage		($RH\leq 50\%$, $T_A=25^\circ\text{C}$) (Note 5) ($t=1\text{min.}$)	VISO	5000			VRMS
Resistance (input to output)		(Note 5) ($V_{I-O}=500\text{VDC}$)	RI-O		1012		W

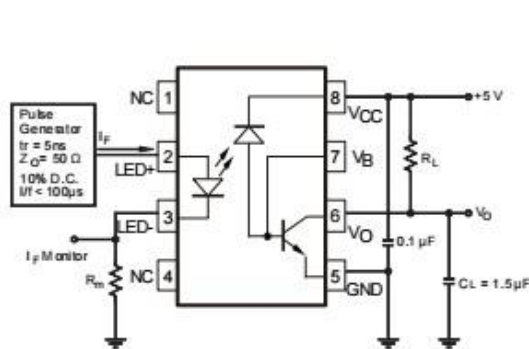
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Capacitance (input to output)	(Note 5) (f=1MHz)	CI-O	0.6		pF
DC Current gain	(I _O =3mA, V _O =5V)	HFE	150		

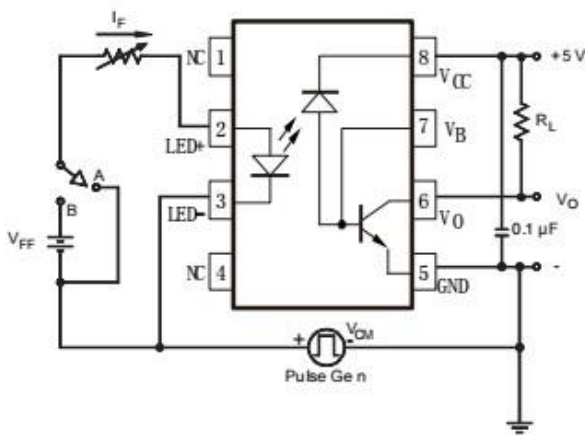
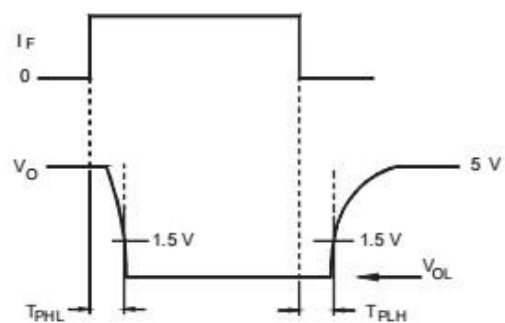
Notes

1. Current Transfer Ratio is defined as a ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
2. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1kΩ pull-up resistor.
3. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and 5.6 kΩ pull-up resistor.
4. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal V_{CM}, to assure that the output will remain in a logic high state (i.e., V_O>2.0 V). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic low state (i.e., V_O<0.8 V).
5. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.

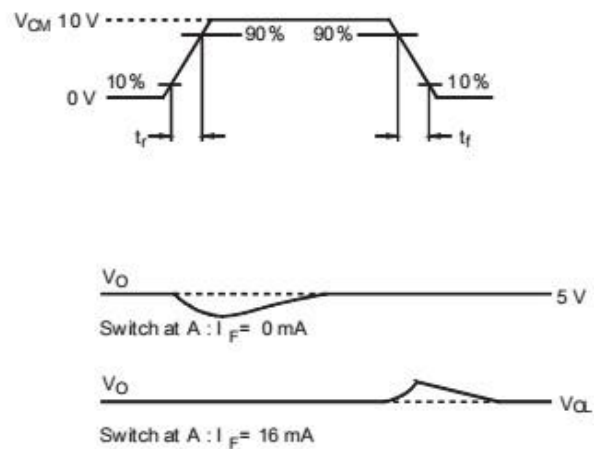
Test Circuits



Switching Time Test Circuit



Common Mode Immunity Test Circuit



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Typical Performance Curves

Fig. 1 Normalized CTR vs. Forward Current

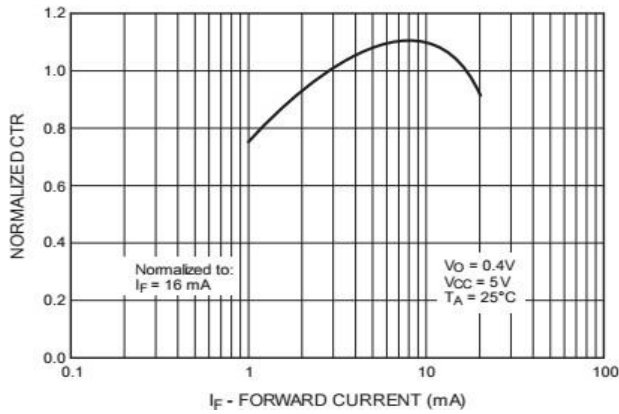


Fig. 2 Normalized CTR vs. Temperature

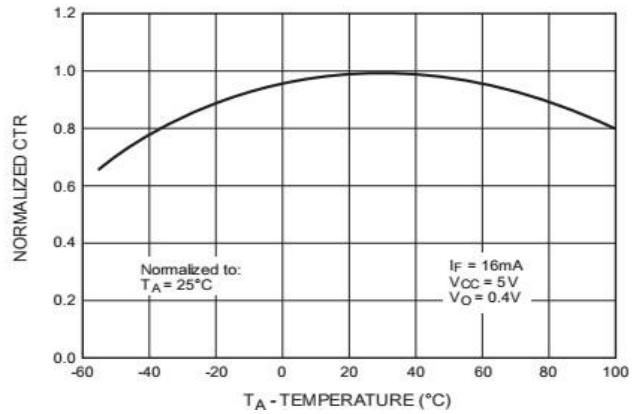


Fig. 3 Output Current vs. Output Voltage

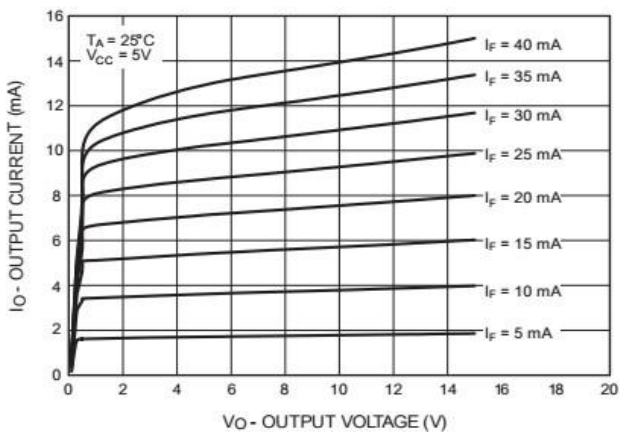


Fig. 4 Logic High Output Current vs. Temperature

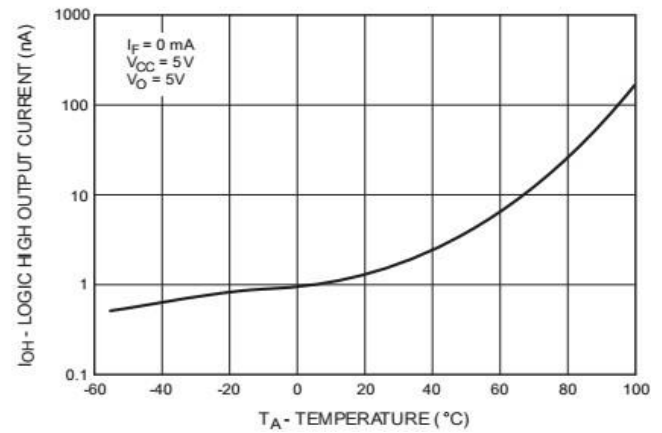


Fig. 5 Propagation Delay vs. Temperature

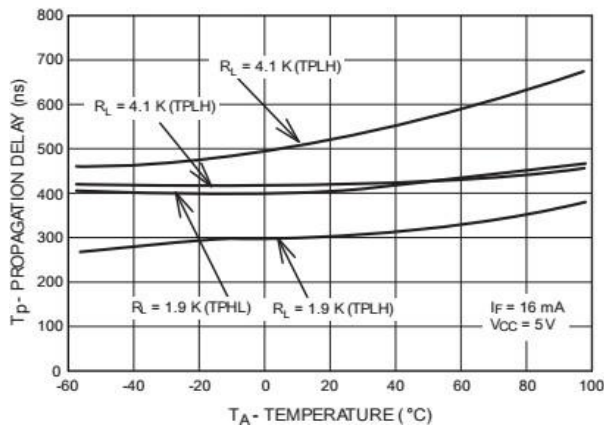
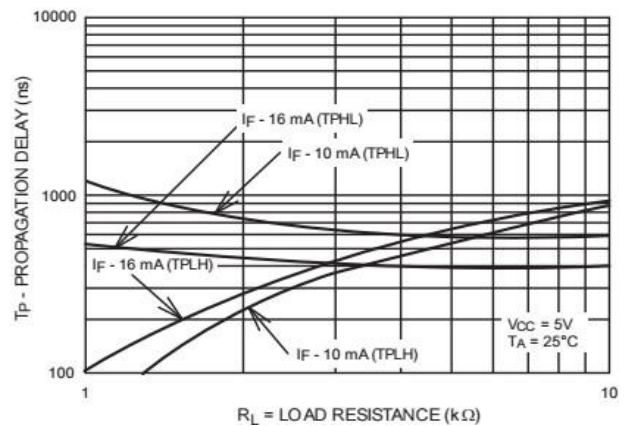


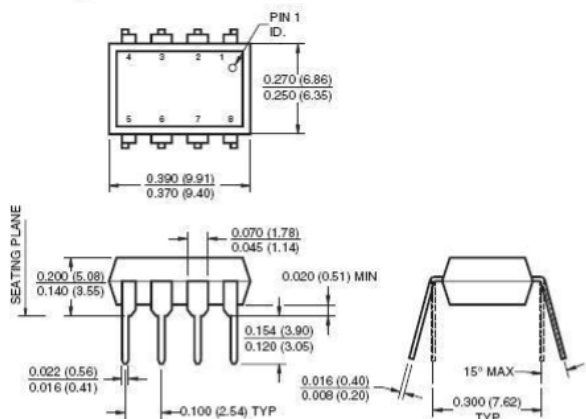
Fig. 6 Propagation Delay vs. Load Resistance



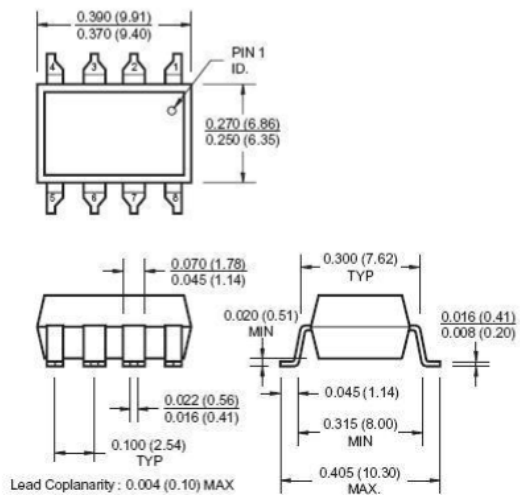
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Package Dimensions

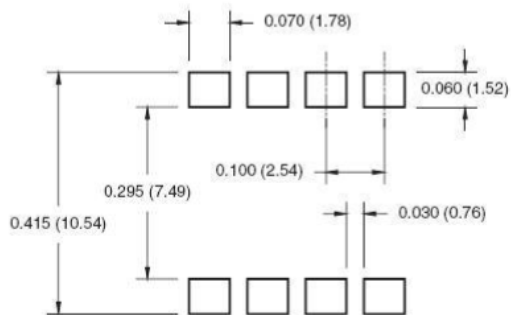
Through Hole



Surface Mount



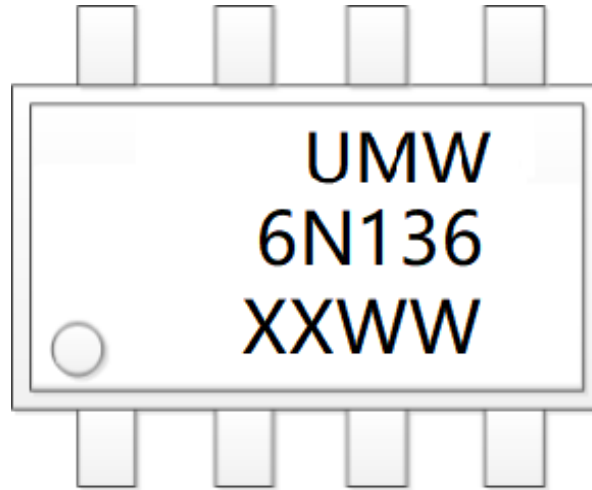
8-Pin DIP – Land Pattern



Note: All dimensions are in inches (millimeters)

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Marking



- “XX” denotes YEAR;
- “WW” denotes WEEK

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