

**FEATURES**

- Offset voltage: 2.2 mV maximum
- Low input bias current: 1 pA maximum
- Single-supply operation: 1.8 V to 5.5 V
- Low noise: 22 nV/ $\sqrt{\text{Hz}}$
- Micropower: 50  $\mu\text{A}$ /amplifier maximum over temperature
- No phase reversal
- Unity gain stable
- Qualified for automotive applications

**APPLICATIONS**

- Battery-powered instrumentation
- Multipole filters
- Current shunt sense
- Sensors
- ADC predrivers
- DAC drivers/level shifters
- Low power ASIC input or output amplifiers

**GENERAL DESCRIPTION**

The AD8613/AD8617/AD8619 are single, dual, and quad micro-power, rail-to-rail input and output amplifiers that feature low supply current, as well as low input voltage and current noise. The parts are fully specified to operate from 1.8 V to 5 V single supply, or  $\pm 0.9$  V and  $\pm 2.5$  V dual supply. The combination of low noise, very low input bias currents, and low power consumption make the AD8613/AD8617/AD8619 especially useful in portable and loop-powered instrumentation.

The ability to swing rail-to-rail at both the input and output enables designers to buffer CMOS ADCs, DACs, ASICs, and other wide output swing devices in low power, single-supply systems.

**PIN CONFIGURATIONS**

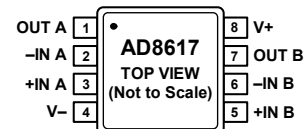
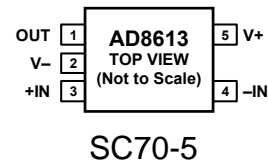
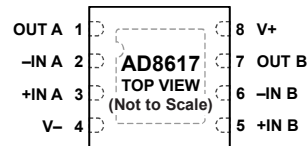


Figure 2. 8-Lead MSOP and 8-Lead SOIC\_N

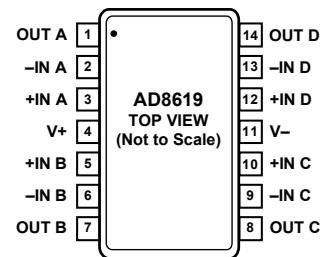
**SOP-8**



**NOTES**

1. PIN 4 AND THE EXPOSED PAD MUST BE CONNECTED TO V-.

**SOP-8**



**TSSOP-14/SOP-14**

## Low Cost Micropower, Low Noise CMOS Rail-to-Rail, Input/Output Operational Amplifiers

**SPECIFICATIONS**

 Electrical characteristics at  $V_{SY} = 5\text{ V}$ ,  $V_{CM} = V_{SY}/2$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$-0.3\text{ V} < V_{CM} < +5.3\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$ , $-0.3\text{ V} < V_{CM} < +5.2\text{ V}$		0.4	2.2	mV
Offset Voltage Drift AD8613	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	4.5	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	1	pA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.1	0.5	pA
Input Voltage Range	IVR		0		5	V
Common-Mode Rejection Ratio	CMRR	$0\text{ V} < V_{CM} < 5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	68	95		dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 10\text{ k}\Omega$ , $0.5\text{ V} < V_O < 4.5\text{ V}$	235	500		V/mV
Input Capacitance	$C_{DIFF}$ $C_{CM}$			1.9	2.5	pF
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$	4.95 4.9	4.98		V V
Output Voltage Low	$V_{OL}$	$I_L = 10\text{ mA}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$	4.50	4.7		V
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$		20	30	mV
Output Voltage Low	$V_{OL}$	$I_L = 10\text{ mA}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$		190	275	mV
Output Voltage Low	$V_{OL}$	$I_L = 10\text{ mA}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$			335	mV
Short-Circuit Current	$I_{SC}$			$\pm 80$		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 10\text{ kHz}$ , $A_V = 1$		15		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$1.8\text{ V} < V_{SY} < 5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	67 64	94		dB dB
Supply Current/Amplifier	$I_{SY}$	$V_O = V_{SY}/2$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		38	50	$\mu\text{A}$ $\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$		0.1		V/ $\mu\text{s}$
Settling Time to 0.1%	$t_S$	$G = \pm 1$ , $V_{IN} = 2\text{ V}$ step, $C_L = 20\text{ pF}$ , $R_L = 1\text{ k}\Omega$		23		$\mu\text{s}$
Gain Bandwidth Product	GBP	$R_L = 100\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$		400	350	kHz kHz
Phase Margin	$\phi_M$	$R_L = 10\text{ k}\Omega$ , $R_L = 100\text{ k}\Omega$ , $C_L = 20\text{ pF}$		70		Degrees
<b>NOISE PERFORMANCE</b>						
Peak-to-Peak Noise	$e_n$ p-p	0.1 Hz to 10 Hz		2.3	3.5	$\mu\text{V}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$ $f = 10\text{ kHz}$		25 22		nV/ $\sqrt{\text{Hz}}$ nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.05		pA/ $\sqrt{\text{Hz}}$

**Low Cost Micropower, Low Noise CMOS Rail-to-Rail, Input/Output Operational Amplifiers**

 Electrical characteristics at  $V_{SY} = 1.8\text{ V}$ ,  $V_{CM} = V_{SY}/2$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$-0.3\text{ V} < V_{CM} < +1.9\text{ V}$ $-0.3\text{ V} < V_{CM} < +1.8\text{ V}; -40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.4	2.2	mV
Offset Voltage Drift AD8613	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	8.5	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	1	pA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.1	0.5	pA
Input Voltage Range	IVR		0		1.8	V
Common-Mode Rejection Ratio	CMRR	$0\text{ V} < V_{CM} < 1.8\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	58	86		dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 10\text{ k}\Omega$ , $0.5\text{ V} < V_O < 1.3\text{ V}$	85	1000		V/mV
Input Capacitance	$C_{DIFF}$ $C_{CM}$			2.1		pF
				3.8		pF
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$	1.65	1.73		V
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$	1.6	44	60	V
Short-Circuit Current	$I_{SC}$			$\pm 7$	80	mV
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 10\text{ kHz}$ , $A_V = 1$		15		mV
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$1.8\text{ V} < V_S < 5\text{ V}$	67	94		dB
Supply Current/Amplifier	$I_{SY}$	$V_O = V_{SY}/2$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		38	50	$\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$		0.1		V/ $\mu\text{s}$
Settling Time to 0.1%	$t_S$	$G = \pm 1$ , $V_{IN} = 1\text{ V}$ step, $C_L = 20\text{ pF}$ , $R_L = 1\text{ k}\Omega$		6.5		$\mu\text{s}$
Gain Bandwidth Product	GBP	$R_L = 100\text{ k}\Omega$ $R_L = 10\text{ k}\Omega$		400	350	kHz
Phase Margin	$\phi_M$	$R_L = 10\text{ k}\Omega$ , $R_L = 100\text{ k}\Omega$ , $C_L = 20\text{ pF}$		70		Degrees
<b>NOISE PERFORMANCE</b>						
Peak-to-Peak Noise	$e_n$ p-p	0.1 Hz to 10 Hz		2.3	3.5	$\mu\text{V}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$ $f = 10\text{ kHz}$		25		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.05		$\text{pA}/\sqrt{\text{Hz}}$

## ABSOLUTE MAXIMUM RATINGS

T<sub>A</sub> = 25°C, unless otherwise noted.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	V <sub>SS</sub> – 0.3 V to V <sub>DD</sub> + 0.3 V
Input Current	±10 mA
Differential Input Voltage	±6 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–40°C to +125°C
Junction Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
ESD AD8613	
HBM	±4000 V
FICDM	±1000 V
ESD AD8617	
HBM	±3000 V
FICDM	±1000 V
MM	±100 V
ESD AD8619	
HBM	±4000 V
FICDM	±1250 V
MM	±200 V

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{SY} = 5\text{ V}$  or  $\pm 2.5\text{ V}$ , unless otherwise noted.

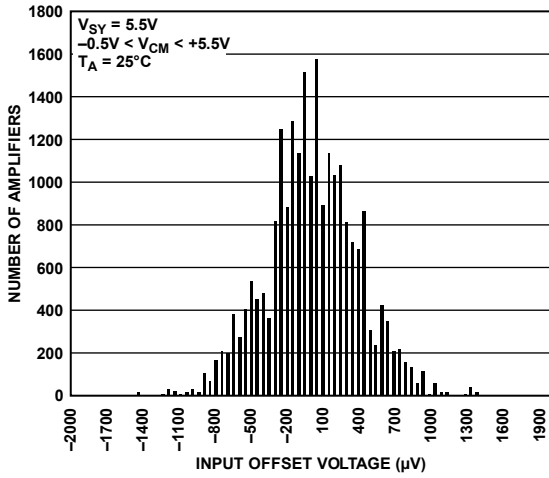


Figure 5. Input Offset Voltage Distribution

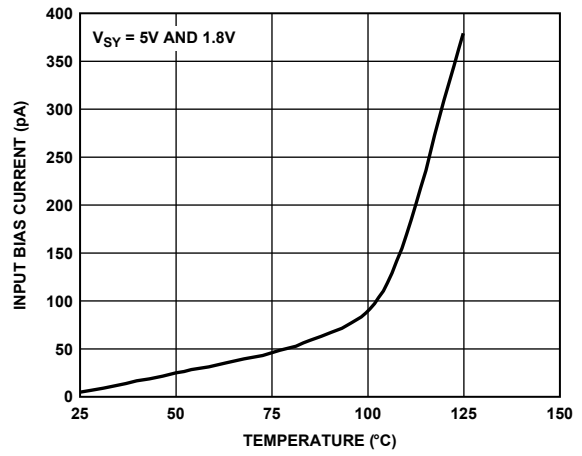


Figure 8. Input Bias Current vs. Temperature

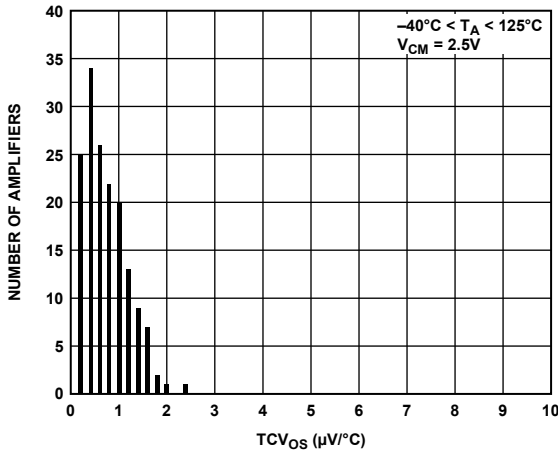


Figure 6. Input Offset Voltage Drift Distribution

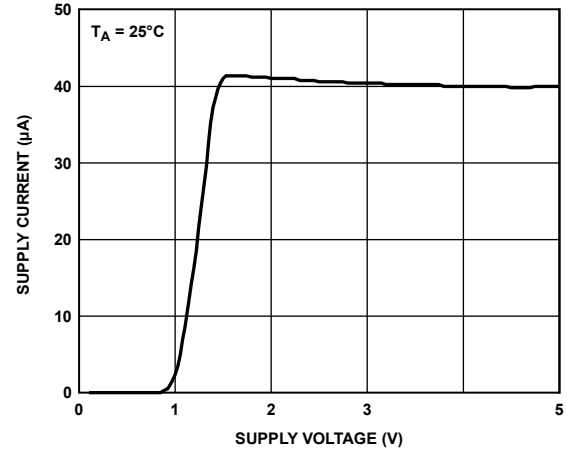


Figure 9. Supply Current vs. Supply Voltage

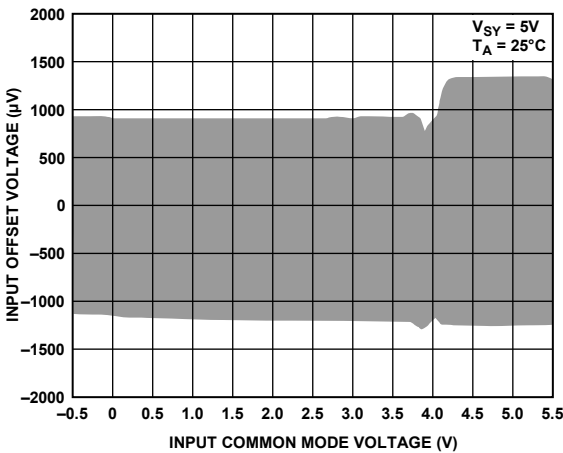


Figure 7. Input Offset Voltage vs. Input Common-Mode Voltage

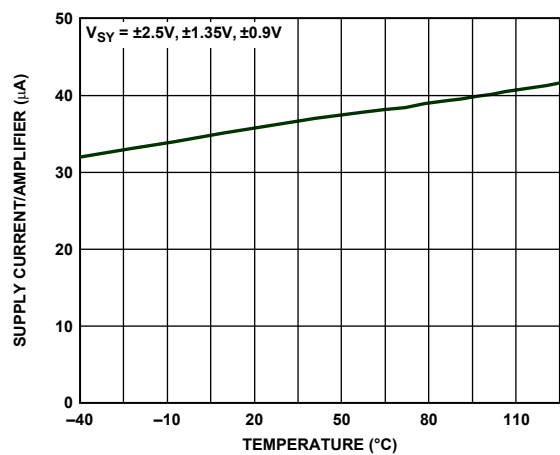


Figure 10. Supply Current vs. Temperature

Low Cost Micropower, Low Noise CMOS Rail-to-Rail, Input/Output Operational Amplifiers

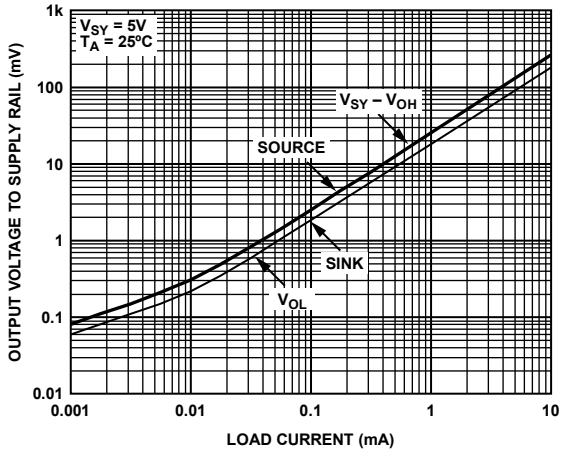


Figure 11. Output Voltage to Supply Rail vs. Load Current

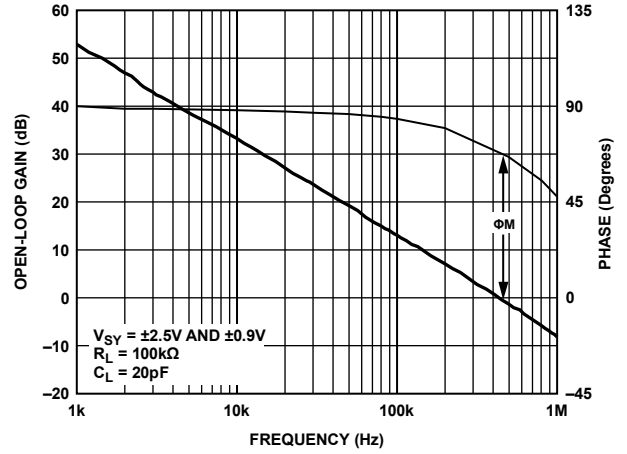


Figure 14. Open-Loop Gain and Phase vs. Frequency

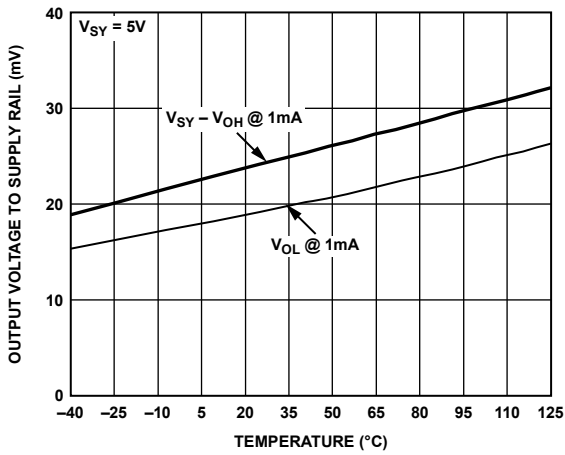


Figure 12. Output Voltage to Supply Rail vs. Temperature ( $I_L = 1\text{ mA}$ )

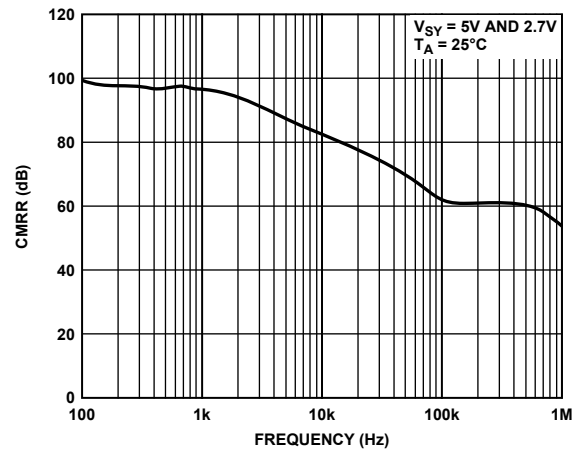


Figure 15. CMRR vs. Frequency

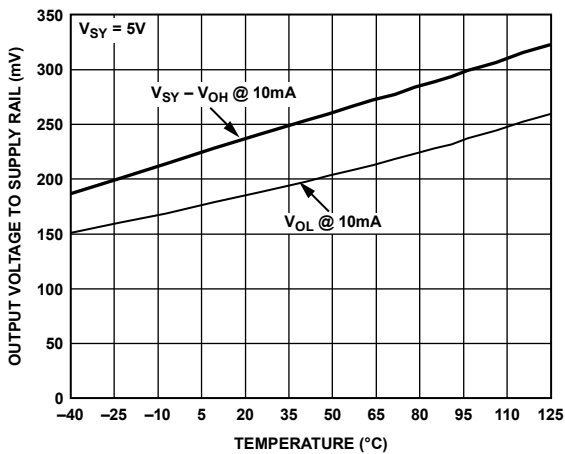


Figure 13. Output Voltage to Supply Rail vs. Temperature ( $I_L = 10\text{ mA}$ )

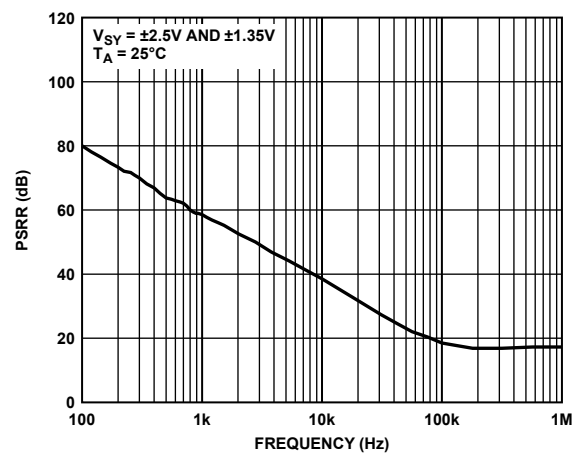


Figure 16. PSRR vs. Frequency

Low Cost Micropower, Low Noise CMOS Rail-to-Rail, Input/Output Operational Amplifiers

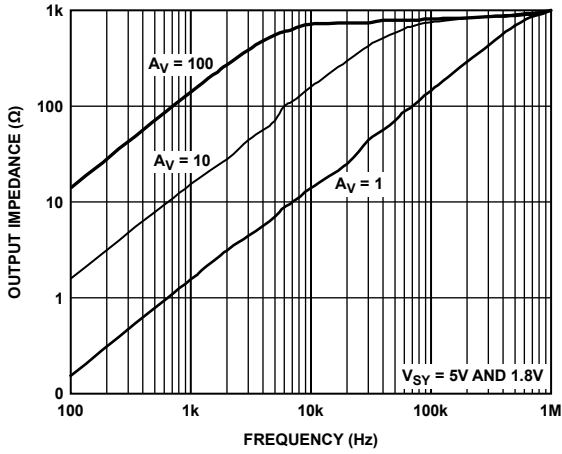


Figure 17. Output Impedance vs. Frequency

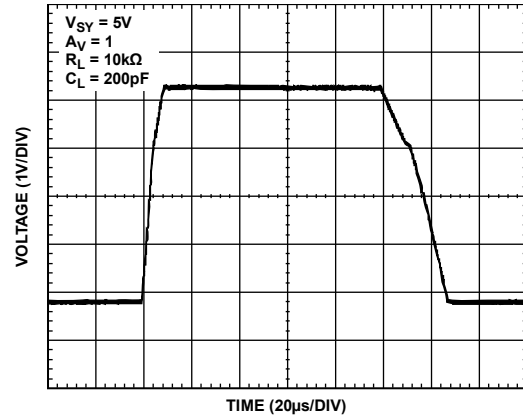


Figure 20. Large Signal Transient Response

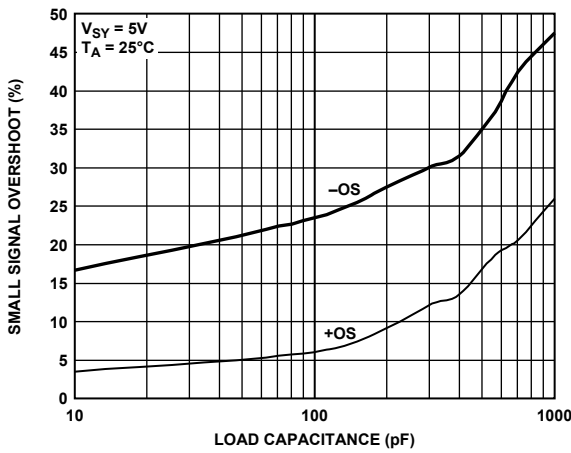


Figure 18. Small Signal Overshoot vs. Load Capacitance

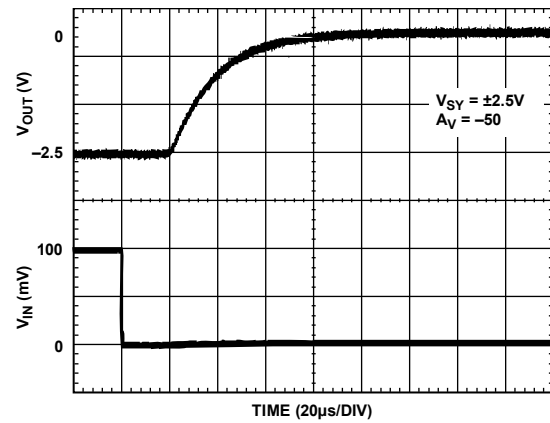


Figure 21. Positive Overload Recovery

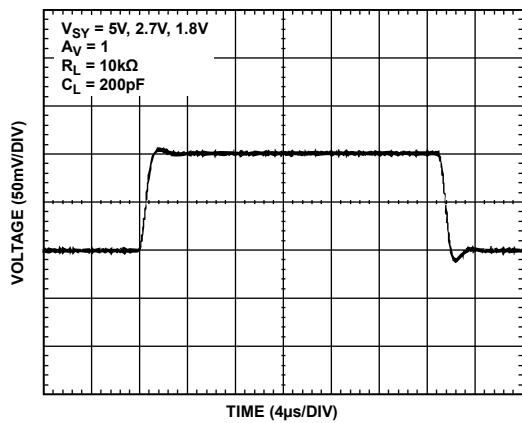


Figure 19. Small Signal Transient Response

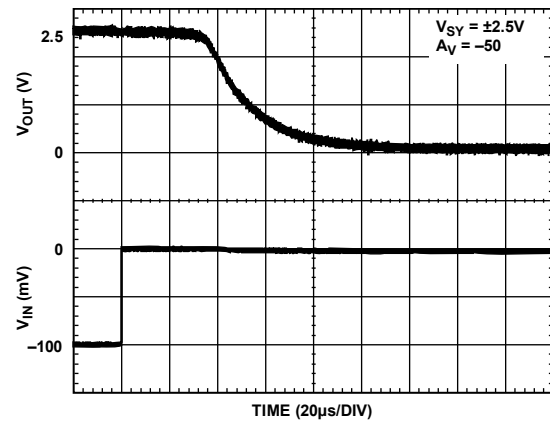


Figure 22. Negative Overload Recovery

Low Cost Micropower, Low Noise CMOS Rail-to-Rail, Input/Output Operational Amplifiers

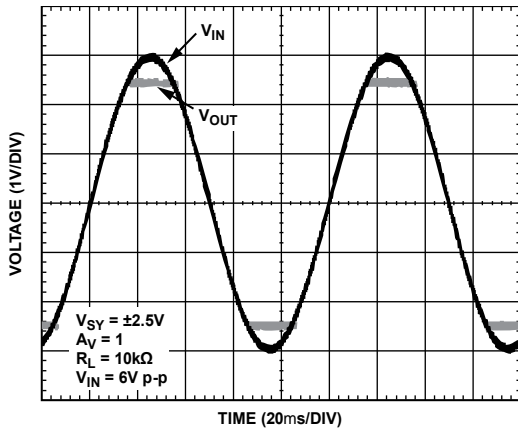


Figure 23. No Phase Reversal

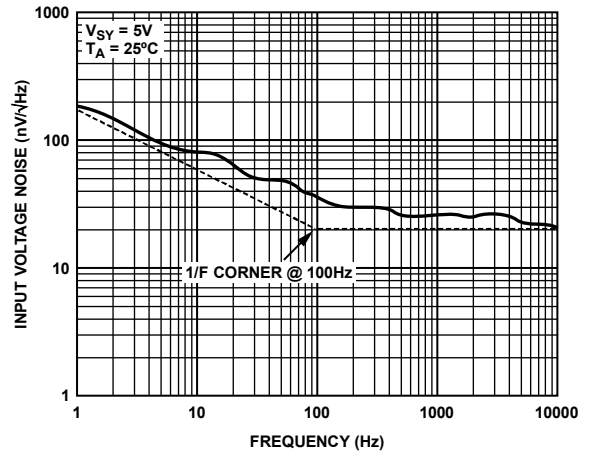


Figure 25. Voltage Noise Density

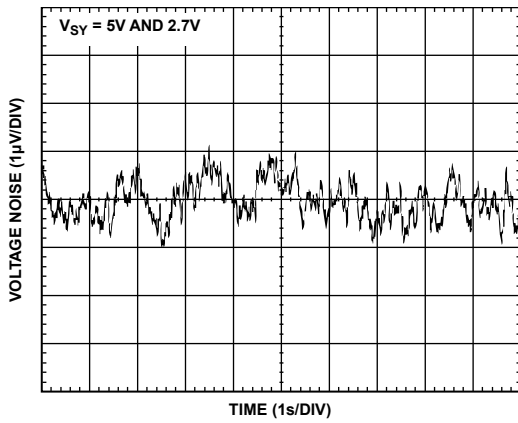


Figure 24. 0.1 Hz to 10 Hz Input Voltage Noise

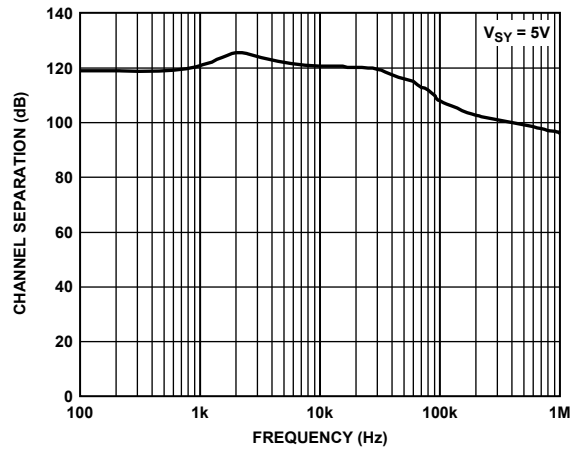


Figure 26. Channel Separation



Low Cost Micropower, Low Noise CMOS Rail-to-Rail, Input/Output Operational Amplifiers

$V_{SY} = 1.8\text{ V}$  or  $\pm 0.9\text{ V}$ , unless otherwise noted.

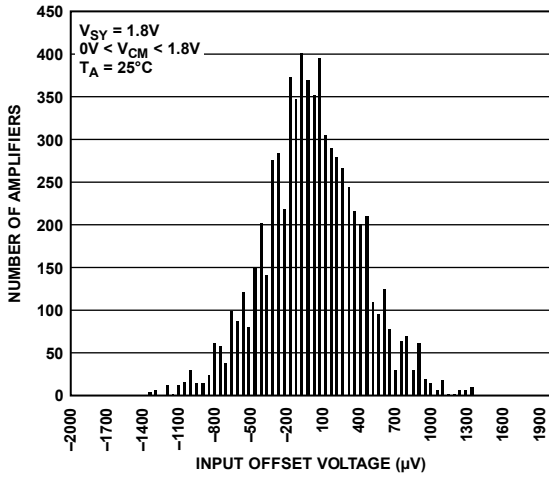


Figure 27. Input Offset Voltage Distribution

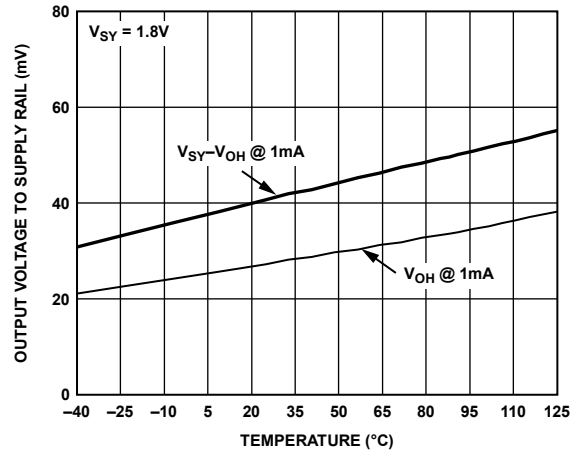


Figure 30. Output Voltage to Supply Rail vs. Temperature ( $I_L = 1\text{ mA}$ )

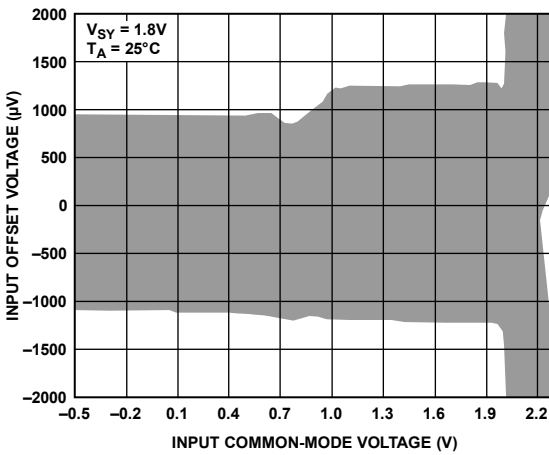


Figure 28. Input Offset Voltage vs. Input Common-Mode Voltage

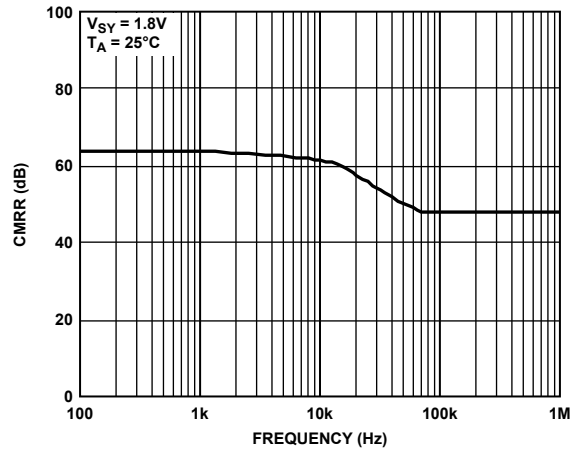


Figure 31. CMRR vs. Frequency

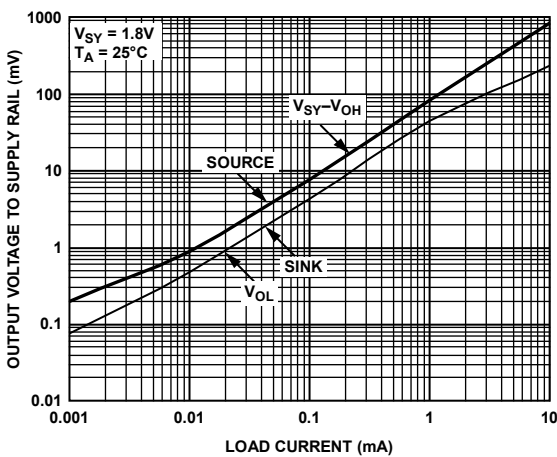


Figure 29. Output Voltage to Supply Rail vs. Load Current

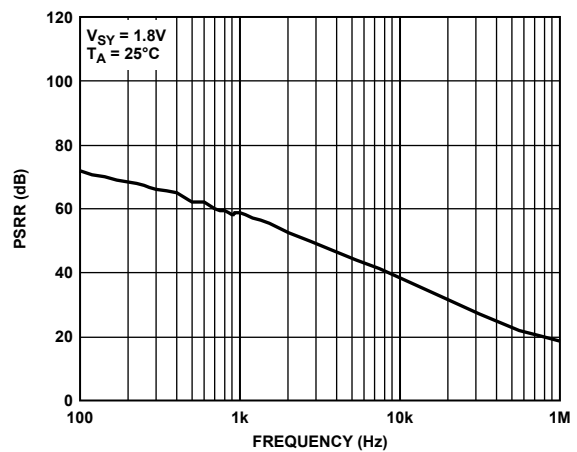


Figure 32. PSRR vs. Frequency

Low Cost Micropower, Low Noise CMOS Rail-to-Rail, Input/Output Operational Amplifiers

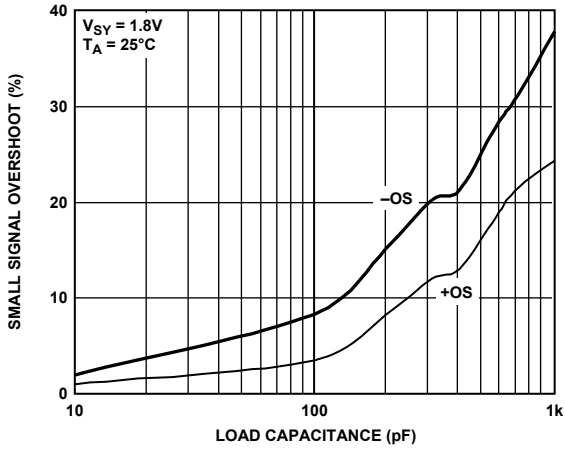


Figure 33. Small Signal Overshoot vs. Load Capacitance

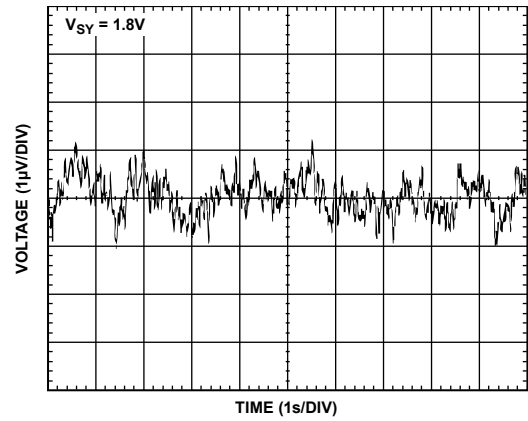


Figure 35. 0.1 Hz to 10 Hz Input Voltage Noise

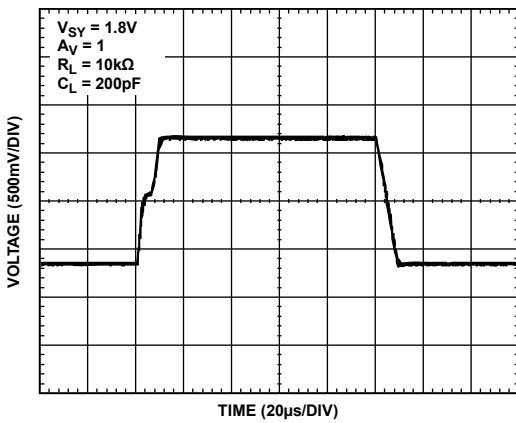


Figure 34. Large Signal Transient Response

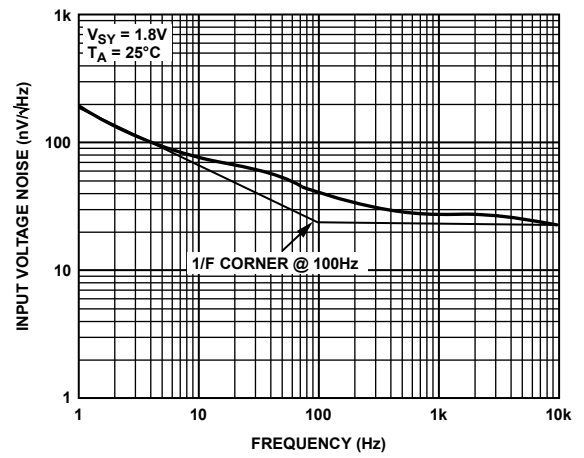
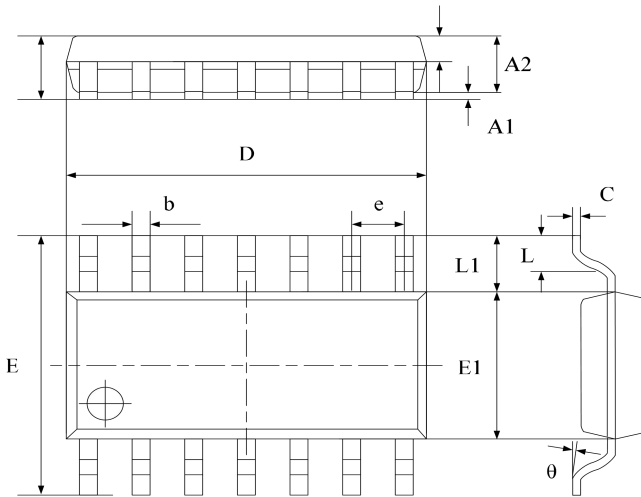


Figure 36. Voltage Noise Density

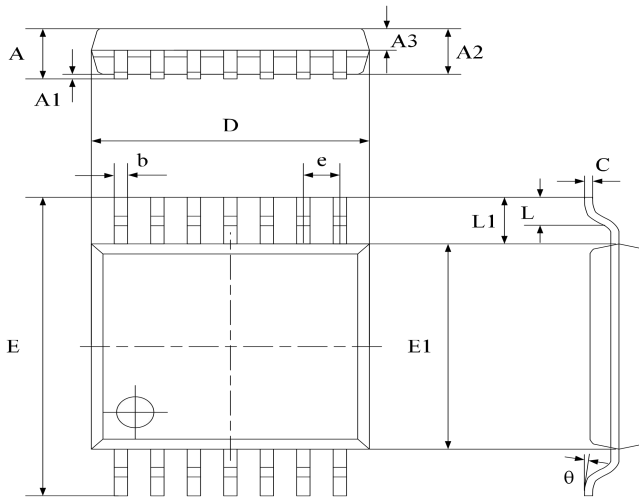
Package Dimension

SOP-14



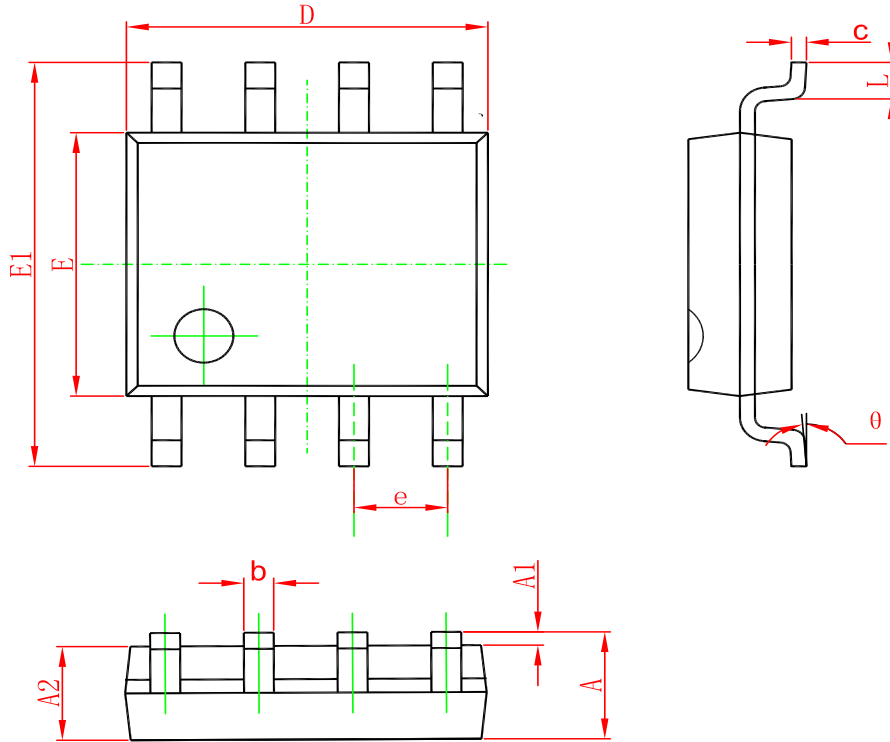
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.450	1.850	0.059	0.076
A1	0.100	0.300	0.004	0.012
A2	1.350	1.550	0.055	0.063
A3	0.550	0.750	0.022	0.031
b	0.406typ.		0.017typ.	
C	0.203typ.		0.008typ.	
D	8.630	8.830	0.352	0.360
E	5.840	6.240	0.238	0.255
E1	3.850	4.050	0.157	0.165
e	1.270 typ.		0.050 typ.	
L1	1.040 ref.		0.041 ref.	
L	0.350	0.750	0.014	0.031
θ	2°	8°	2°	8°

TSSOP-14



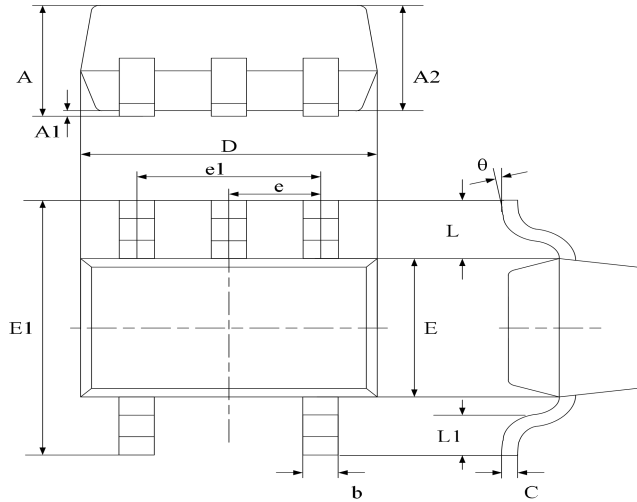
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.200	-	0.0472
A1	0.050	0.150	0.002	0.006
A2	0.900	1.050	0.037	0.043
A3	0.390	0.490	0.016	0.020
b	0.200	0.290	0.008	0.012
C	0.130	0.180	0.005	0.007
D	4.860	5.060	0.198	0.207
E	6.200	6.600	0.253	0.269
E1	4.300	4.500	0.176	0.184
e	0.650 typ.		0.0256 typ.	
L1	1.000 ref.		0.0393 ref.	
L	0.450	0.750	0.018	0.031
θ	0°	8°	0°	8°

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°

SC70-5 (SOT353)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.800	0.900	0.035	0.039
b	0.150	0.350	0.006	0.014
C	0.080	0.150	0.003	0.006
D	1.8500	2.150	0.079	0.087
E	1.100	1.400	0.045	0.053
E1	1.950	2.200	0.085	0.096
e	0.850 typ.		0.026 typ.	
e1	1.200	1.400	0.047	0.055
L	0.42 ref.		0.021 ref.	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°

Ordering information

Order code	Package	Baseqty	Deliverymode	Marking
UMW AD8619ARZ	SOP-14	2500	Tape and reel	AD8619
UMW AD8619ARUZ	TSSOP-14	4000	Tape and reel	AD8619
UMW AD8613AKSZ	SC70-5	3000	Tape and reel	A0T U
UMW AD8617ARZ	SOP-8	2500	Tape and reel	AD8617

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