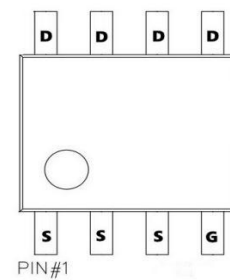
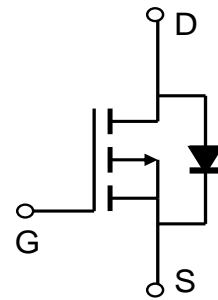


General Description

- Latest Advanced Trench Technology
- Low $R_{DS(ON)}$
- High Current Capability
- RoHS and Halogen-Free Compliant

Product Summary

V_{DS}	-30V
I_D (at $V_{GS}=-10V$)	-14A
$R_{DS(ON)}$ (at $V_{GS}=-10V$)	< 11.5m Ω
$R_{DS(ON)}$ (at $V_{GS}=-4.5V$)	< 18.5m Ω



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current	I_D	$T_A=25^\circ C$	-14
		$T_A=70^\circ C$	-11
Pulsed Drain Current ^C	I_{DM}	-56	A
Avalanche Current ^C	I_{AS}	-33	A
Avalanche energy L=0.1mH ^C	E_{AS}	54	mJ
Power Dissipation ^B	P_D	$T_A=25^\circ C$	3.1
		$T_A=70^\circ C$	2.0
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	31	40	$^\circ C/W$
Maximum Junction-to-Ambient ^{A,D}				
Maximum Junction-to-Lead	$R_{\theta JL}$	16	24	$^\circ C/W$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-30			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V			-1	μA
		T _J =55°C			-5	
advanced	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±25V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1.3	-1.8	-2.3	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-14A		9.5	11.5	mΩ
		V _{GS} =-4.5V, I _D =-10A		14.7	18.5	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-14A		42		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.7	-1	V
I _S	Maximum Body-Diode Continuous Current				-4	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, f=1MHz		2050		pF
C _{oss}	Output Capacitance			330		pF
C _{rss}	Reverse Transfer Capacitance			300		pF
R _g	Gate resistance	f=1MHz		3.2	6.4	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =-10V, V _{DS} =-15V, I _D =-14A		40	60	nC
Q _{g(4.5V)}	Total Gate Charge			20	30	nC
Q _{gs}	Gate Source Charge			6		nC
Q _{gd}	Gate Drain Charge			10		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-15V, R _L =1.05Ω, R _{GEN} =3Ω		11		ns
t _r	Turn-On Rise Time			10		ns
t _{D(off)}	Turn-Off DelayTime			40		ns
t _f	Turn-Off Fall Time			18		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =-14A, di/dt=500A/μs		14		ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-14A, di/dt=500A/μs		25		nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

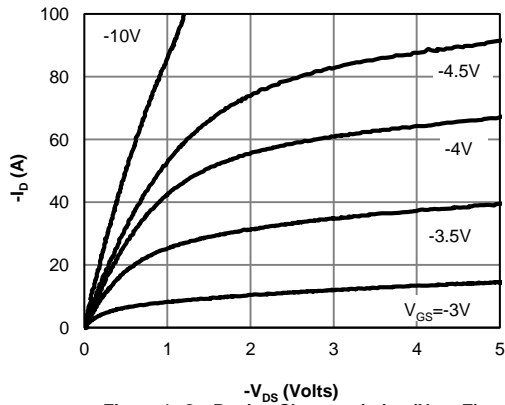


Figure 1: On-Region Characteristics (Note E)

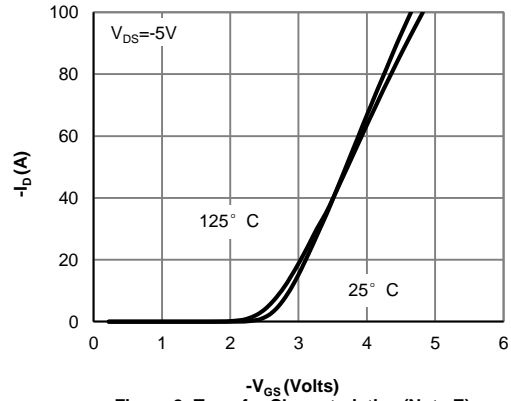


Figure 2: Transfer Characteristics (Note E)

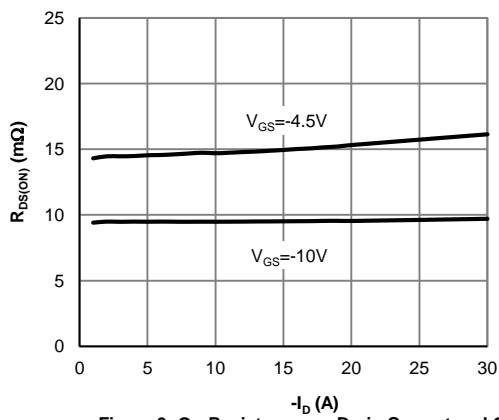


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

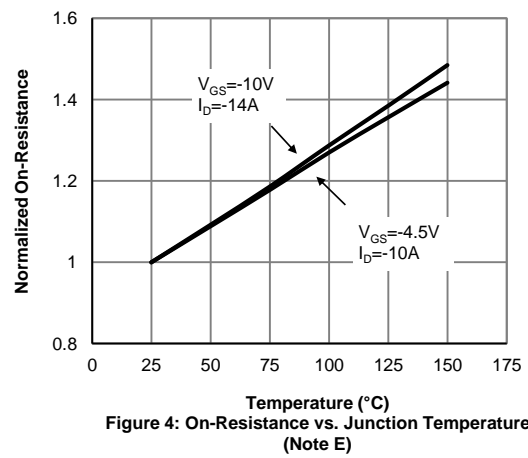


Figure 4: On-Resistance vs. Junction Temperature (Note E)

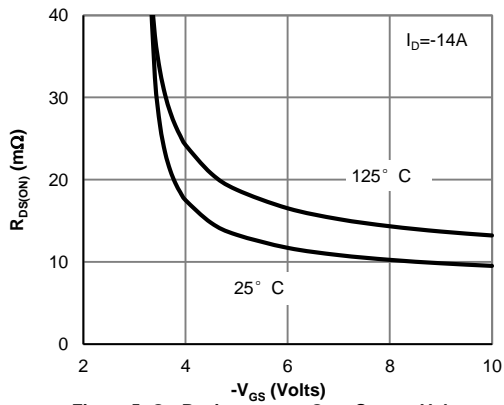


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

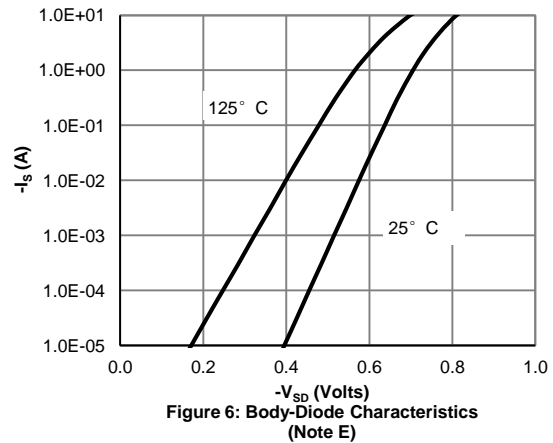


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

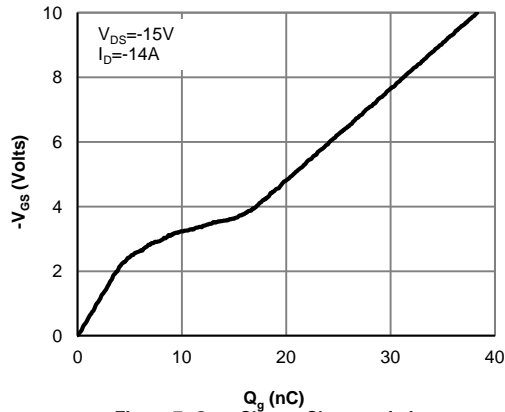


Figure 7: Gate-Charge Characteristics

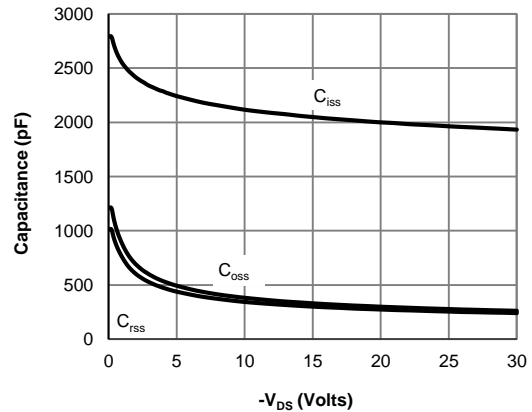


Figure 8: Capacitance Characteristics

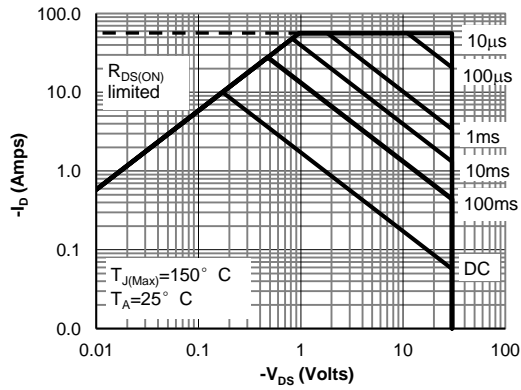


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

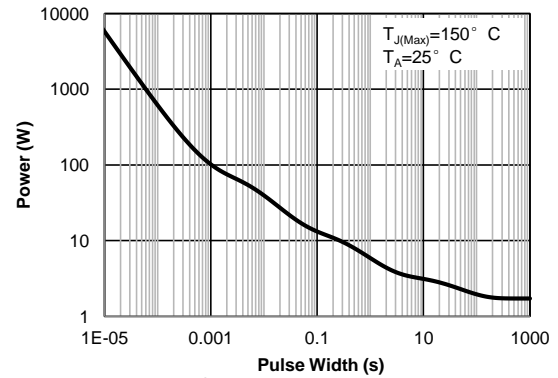


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

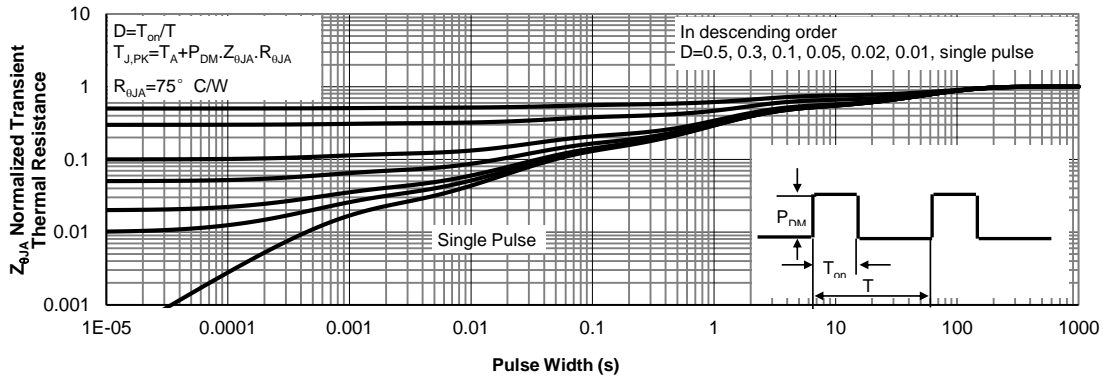
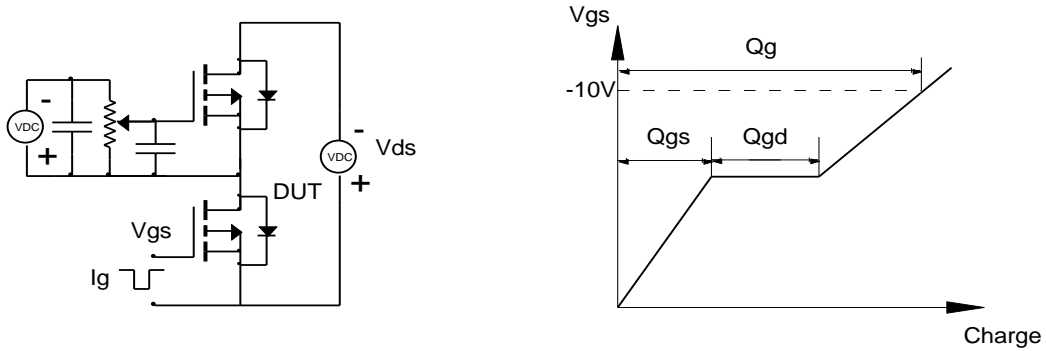
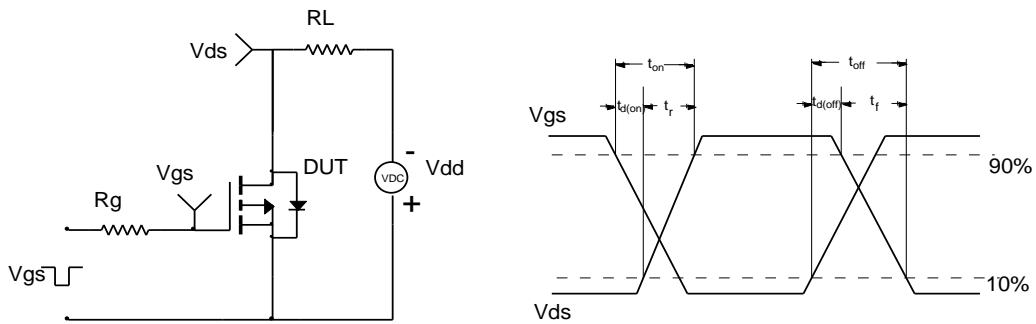


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

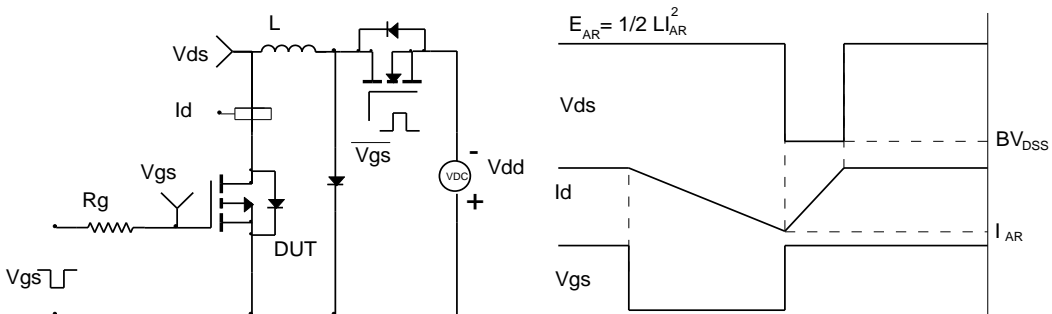
Gate Charge Test Circuit & Waveform



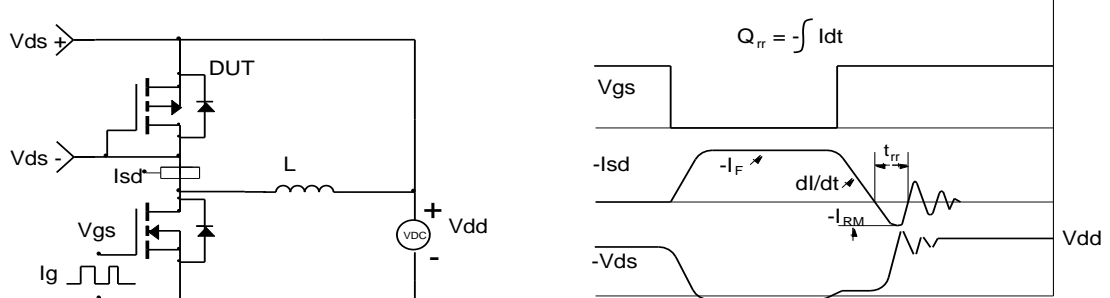
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

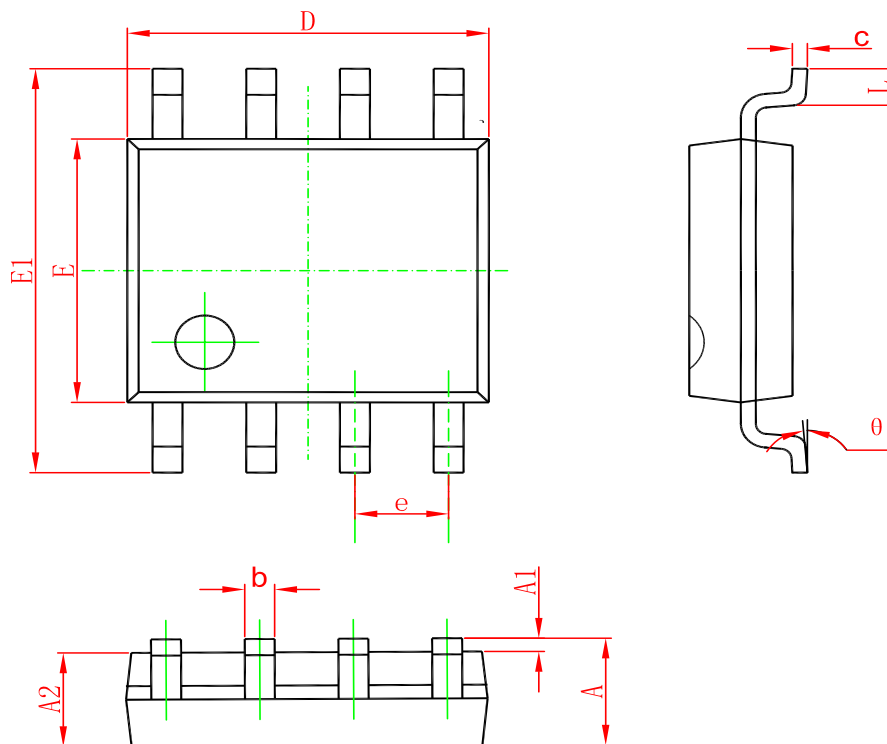


Diode Recovery Test Circuit & Waveforms



PACKAGE OUTLINE DIMENSIONS

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Marking

AO4407
UMW xxxx

Ordering information

Order code	Package	Baseqty	Deliverymode
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