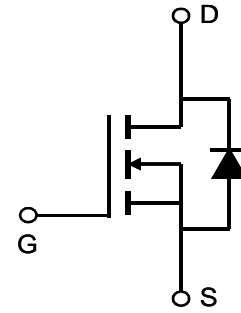


General Description

The AO4486 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for boost converters and synchronous rectifiers for consumer, telecom, industrial power supplies and LED backlighting.



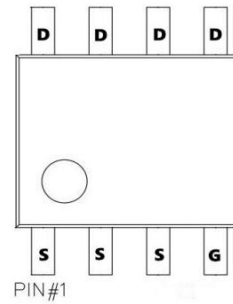
Product Summary

$V_{DS} (V) = 100V$

$I_D = 4.2A$

$R_{DS(ON)} < 79m\Omega (V_{GS} = 10V)$

$R_{DS(ON)} < 94m\Omega (V_{GS} = 4.5V)$



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_A=25^\circ C$	A
		$T_A=70^\circ C$	
Pulsed Drain Current ^C	I_{DM}	31	
Avalanche Current ^C	I_{AS}, I_{AR}	14	A
Avalanche energy $L=0.1mH$ ^C	E_{AS}, E_{AR}	10	mJ
Power Dissipation ^B	P_D	$T_A=25^\circ C$	W
		$T_A=70^\circ C$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	31	40	$^\circ C/W$
Maximum Junction-to-Ambient ^{A D}		Steady-State	59	75
Maximum Junction-to-Lead	$R_{\theta JL}$	16	24	$^\circ C/W$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	100			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =100V, V _{GS} =0V T _J =55°C			1	μA
					5	
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	1.6	2.2	2.7	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	31			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =5A		69	79	mΩ
		V _{GS} =4.5V, I _D =3A		82	94	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =3A		20		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.74	1	V
I _S	Maximum Body-Diode Continuous Current				3.5	A
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =50V, f=1MHz	620	778	942	pF
C _{oss}	Output Capacitance		38	55	81	pF
C _{rss}	Reverse Transfer Capacitance		13	24	35	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.7	1.45	2.2	Ω
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =50V, I _D =3.0A	13	16.3	20	nC
Q _{g(4.5V)}	Total Gate Charge		6.4	8.1	10	nC
Q _{gs}	Gate Source Charge		2.2	2.8	3.4	nC
Q _{gd}	Gate Drain Charge		2.4	4.1	5.8	nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =50V, R _L =16.7Ω, R _{GEN} =3Ω		6		ns
t _r	Turn-On Rise Time			2.5		ns
t _{D(off)}	Turn-Off DelayTime			21		ns
t _f	Turn-Off Fall Time			2.4		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =3A, dI/dt=500A/μs	14	21	28	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =3A, dI/dt=500A/μs	65	94	123	nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

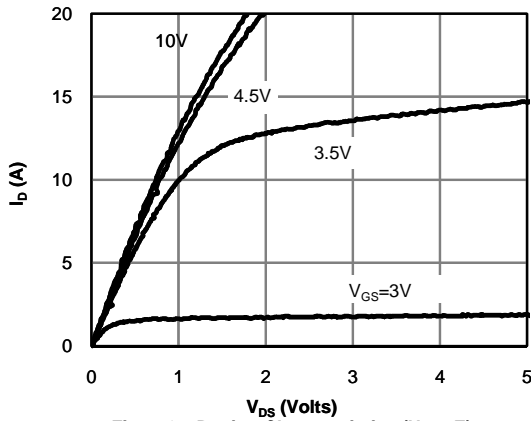


Fig 1: On-Region Characteristics (Note E)

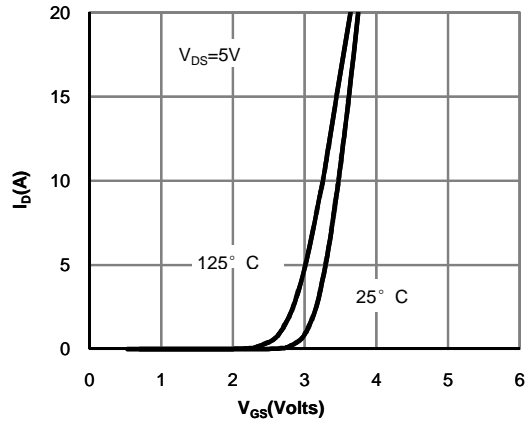


Figure 2: Transfer Characteristics (Note E)

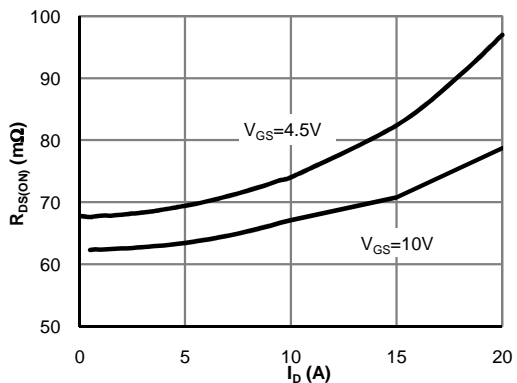


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

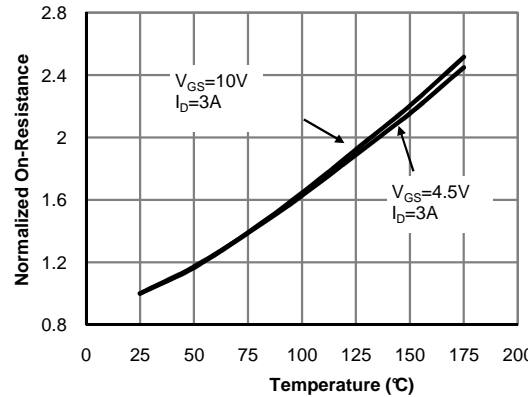


Figure 4: On-Resistance vs. Junction Temperature (Note E)

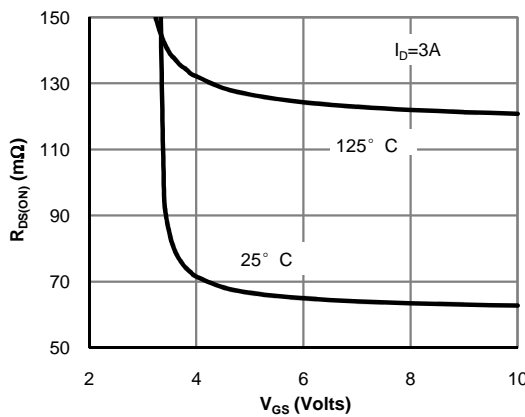


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

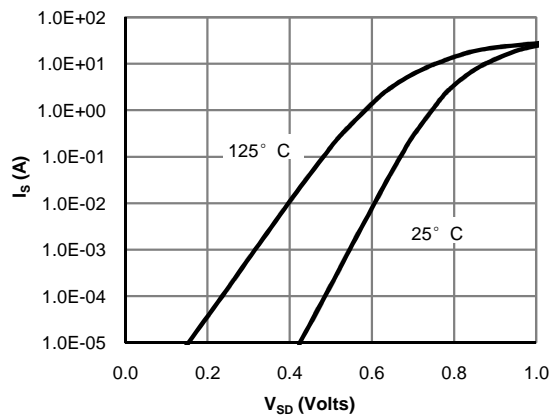


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

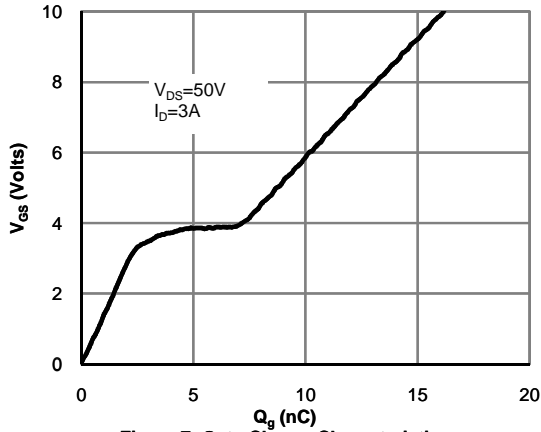


Figure 7: Gate-Charge Characteristics

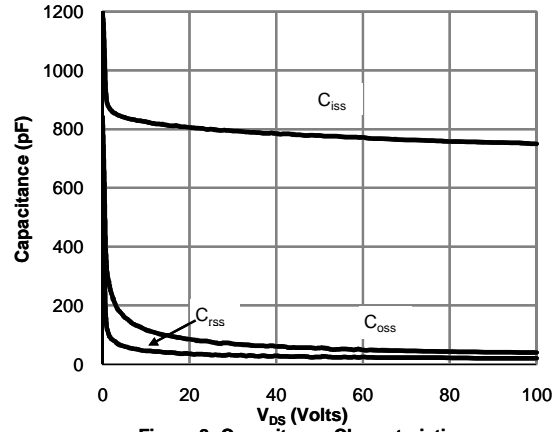


Figure 8: Capacitance Characteristics

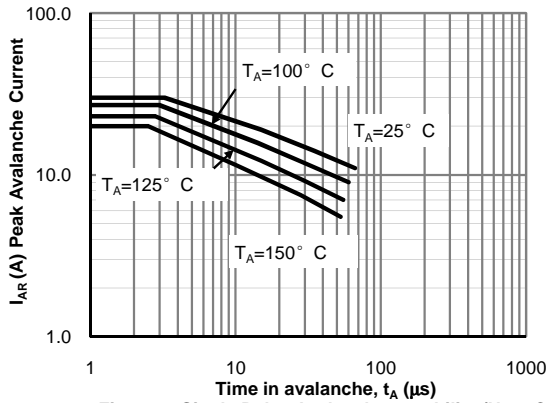


Figure 9: Single Pulse Avalanche capability (Note C)

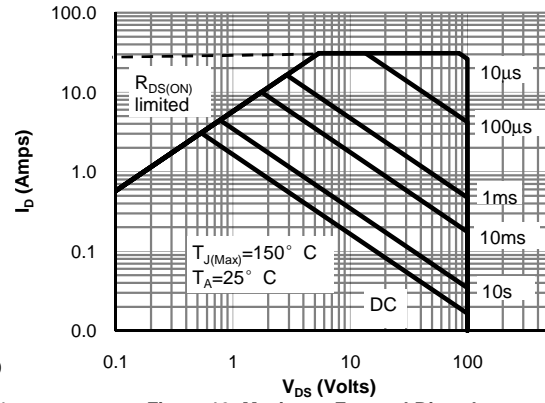


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

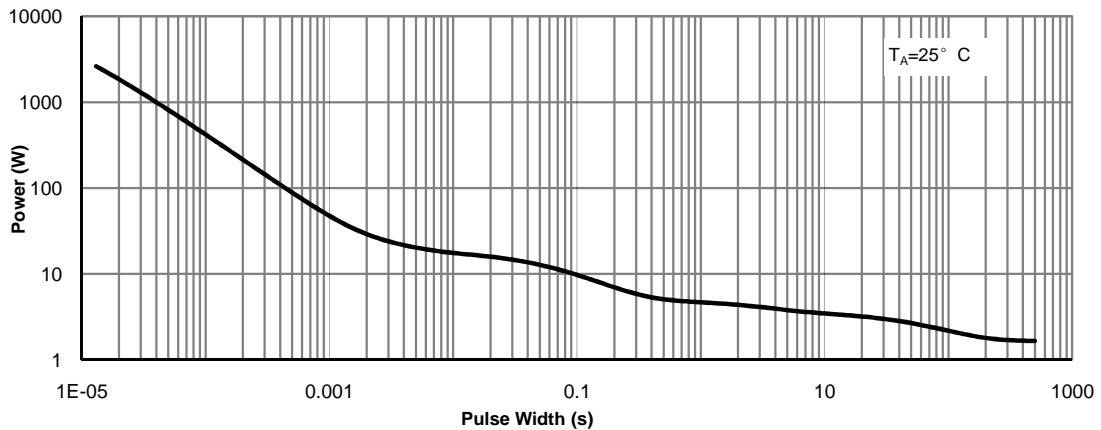
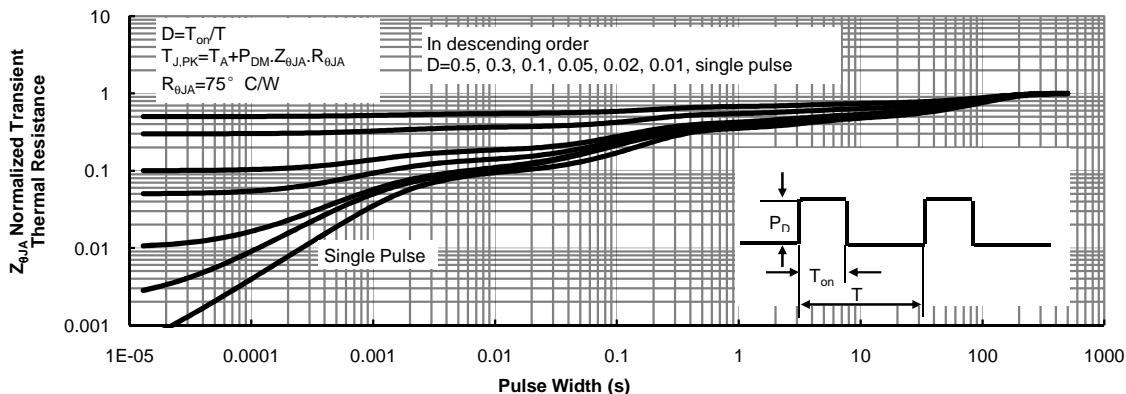
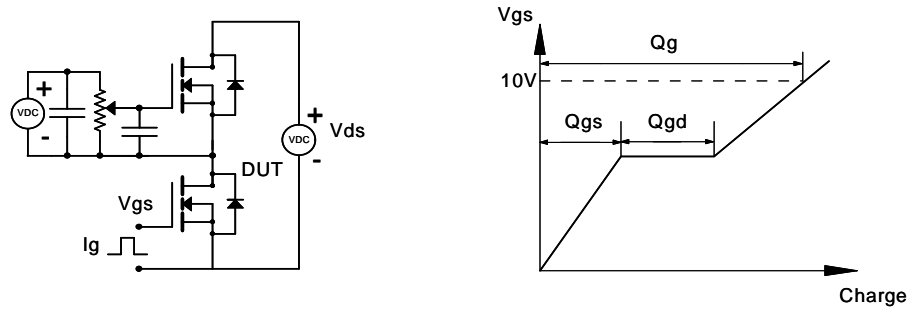


Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)

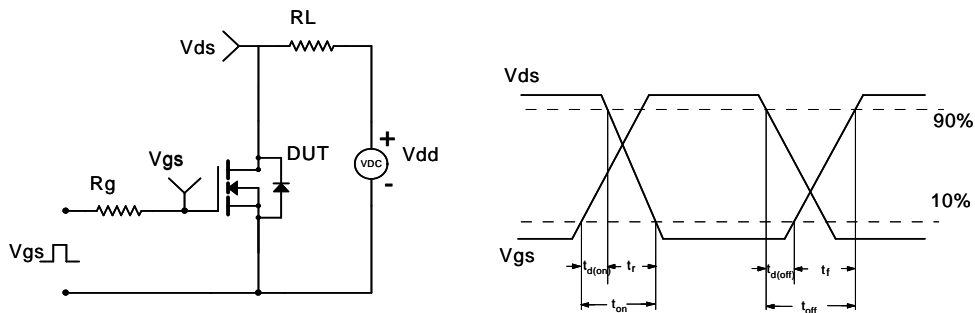
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



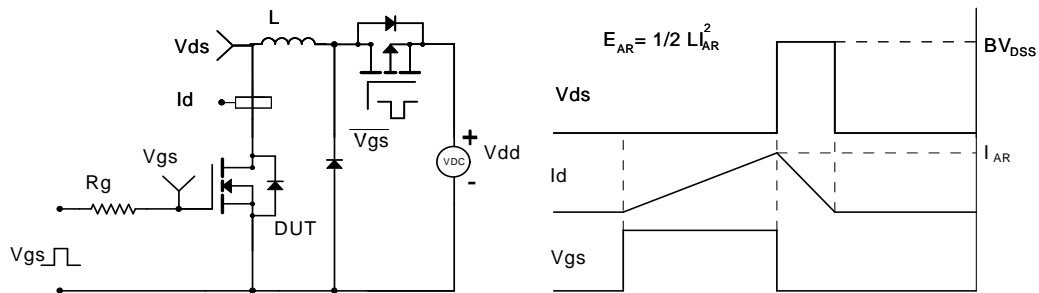
Gate Charge Test Circuit & Waveform



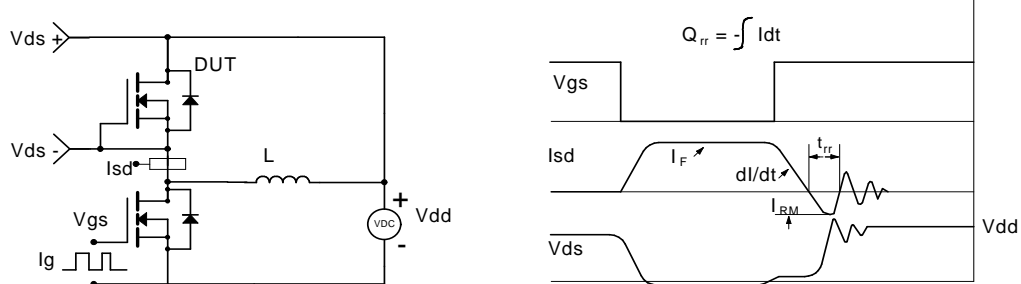
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

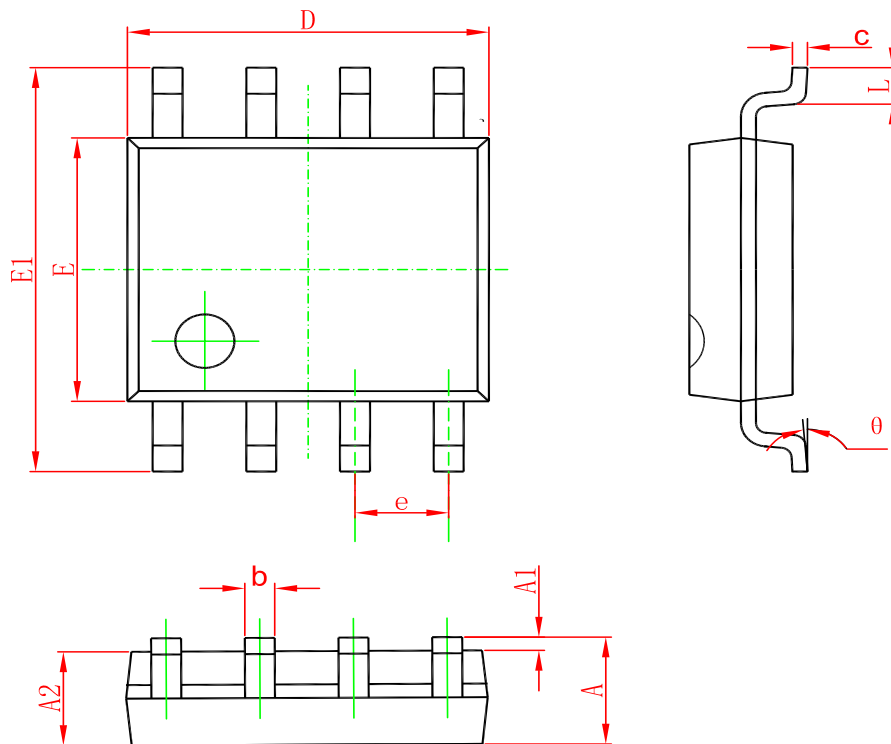


Diode Recovery Test Circuit & Waveforms



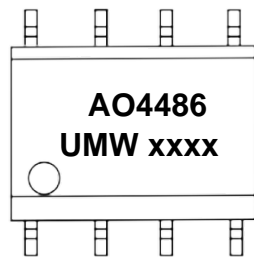
PACKAGE OUTLINE DIMENSIONS

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Marking



("xxxx"代表年份周期)

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