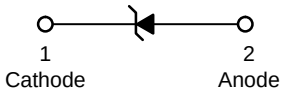
Descriptions

The ESD5Zxx Series is designed to protect voltage sensitive components from ESD and transient voltage events. Excellent clamping capability, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its small size, it is suited for use in cellular phones, portable devices, digital cameras, power supplies and many other portable applications.



MARKING DIAGRAM

Specification Features:

- Low Clamping Voltage
- Small Body Outline Dimensions:
  0.047″ x 0.032″ (1.20 mm x 0.80 mm)
- Low Body Height: 0.028″ (0.7 mm)
- Stand−off Voltage: 2.5 V − 12 V
- Peak Power up to 240 Watts @ 8 x 20 μs Pulse
- Low Leakage
- Response Time is Typically < 1 ns
- ESD Rating of Class 3 (> 16 kV) per Human Body Model
- IEC61000−4−2 Level 4 ESD Protection
- IEC61000−4−4 Level 4 EFT Protection
- These Devices are Pb−Free and are RoHS Compliant

Mechanical Characteristics:

CASE: Void-free, transfer-molded, thermosetting plastic Epoxy Meets UL 94 V−0

LEAD FINISH: 100% Matte Sn (Tin)

MOUNTING POSITION: Any

QUALIFIED MAX REFLOW TEMPERATURE: 260°C

Device Meets MSL 1 Requirements

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IEC 61000−4−2 (ESD) Contact Air		 ±30 ±30	kV
IEC 61000−4−4 (EFT)		40	A
ESD Voltage Per Human Body Model Per Machine Model		 16 400	kV V
Total Power Dissipation on FR−4 Board (Note 1) @ T_A = 25°C	P_D	500	mW
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Second Duration)	T_L	260	°C

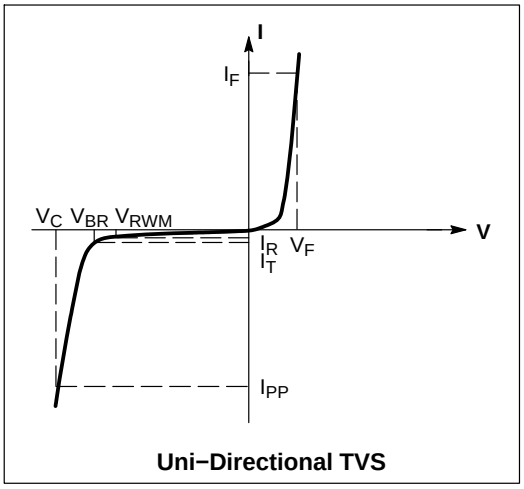
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR−4 printed circuit board, single−sided copper, mounting pad 1 cm^2.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Max. Capacitance @V_R = 0 and f = 1 MHz



Uni−Directional TVS

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, V_F = 1.1 V Max. @ I_F = 10 mA for all types)

Device	Device Marking	V_{RWM} (V)	I_R (μA) @ V_{RWM}	V_{BR} (V) @ I_T (Note 2)	I_T	V_C (V) @ I_{PP} = 5.0 A†	V_C (V) @ Max I_{PP}†	I_{PP} (A)†	P_{pk} (W)†	C (pF)	V_C
		Max	Max	Min	mA	Typ	Max	Max	Max	Typ	Per IEC61000−4−2 (Note 3)
ESD5Z2.5T1G	ZD	2.5	6.0	4.0	1.0	6.5	10.9	11.0	120	145	Figures 1 and 2 See Below (Note 4)
ESD5Z3.3T1G	ZE	3.3	0.05	5.0	1.0	8.4	14.1	11.2	158	105	
ESD5Z5.0T1G	ZF	5.0	0.05	6.2	1.0	11.6	18.6	9.4	174	80	
ESD5Z6.0T1G	ZG	6.0	0.01	6.8	1.0	12.4	20.5	8.8	181	70	
ESD5Z7.0T1G	ZH	7.0	0.01	7.5	1.0	13.5	22.7	8.8	200	65	
ESD5Z12T1G	ZM	12	0.01	14.1	1.0	17	25	9.6	240	55	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

†Surge current waveform per Figure 5.

2. V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C.

3.ESD5Z5.0T1G shown below.

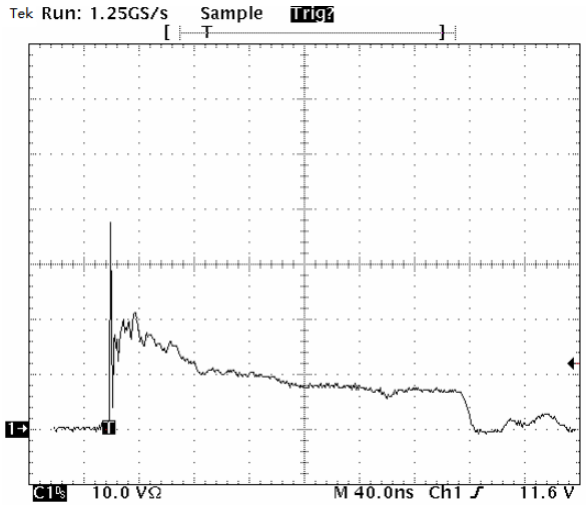


Figure 1. ESD Clamping Voltage Screenshot
Positive 8 kV contact per IEC 61000−4−2

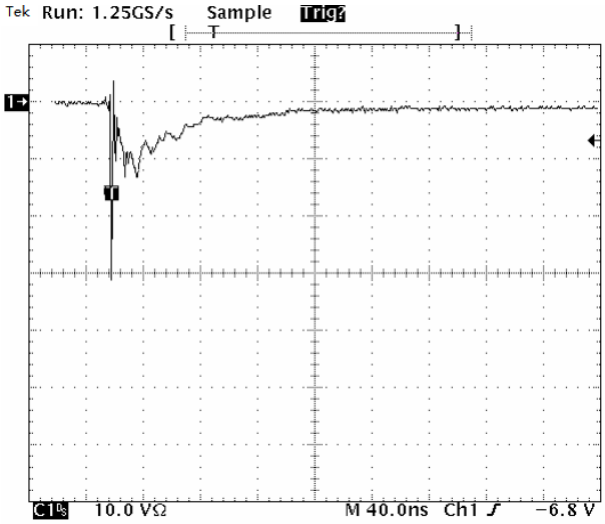


Figure 2. ESD Clamping Voltage Screenshot
Negative 8 kV contact per IEC 61000−4−2

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

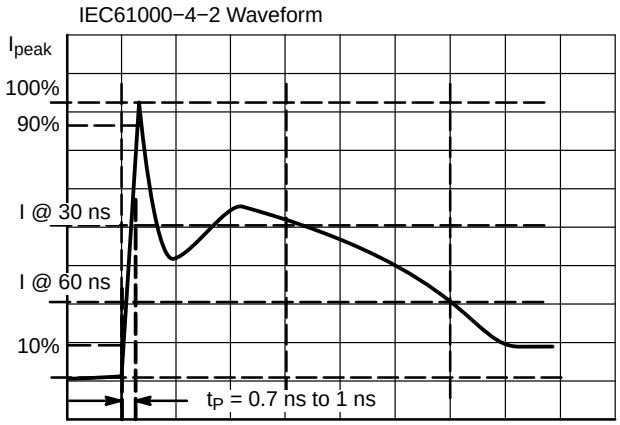


Figure 3. IEC61000−4−2 Spec

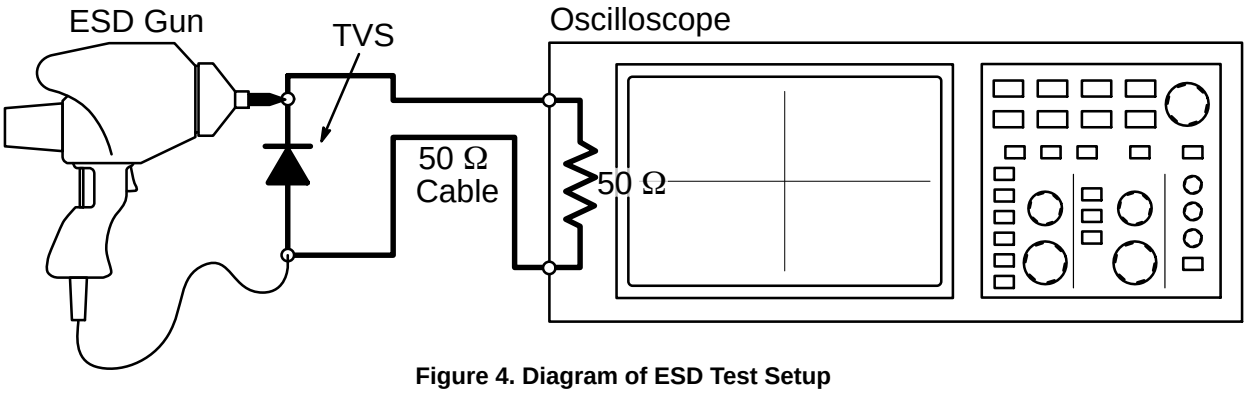


Figure 4. Diagram of ESD Test Setup

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. They has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes.

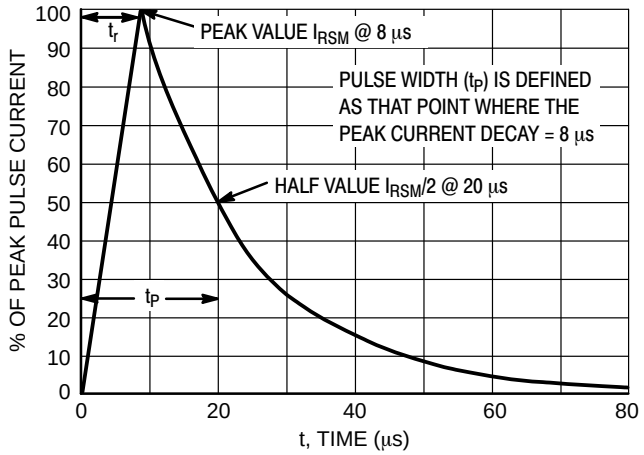
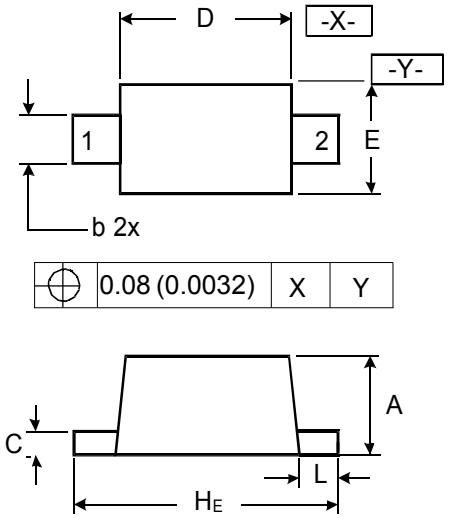


Figure 5. 8 X 20 μs Pulse Waveform

Package outline dimensions

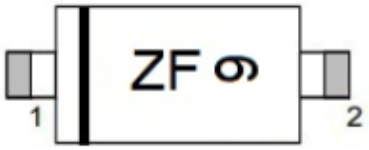
SOD-523



DIMENSIONS

SYMBOL	MILLIMETER		INCHES	
	MIN	MAX	MIN	MAX
A	0.50	0.70	0.020	0.028
b	0.25	0.35	0.010	0.014
C	0.07	0.20	0.0028	0.0079
D	1.10	1.30	0.043	0.051
E	0.70	0.90	0.028	0.035
H_E	1.50	1.70	0.059	0.067
L	0.15	0.25	0.006	0.010

Marking



Ordering information

Order code	Package	Baseqty	Delivery mode
UMW ESD5Z2.5T1G	SOD-523	3000	Tape and reel
UMW ESD5Z3.3T1G	SOD-523	3000	Tape and reel
UMW ESD5Z5.0T1G	SOD-523	3000	Tape and reel
UMW ESD5Z6.0T1G	SOD-523	3000	Tape and reel
UMW ESD5Z7.0T1G	SOD-523	3000	Tape and reel
UMW ESD5Z12T1G	SOD-523	3000	Tape and reel

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