

### General Description

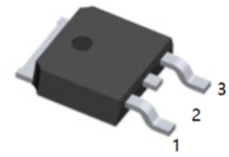
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $R_{DS(ON)}$  and fast switching speed.

### Features

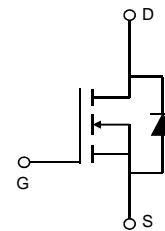
- $V_{DS} = 30V$
- $R_{DS(ON)}$  (at  $V_{GS} = 10V$ ) < 3.9m $\Omega$
- $R_{DS(ON)}$  (at  $V_{GS} = 4.5V$ ) < 4.4m $\Omega$
- High performance trench technology for extremely low  $R_{DS(ON)}$
- Low gate charge
- High power and current handling capability

### Applications

- DC/DC converters



1.G 2.D 3.S  
TO-252(DPAK) top view



### MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current		
	Continuous ( $T_C = 25^\circ C, V_{GS} = 10V$ ) (Note 1)	160	A
	Continuous ( $T_C = 25^\circ C, V_{GS} = 4.5V$ ) (Note 1)	150	A
	Continuous ( $T_{amb} = 25^\circ C, V_{GS} = 10V$ , with $R_{\theta JA} = 52^\circ C/W$ )	21	A
	Pulsed	Figure 4	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	690	mJ
$P_D$	Power dissipation	160	W
	Derate above 25 $^\circ C$	1.07	W/ $^\circ C$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to 175	$^\circ C$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-252, TO-251	0.94	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, TO-251	100	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, 1in <sup>2</sup> copper pad area	52	$^\circ C/W$

### Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$B_{VDSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	30			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}$ $V_{GS} = 0\text{V}$ $T_C = 150^\circ\text{C}$			1 250	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$			$\pm 100$	nA
$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.0	1.7	2.5	V
$R_{DS(ON)}$	Drain to Source On Resistance	$I_D = 35\text{A}, V_{GS} = 10\text{V}$		3.2	3.9	m $\Omega$
		$I_D = 35\text{A}, V_{GS} = 4.5\text{V}$		36	4.4	
$C_{ISS}$	Input Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$		5160		pF
$C_{OSS}$	Output Capacitance			990		pF
$C_{RSS}$	Reverse Transfer Capacitance			590		pF
$R_G$	Gate Resistance	$V_{GS} = 0.5\text{V}, f = 1\text{MHz}$		2.1		$\Omega$
$Q_g(TOT)$	Total Gate Charge at 10V	$V_{GS} = 0\text{V}$ to 10V	$V_{DD} = 15\text{V}$ $I_D = 35\text{A}$ $I_g = 1.0\text{mA}$	91	118	nC
$Q_g(5)$	Total Gate Charge at 5V	$V_{GS} = 0\text{V}$ to 5V		48	62	nC
$Q_g(TH)$	Threshold Gate Charge	$V_{GS} = 0\text{V}$ to 1V		5	6.5	nC
$Q_{gs}$	Gate to Source Gate Charge			14		nC
$Q_{gs2}$	Gate Charge Threshold to Plateau			9		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			18		nC
$t_{ON}$	Turn-On Time	$V_{DD} = 15\text{V}, I_D = 35\text{A}$ $V_{GS} = 10\text{V}, R_{GS} = 3.3\Omega$			139	ns
$t_{d(ON)}$	Turn-On Delay Time			9		ns
$t_r$	Rise Time			83		ns
$t_{d(OFF)}$	Turn-Off Delay Time			83		ns
$t_f$	Fall Time			42		ns
$t_{OFF}$	Turn-Off Time				189	ns
$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 35\text{A}$			1.25	V
		$I_{SD} = 15\text{A}$			1.0	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 35\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$			37	ns
$Q_{RR}$	Reverse Recovered Charge	$I_{SD} = 35\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$			21	nC

**Notes:**

1: Package current limitation is 35A.

**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted

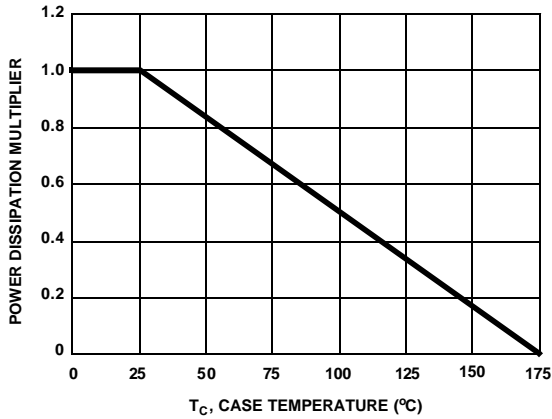


Figure 1. Normalized Power Dissipation vs Case Temperature

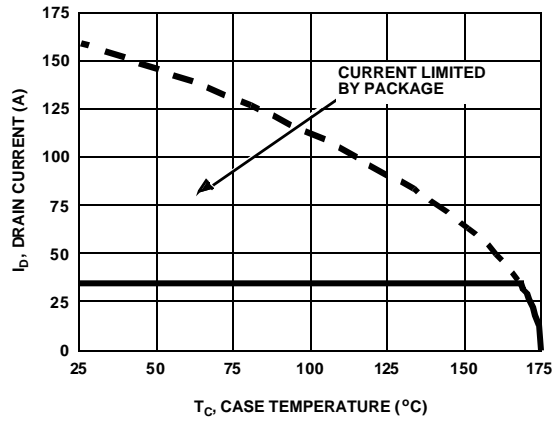


Figure 2. Maximum Continuous Drain Current vs Case Temperature

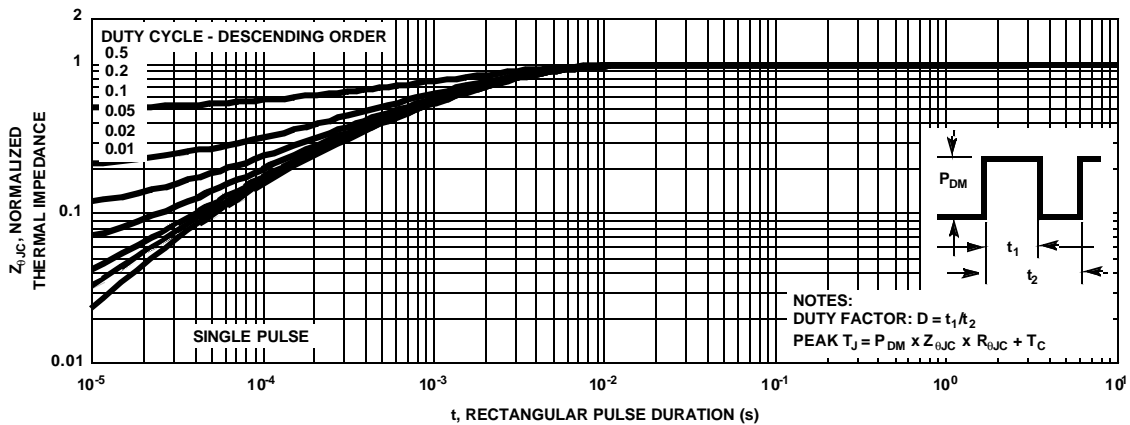


Figure 3. Normalized Maximum Transient Thermal Impedance

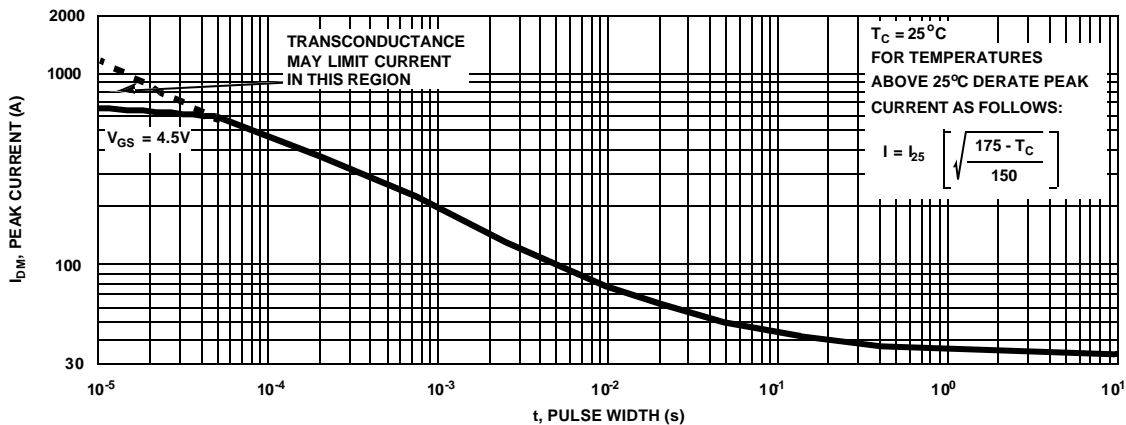


Figure 4. Peak Current Capability

Typical Characteristics  $T_C = 25^\circ\text{C}$  unless otherwise noted

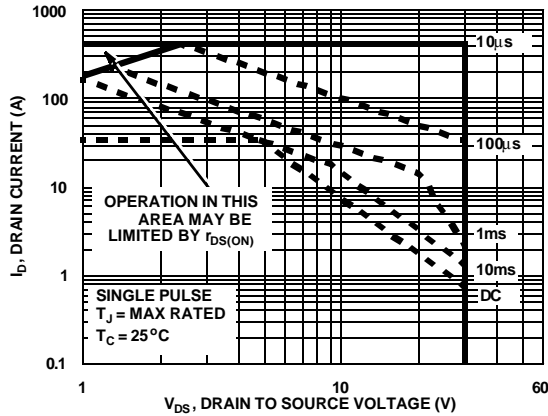
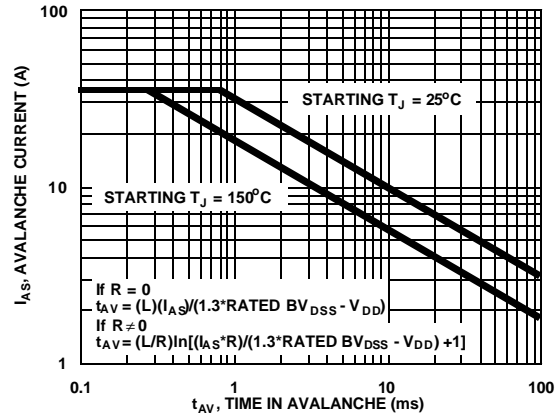


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515  
Figure 6. Unclamped Inductive Switching Capability

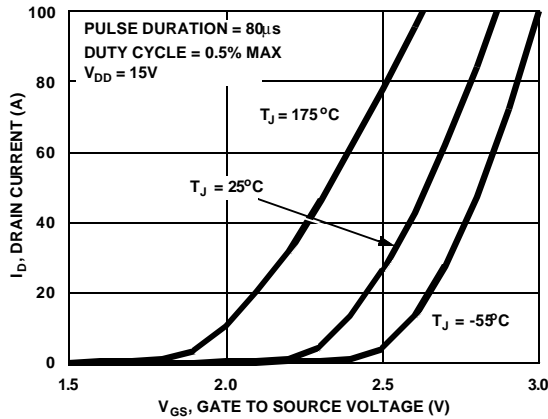


Figure 7. Transfer Characteristics

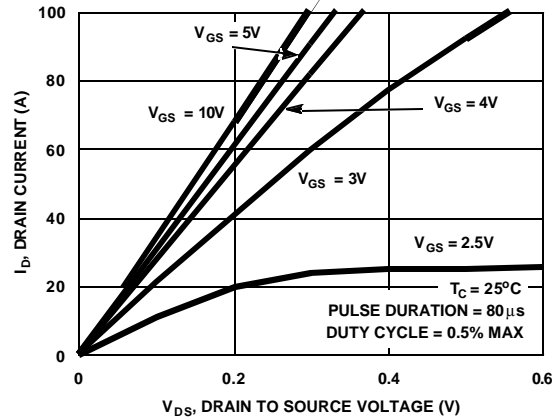


Figure 8. Saturation Characteristics

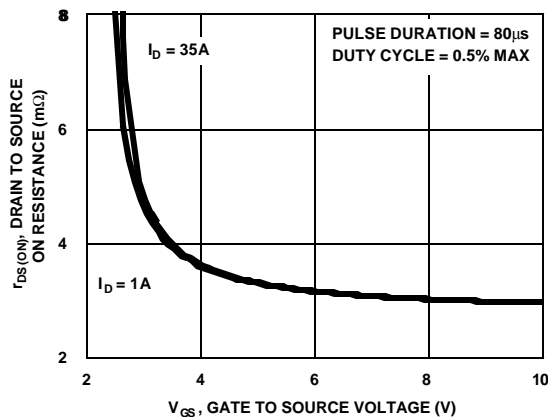


Figure 9. Drain to Source On Resistance vs Gate Voltage and Drain Current

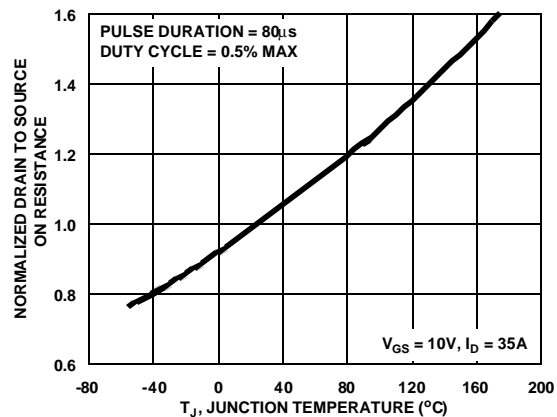
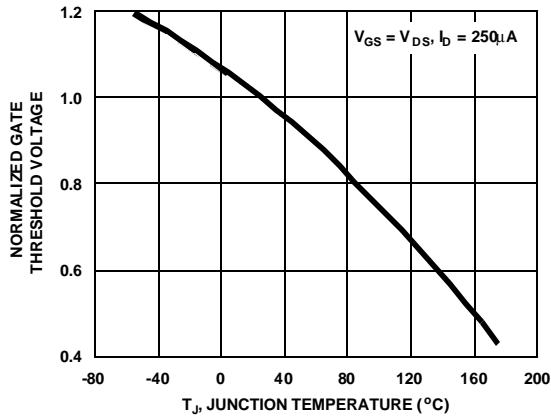
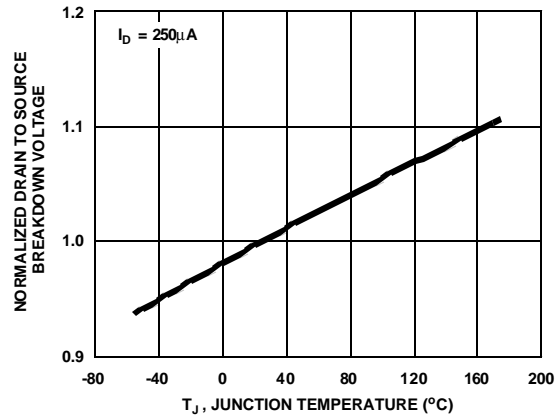


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

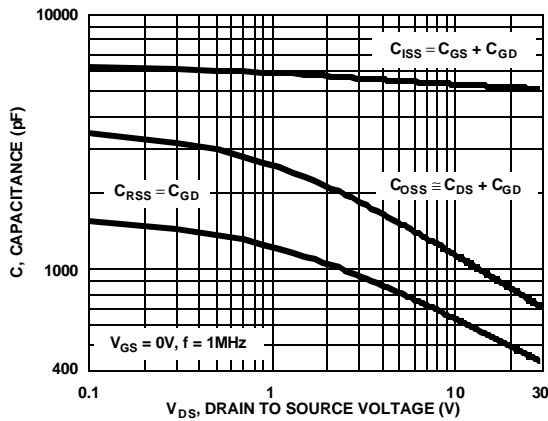
**Typical Characteristics**  $T_C = 25^\circ\text{C}$  unless otherwise noted



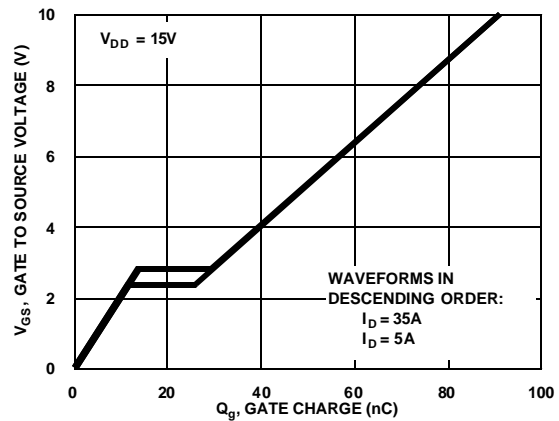
**Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature**



**Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**



**Figure 13. Capacitance vs Drain to Source Voltage**



**Figure 14. Gate Charge Waveforms for Constant Gate Current**

Test Circuits and Waveforms

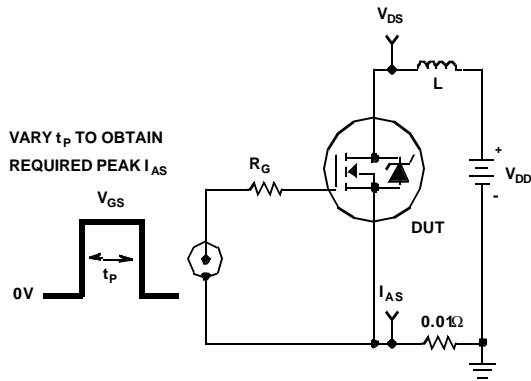


Figure 15. Unclamped Energy Test Circuit

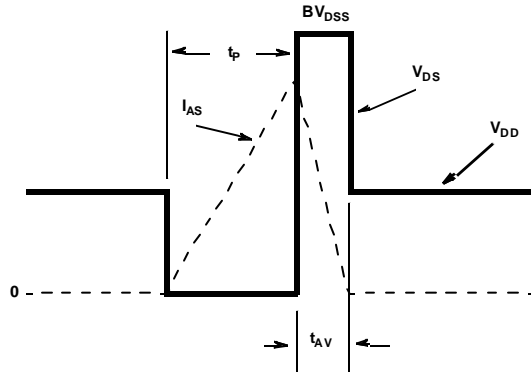


Figure 16. Unclamped Energy Waveforms

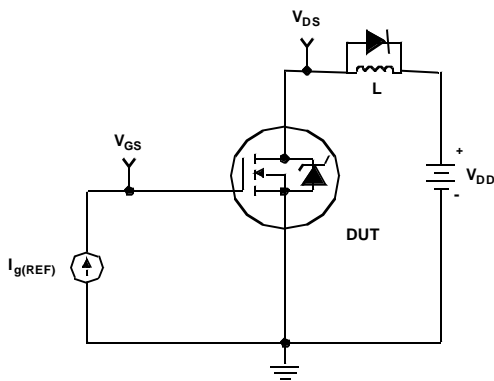


Figure 17. Gate Charge Test Circuit

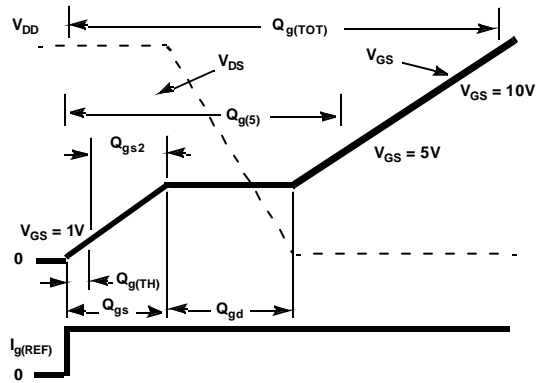


Figure 18. Gate Charge Waveforms

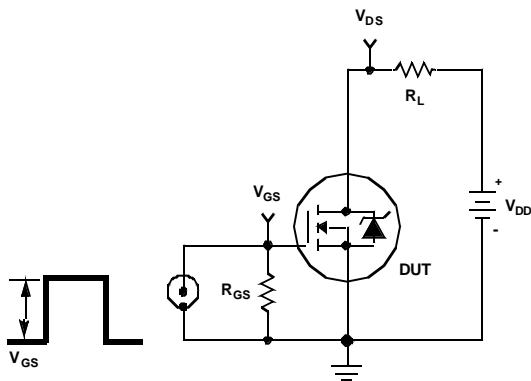


Figure 19. Switching Time Test Circuit

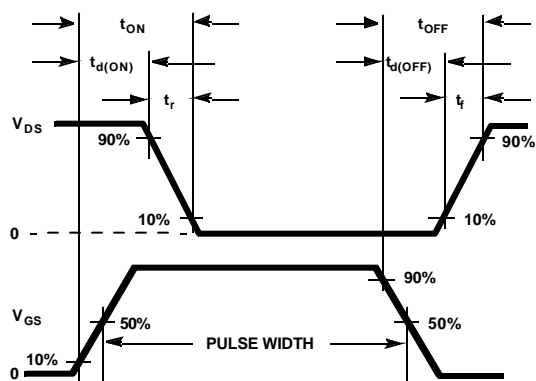


Figure 20. Switching Time Waveforms

### Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature,  $T_{JM}$ , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation,  $P_{DM}$ , in an application. Therefore the application's ambient temperature,  $T_A$  ( $^{\circ}C$ ), and thermal resistance  $R_{\theta JA}$  ( $^{\circ}C/W$ ) must be reviewed to ensure that  $T_{JM}$  is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \quad (EQ. 1)$$

In using surface mount devices such as the TO-252 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of  $P_{DM}$  is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Figure 21 defines the  $R_{\theta JA}$  for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 33.32 + \frac{23.84}{(0.268 + Area)} \quad (EQ. 2)$$

$$R_{\theta JA} = 33.32 + \frac{154}{(1.73 + Area)} \quad (EQ. 3)$$

Area in Centimeters Squared

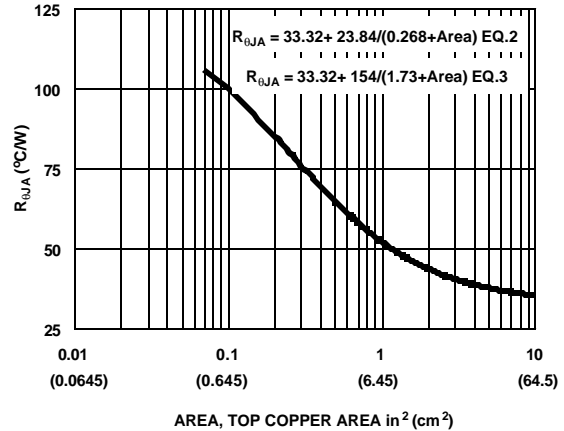
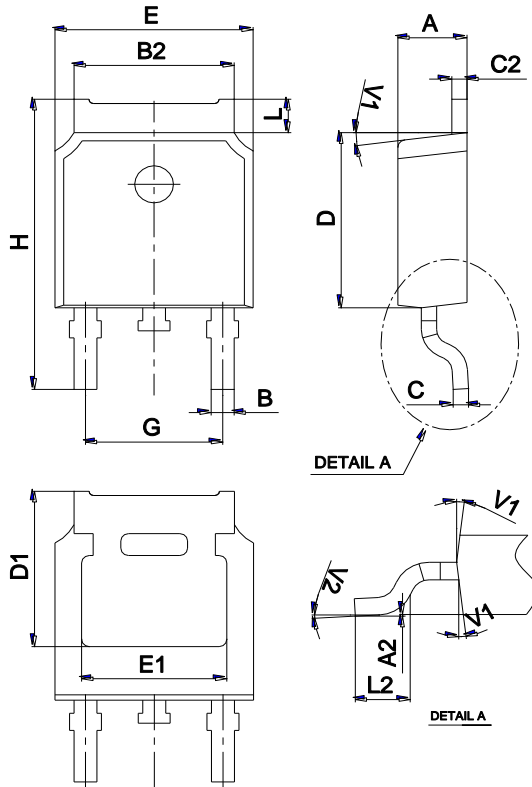


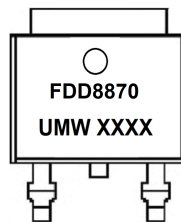
Figure 21. Thermal Resistance vs Mounting Pad Area

Package Mechanical Data TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW FDD8870	TO-252	2500	Tape and reel



## X-ON Electronics

Largest Supplier of Electrical and Electronic Components

*Click to view similar products for [MOSFET](#) category:*

*Click to view products by [Youtai](#) manufacturer:*

Other Similar products are found below :

[IRFD120](#) [JANTX2N5237](#) [2SK2267\(Q\)](#) [BUK455-60A/B](#) [TK100A10N1,S4X\(S](#) [MIC4420CM-TR](#) [VN1206L](#) [NDP4060](#) [SI4482DY](#)  
[IRS2092STRPBF-EL](#) [IPS70R2K0CEAKMA1](#) [TK31J60W5,S1VQ\(O](#) [TK31J60W,S1VQ\(O](#) [TK16J60W,S1VQ\(O](#) [2SK2614\(TE16L1,Q\)](#)  
[DMN1017UCP3-7](#) [EFC2J004NUZTDG](#) [P85W28HP2F-7071](#) [DMN1053UCP4-7](#) [NTE2384](#) [DMC2700UDMQ-7](#) [DMN2080UCB4-7](#)  
[DMN61D9UWQ-13](#) [US6M2GTR](#) [DMN31D5UDJ-7](#) [DMP22D4UFO-7B](#) [IPS60R3K4CEAKMA1](#) [DMN1006UCA6-7](#) [DMN16M9UCA6-7](#)  
[STF5N65M6](#) [IRF40H233XTMA1](#) [STU5N65M6](#) [DMN6022SSD-13](#) [DMN13M9UCA6-7](#) [DMTH10H4M6SPS-13](#) [IPS60R360PFD7SAKMA1](#)  
[DMN2990UFB-7B](#) [SSM3K35CT,L3F](#) [IPLK60R1K0PFD7ATMA1](#) [2N7002W-G](#) [MCAC30N06Y-TP](#) [IPWS65R035CFD7AXKSA1](#)  
[MCQ7328-TP](#) [SSM3J143TU,LXHF](#) [PJMF280N65E1\\_T0\\_00201](#) [PJMF380N65E1\\_T0\\_00201](#) [PJMF280N60E1\\_T0\\_00201](#)  
[PJMF600N65E1\\_T0\\_00201](#) [PJMF900N65E1\\_T0\\_00201](#) [PJMF900N60E1\\_T0\\_00201](#)