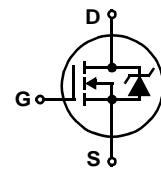**UMW**®

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

Applications

● DC/DC converters

Features

● $V_{DS} = 30V$

● $R_{DS(ON)}$ (at $V_{GS} = 10V$) < 9mΩ

● $R_{DS(ON)}$ (at $V_{GS} = 4.5V$) < 12mΩ

● High performance trench technology for extremely low $R_{DS(ON)}$

● Low gate charge

● High power and current handling capability

MOSFET Maximum Ratings T_C= 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current		
	Continuous (T_C = 25°C, V_{GS}= 10V) (Note 1)	58	A
	Continuous (T_C = 25°C, V_{GS}= 4.5V) (Note 1)	51	A
	Continuous (T_{amb} = 25°C, V_{GS}= 10V, with $R_{\theta JA}$ = 52°C/W)	13	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	53	mJ
P_D	Power dissipation	55	W
	Derate above 25°C	0 .37	W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-252	2.73	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252	100	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-252, 1in^2 copper pad area	52	°C/W

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu A$, $V_{GS} = 0V$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24V$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20V$			±100	nA
$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	1.2		2.5	V
$R_{DS(ON)}$	Drain to Source On Resistance	$I_D = 35A$, $V_{GS} = 10V$		7	9	mΩ
		$I_D = 35A$, $V_{GS} = 4.5V$		9	12	
C_{ISS}	Input Capacitance	$V_{DS} = 15V$, $V_{GS} = 0V$, f = 1MHz		1260		pF
C_{OSS}	Output Capacitance			260		pF
C_{RSS}	Reverse Transfer Capacitance			150		pF
R_G	Gate Resistance	$V_{GS} = 0.5V$, f = 1MHz		2.3		Ω
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0V$ to 10V		23	31	nC
$Q_{g(5)}$	Total Gate Charge at 5V	$V_{GS} = 0V$ to 5V		13	17	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0V$ to 1V, $V_{DD} = 15V$, $I_D = 35A$, $I_g = 1.0mA$		1.3	1.7	nC
Q_{gs}	Gate to Source Gate Charge			3.8		nC
Q_{gs2}	Gate Charge Threshold to Plateau			2.5		nC
Q_{gd}	Gate to Drain "Miller" Charge			5.0		nC
t_{ON}	Turn-On Time	$V_{DD} = 15V$, $I_D = 35A$, $V_{GS} = 10V$, $R_{GS} = 10\Omega$			147	ns
$t_{d(ON)}$	Turn-On Delay Time			8		ns
t_r	Rise Time			91		ns
$t_{d(OFF)}$	Turn-Off Delay Time			38		ns
t_f	Fall Time			32		ns
t_{OFF}	Turn-Off Time				108	ns
V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 35A$			1.25	V
		$I_{SD} = 15A$			1.0	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 35A$, $dI_{SD}/dt = 100A/\mu s$			27	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD} = 35A$, $dI_{SD}/dt = 100A/\mu s$			14	nC

Notes:
1: Package current limitation is 35A.
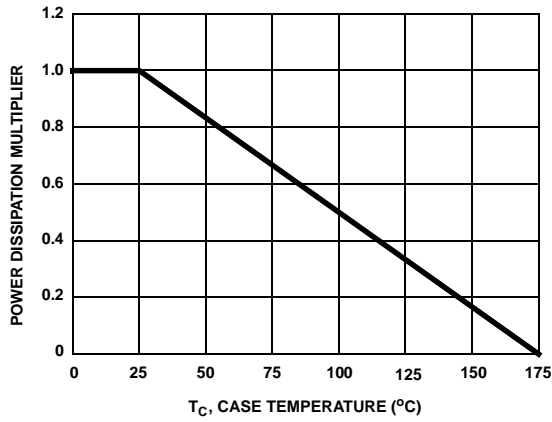
Typical Characteristics T_C = 25°C unless otherwise noted

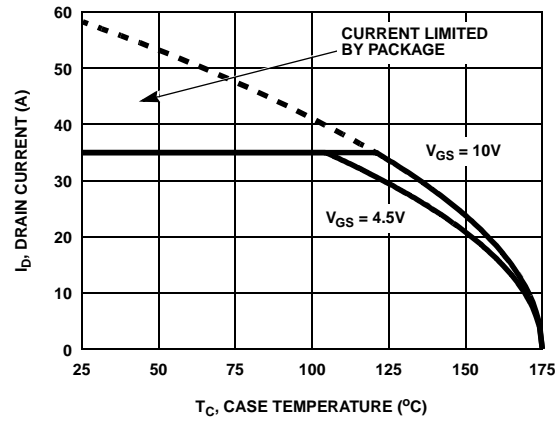**Figure 1. Normalized Power Dissipation vs Case Temperature**

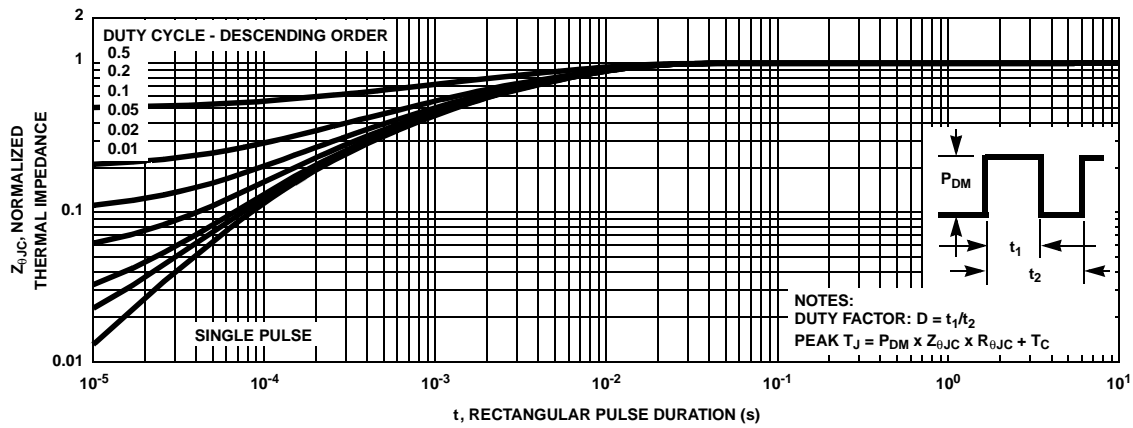**Figure 2. Maximum Continuous Drain Current vs Case Temperature**

NOTES:
DUTY FACTOR: $D = t_1/t_2$
PEAK $T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C$

Figure 3. Normalized Maximum Transient Thermal Impedance

$T_C = 25°C$
FOR TEMPERATURES
ABOVE 25°C DERATE PEAK
CURRENT AS FOLLOWS:

$$I = I_{25} \sqrt{\frac{175 - T_C}{150}}$$

Figure 4. Peak Current Capability

Typical Characteristics T_C = 25°C unless otherwise noted

Figure 5. Forward Bias Safe Operating Area

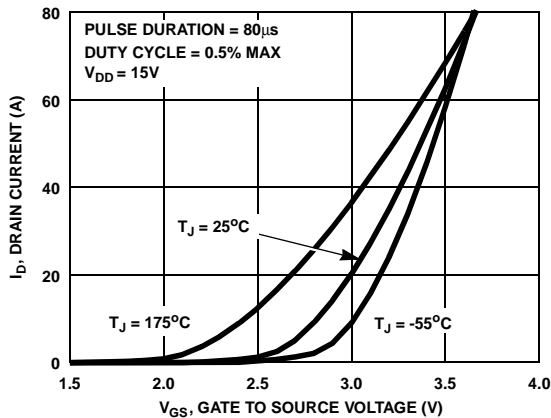Figure 6. Unclamped Inductive Switching Capability
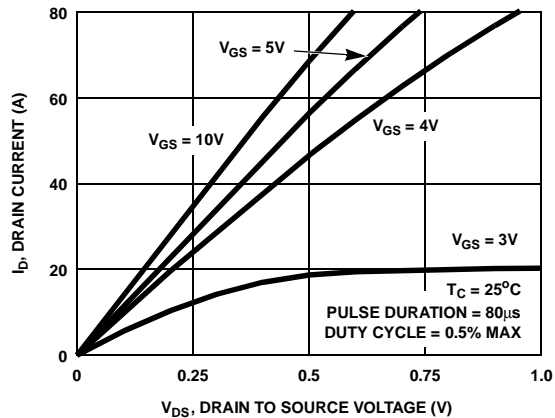

Figure 7. Transfer Characteristics

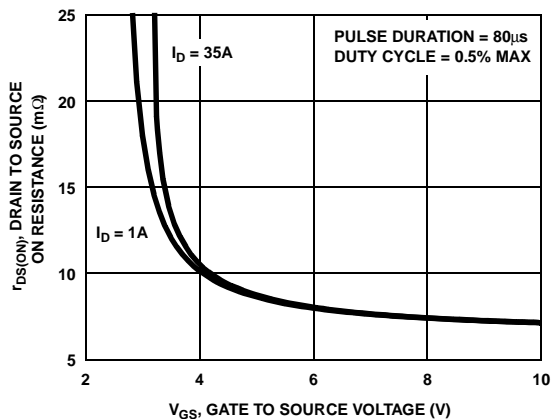Figure 8. Saturation Characteristics

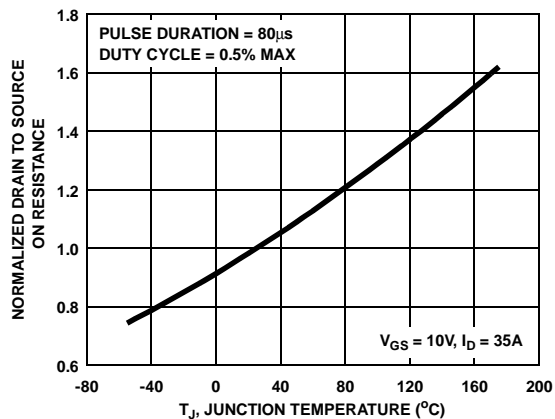Figure 9. Drain to Source On Resistance vs Gate Voltage and Drain Current

Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

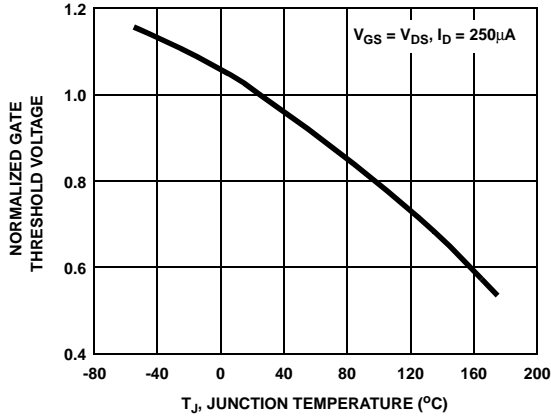**Typical Characteristics** T_C = 25°C unless otherwise noted

Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature
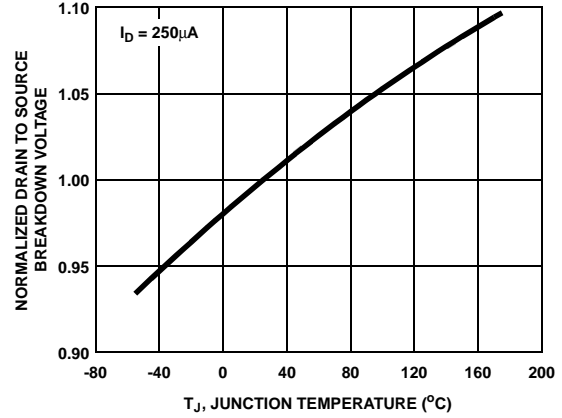

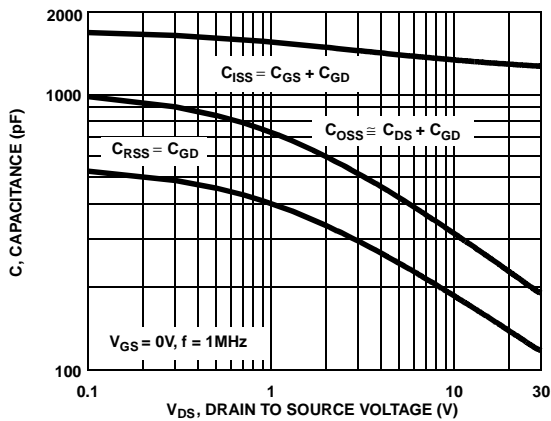**Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature**
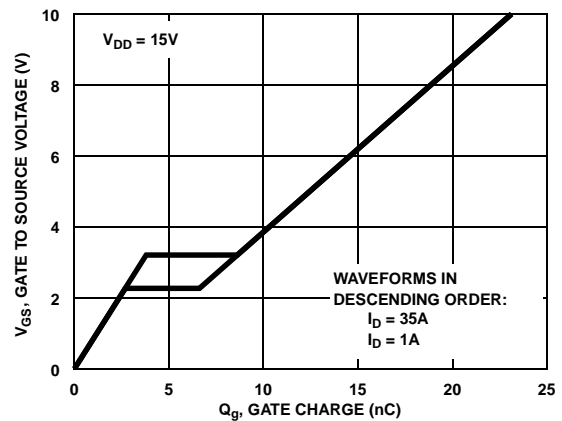

Figure 13. Capacitance vs Drain to Source Voltage

Figure 14. Gate Charge Waveforms for Constant Gate Current
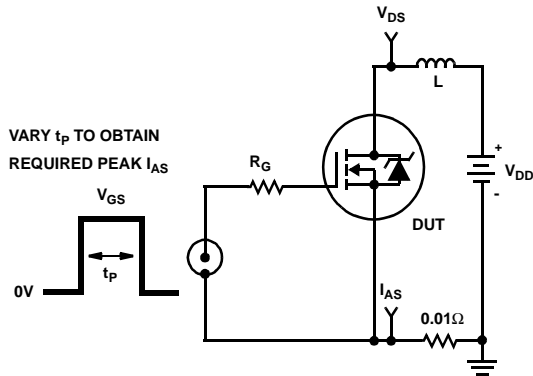
Test Circuits and Waveforms

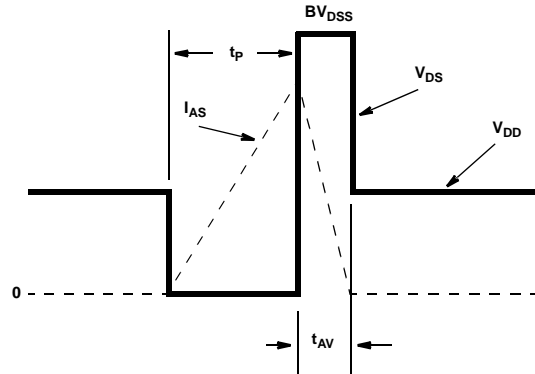**Figure 15. Unclamped Energy Test Circuit**
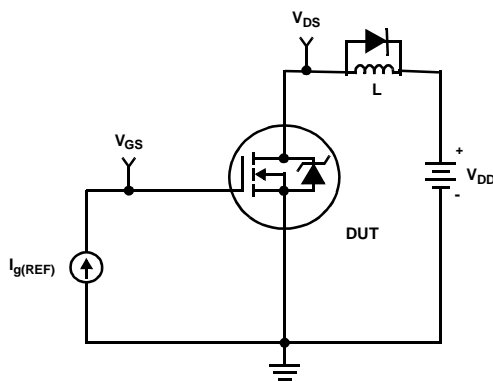

Figure 16. Unclamped Energy Waveforms

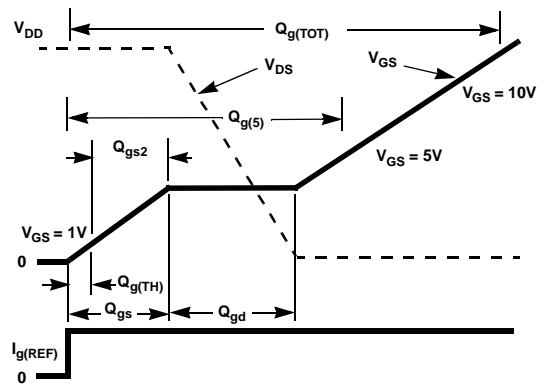**Figure 17. Gate Charge Test Circuit**

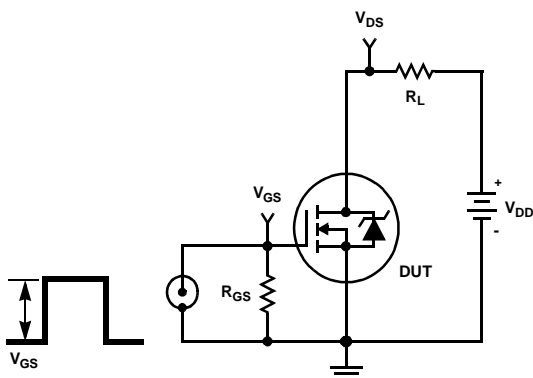

Figure 18. Gate Charge Waveforms

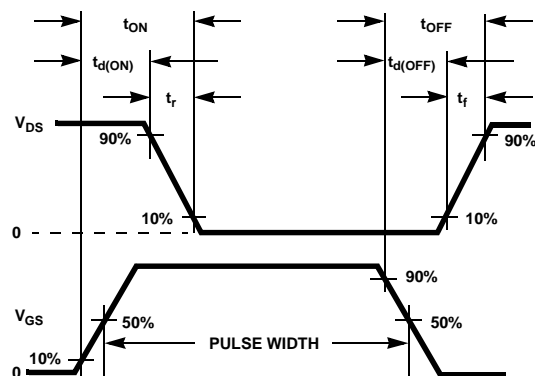**Figure 19. Switching Time Test Circuit**

Figure 20. Switching Time Waveforms

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (^oC), and thermal resistance $R_{\theta JA}$ ($^oC/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}}$$ (EQ. 1)

In using surface mount devices such as the TO-252 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.

2. The number of copper layers and the thickness of the board.

3. The use of external heat sinks.

4. The use of thermal vias.

5. Air flow and board orientation.

6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Figure 21 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeters square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{\theta JA} = 33.32 + \frac{23.84}{(0.268 + Area)}$$ (EQ. 2)

Area in Inches Squared

$$R_{\theta JA} = 33.32 + \frac{154}{(1.73 + Area)}$$ (EQ. 3)
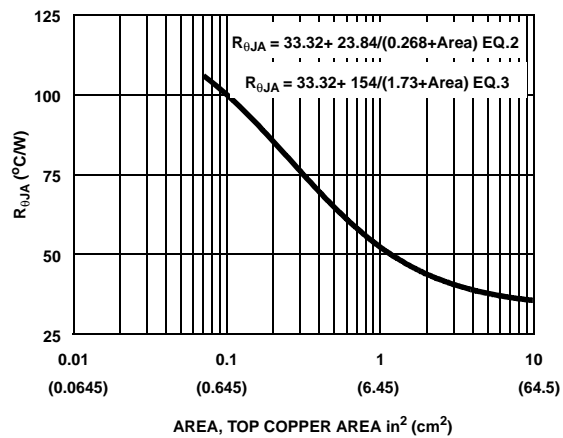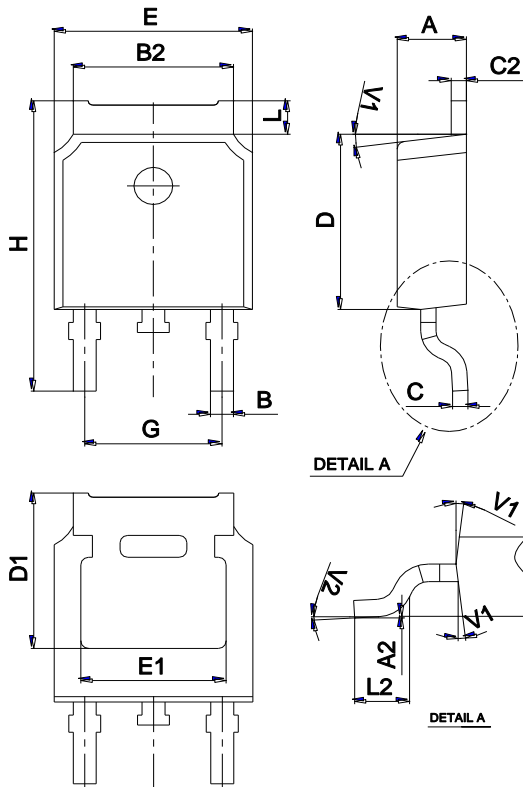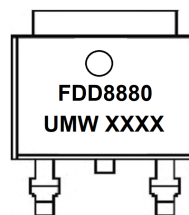
Area in Centimeters Squared

Figure 21. Thermal Resistance vs Mounting Pad Area

Package Mechanical Data TO-252

DETAIL A

DETAIL A

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1		5.30REF			0.209REF	
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Marking

FDD8880
UMW XXXX

Ordering information

Order code	Package	Baseqty	Deliverymode
UMW FDD8880	TO-252	2500	Tape and reel

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DMN1017UCP3-7 EFC2J004NUZTDG P85W28HP2F-7071 DMN1053UCP4-7 NTE2384 DMC2700UDMQ-7 DMN2080UCB4-7

DMN61D9UWQ-13 US6M2GTR DMN31D5UDJ-7 DMP22D4UFO-7B IPS60R3K4CEAKMA1 DMN1006UCA6-7 DMN16M9UCA6-7

STF5N65M6 IRF40H233XTMA1 STU5N65M6 DMN6022SSD-13 DMN13M9UCA6-7 DMTH10H4M6SPS-13 IPS60R360PFD7SAKMA1

DMN2990UFB-7B SSM3K35CT,L3F IPLK60R1K0PFD7ATMA1 2N7002W-G MCAC30N06Y-TP IPWS65R035CFD7AXKSA1

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