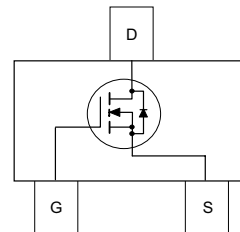
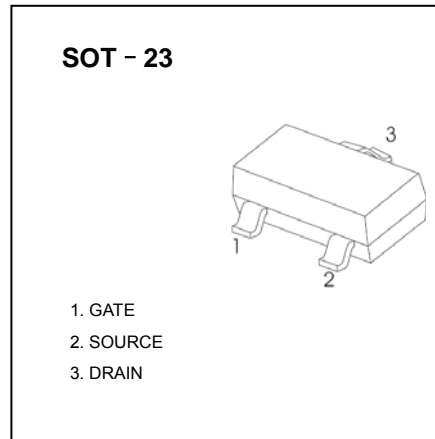


General Description

These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package. [®]

Features

- V_{DS} (V) = 30V
- R_{DS(ON)} <110mΩ (V_{GS} = 10V)
- R_{DS(ON)} <160mΩ (V_{GS} = 4.5V)



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	Drain-Source Voltage	30	V
V _{GSS}	Gate-Source Voltage	± 20	V
I _D	Drain Current – Continuous (Note 1a)	1.4	A
	– Pulsed	10	
P _D	Power Dissipation for Single Operation (Note 1a) (Note 1b)	0.5	W
		0.46	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C
Thermal Characteristics			
R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case (Note 1)	75	

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		26		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			10	μA
I_{GSS}	Gate–Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	2.1	3	V
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}, I_D = 1.4\text{ A}$		92	110	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 1.2\text{ A}$		120	160	
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	3.5			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 1.4\text{ A}$		4		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$		145	193	pF
C_{oss}	Output Capacitance			35	47	
C_{rss}	Reverse Transfer Capacitance			15	23	
R_G	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		1.6		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A}, V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		3	6	ns
t_r	Turn–On Rise Time			8	16	
$t_{d(off)}$	Turn–Off Delay Time			16	29	
t_f	Turn–Off Fall Time			2	4	
Q_g	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 1.4\text{ A}, V_{GS} = 4.5\text{ V}$		1.3	1.8	nC
Q_{gs}	Gate–Source Charge			0.5		
Q_{gd}	Gate–Drain Charge			0.5		
Drain–Source Diode Characteristics						
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.42\text{ A}$ (Note 2)		0.8	1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = 1.4\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$		11	22	nS
Q_{rr}	Diode Reverse Recovery Charge			4		

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 250°C/W when mounted on a 0.02 in^2 pad of 2 oz. copper.



b) 270°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$

Typical Characteristics

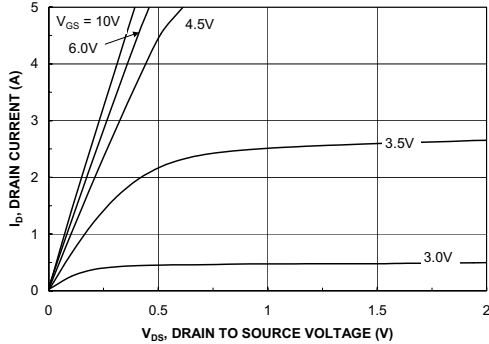


Figure 1. On-Region Characteristics.

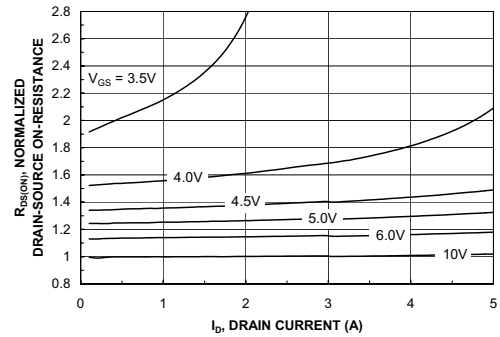


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

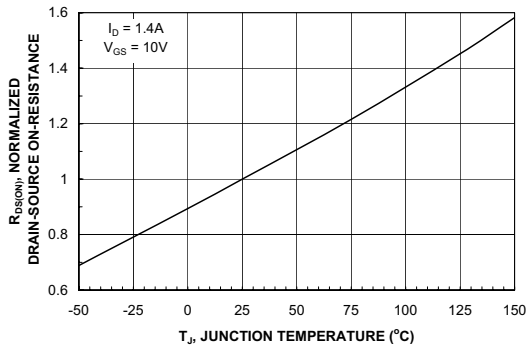


Figure 3. On-Resistance Variation with Temperature.

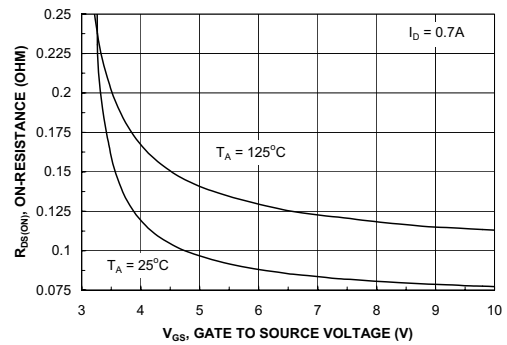


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

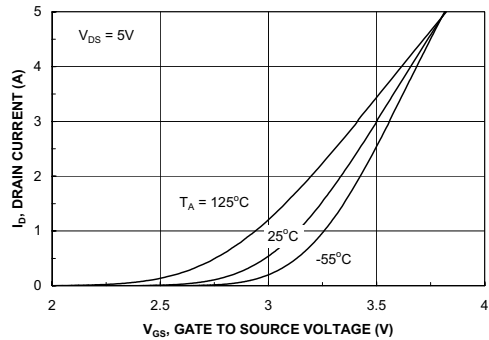


Figure 5. Transfer Characteristics.

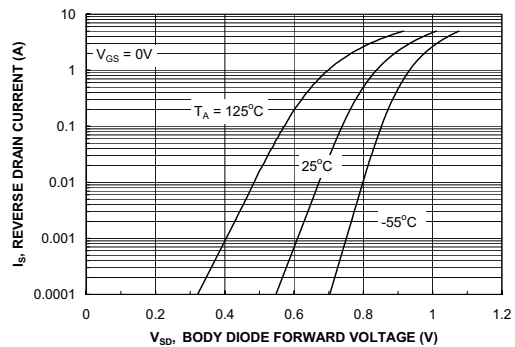


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

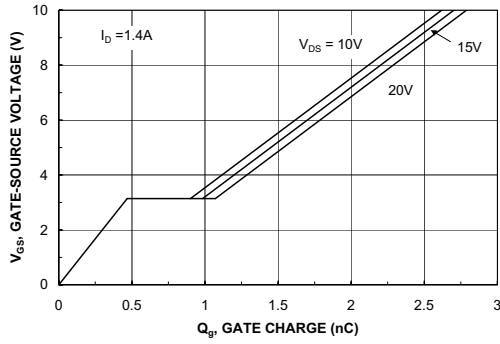


Figure 7. Gate Charge Characteristics.

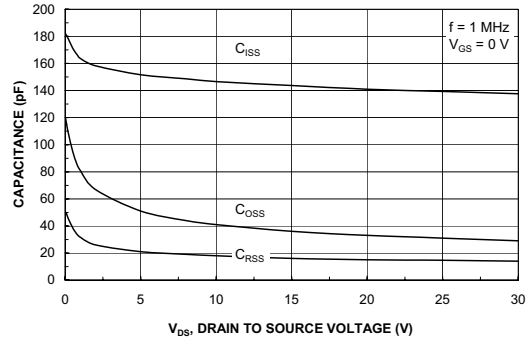


Figure 8. Capacitance Characteristics.

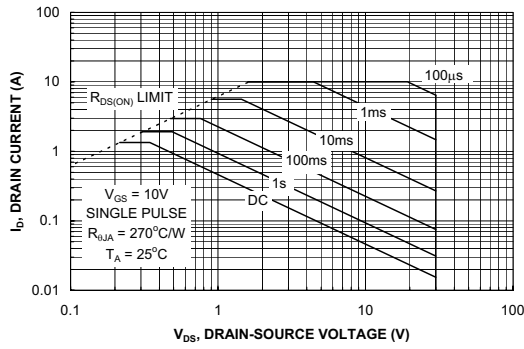


Figure 9. Maximum Safe Operating Area.

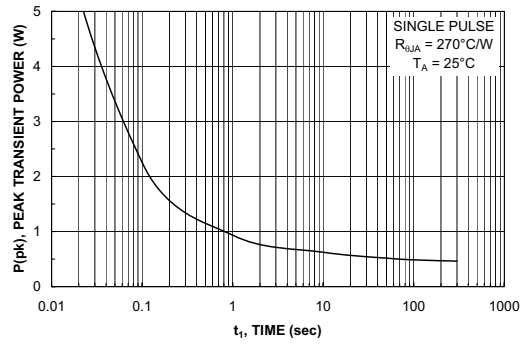


Figure 10. Single Pulse Maximum Power Dissipation.

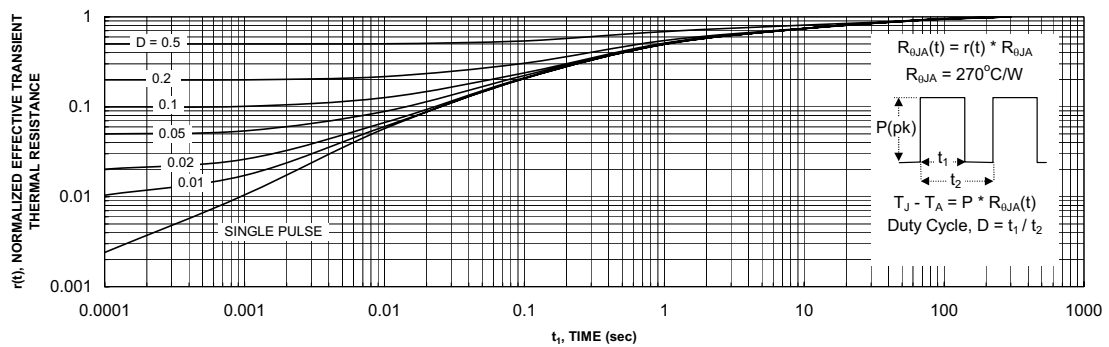
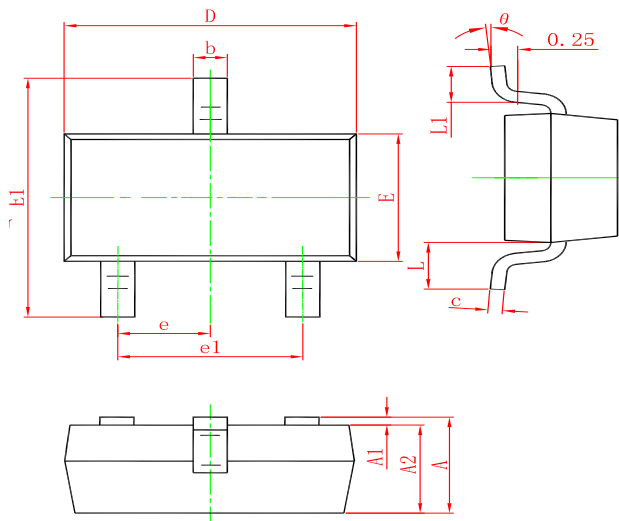


Figure 11. Transient Thermal Response Curve.

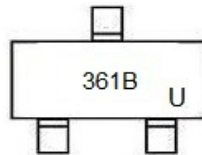
Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

SOT-23 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.550 REF.		0.022 REF.	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
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