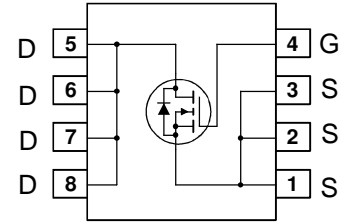


### Features

- $V_{DS(V)} = 30V$
- $I_D = 11 A$  ( $V_{GS} = 10V$ )
- $R_{DS(ON)} < 12.5m\Omega$  ( $V_{GS}=10V$ )
- $R_{DS(ON)} < 17m\Omega$  ( $V_{GS}=4.5V$ )
- Fast switching speed
- Low gate charge
- High performance trench technology for extremely low  $R_{DS(ON)}$
- High power and current handling capability



### Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Drain Current – Continuous (Note 1a) – Pulsed	11	A
		50	
$P_D$	Power Dissipation for Single Operation (Note 1a) (Note 1b)	2.5	W
		1.0	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	96	mJ
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ C$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	125	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	

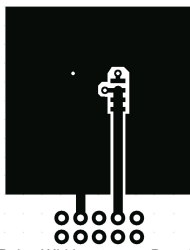
### Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		25		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			1 10	$\mu\text{A}$
$I_{GSS}$	Gate–Body Leakage	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-5		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}, I_D = 11\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		9.8 12.0	12.5 17.0	m $\Omega$
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	50			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 11\text{ A}$		48		S
$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		1205		pF
$C_{oss}$	Output Capacitance			290		pF
$C_{rss}$	Reverse Transfer Capacitance			115		pF
$R_G$	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		2.4		$\Omega$
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		9	19	ns
$t_r$	Turn–On Rise Time			5	10	ns
$t_{d(off)}$	Turn–Off Delay Time			28	44	ns
$t_f$	Turn–Off Fall Time			9	19	ns
$Q_g$	Total Gate Charge		$V_{DS} = 15\text{ V}, I_D = 11\text{ A},$ $V_{GS} = 5\text{ V}$		12	16
$Q_{gs}$	Gate–Source Charge			3.4		nC
$Q_{gd}$	Gate–Drain Charge			4.0		nC
$I_S$	Maximum Continuous Drain–Source Diode Forward Current				2.1	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.1\text{ A}$ (Note 2)		0.74	1.2	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 11\text{ A}, d_F/d_i = 100\text{ A}/\mu\text{s}$		24		nS
$Q_{rr}$	Diode Reverse Recovery Charge			27		nC

#### Notes:

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $50^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



b)  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2 Test: Pulse Width <  $300\ \mu\text{s}$ , Duty Cycle < 2.0%

3. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 8\text{ A}$ ,  $V_{DD} = 30\text{ V}$ ,  $V_{GS} = 10\text{ V}$

Typical Characteristics

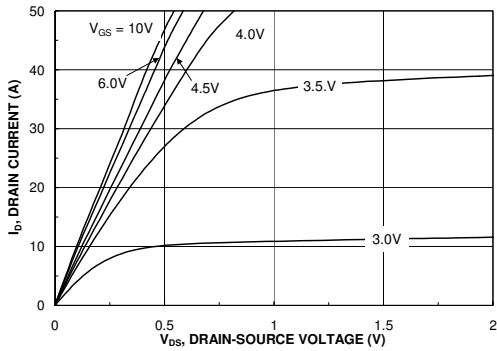


Figure 1. On-Region Characteristics.

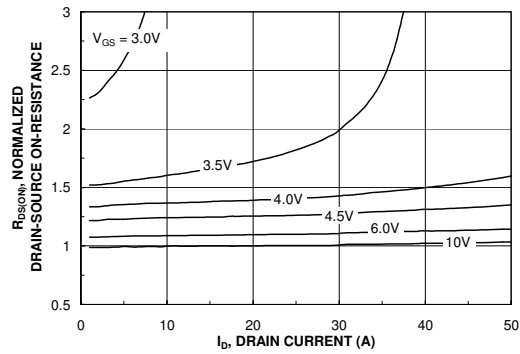


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

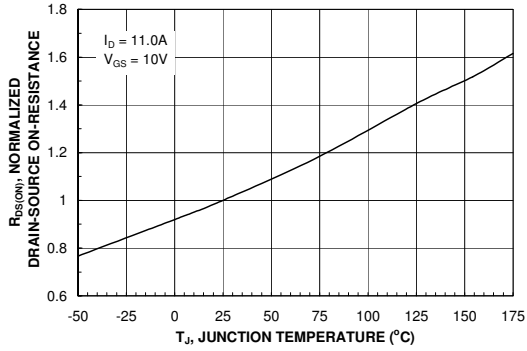


Figure 3. On-Resistance Variation with Temperature.

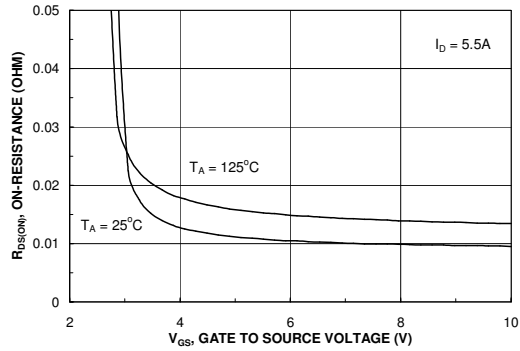


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

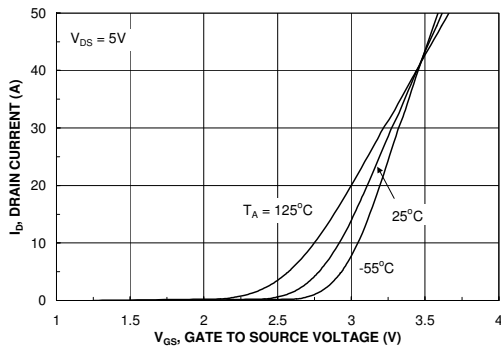


Figure 5. Transfer Characteristics.

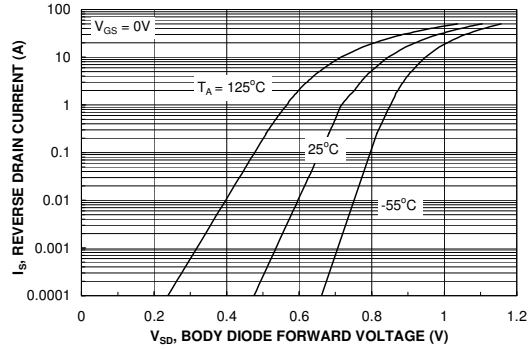


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

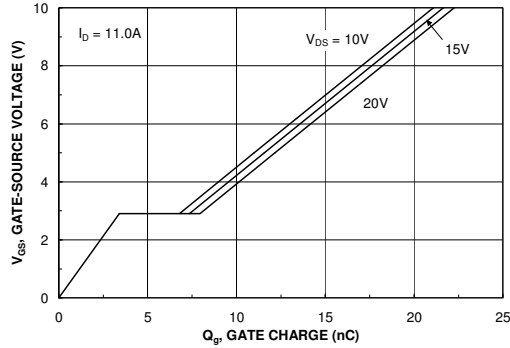


Figure 7. Gate Charge Characteristics.

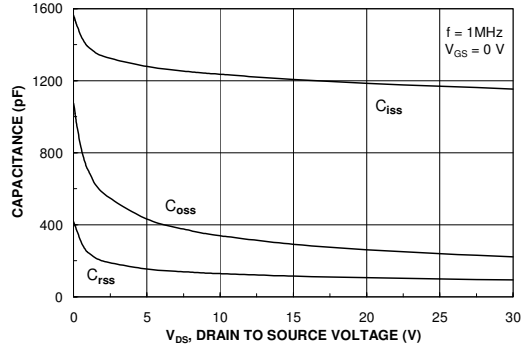


Figure 8. Capacitance Characteristics.

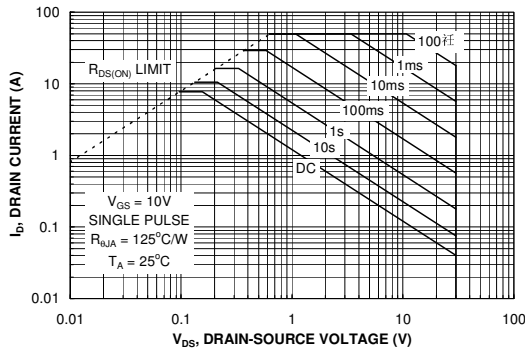


Figure 9. Maximum Safe Operating Area.

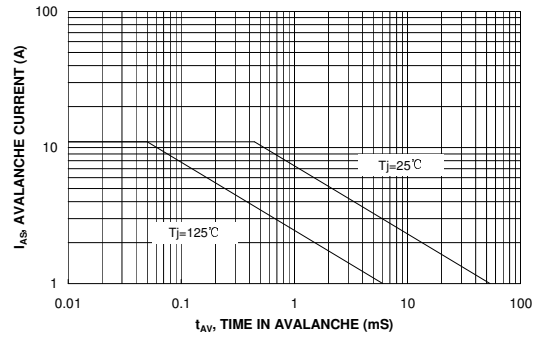


Figure 10. Unclamped Inductive Switching Capability Figure

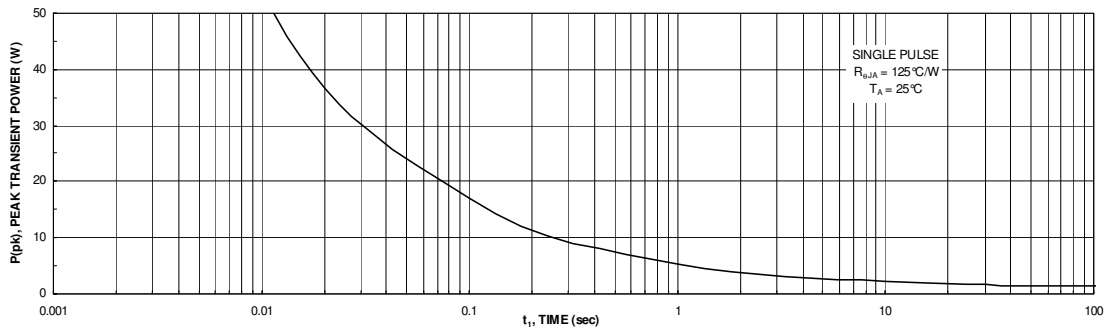
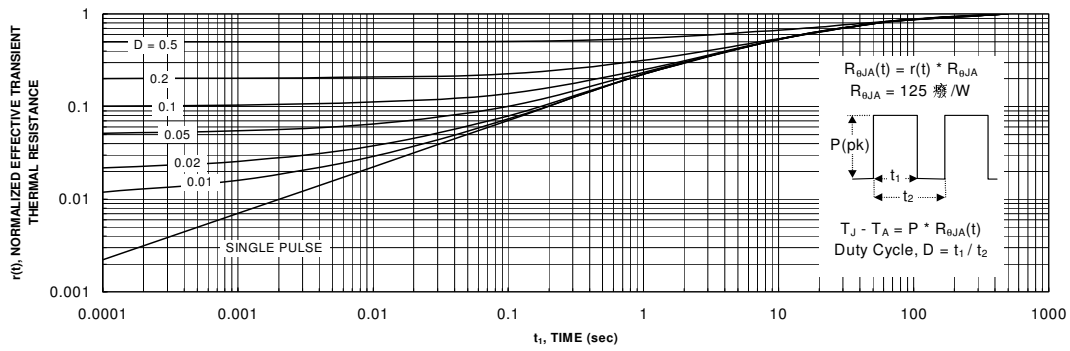


Figure 11. Single Pulse Maximum Power Dissipation.

Typical Characteristic

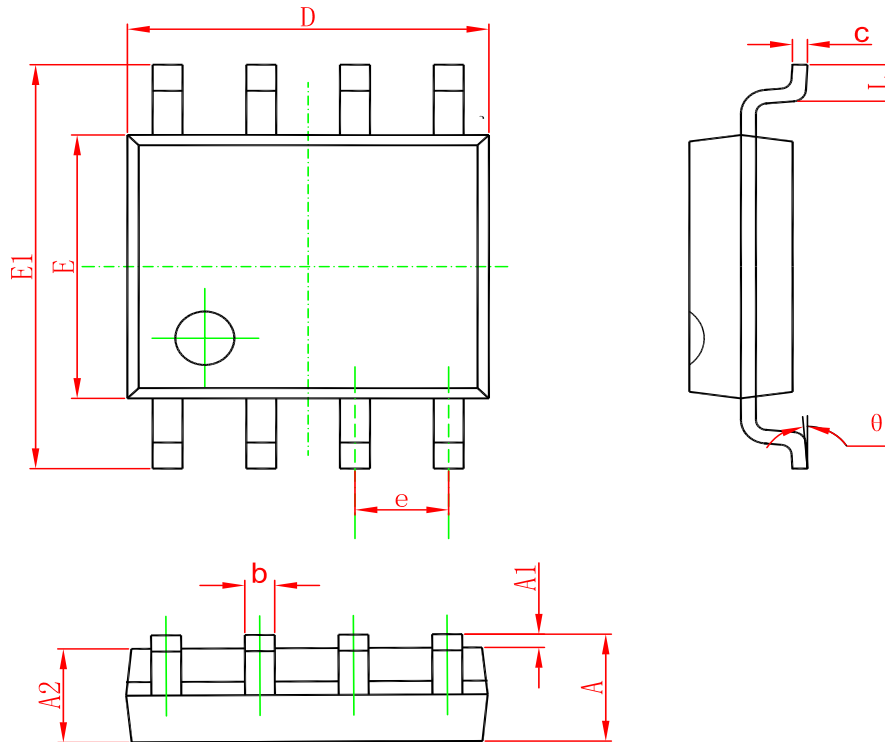


**Figure 12. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c.  
Transient thermal response will change depending on the circuit board design.

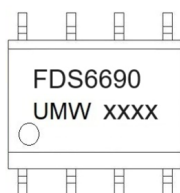
PACKAGE OUTLINE DIMENSIONS

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

## Marking



## Ordering information

Order code	Package	Baseqty	Deliverymode
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