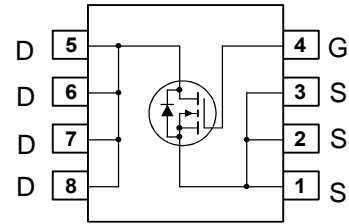


General Descriptions

This N-channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$ and fast switching speed.



Features

- $V_{DS(V)} = 30V$
- $I_D = 8.5 A$ ($V_{GS} = 10V$)
- $R_{DS(ON)} < 23m\Omega$ ($V_{GS}=10V$)
- $R_{DS(ON)} < 30 m\Omega$ ($V_{GS}=4.5V$)
- Low gate charge

MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current Continuous (Note 1a)	8.5	A
	Pulsed	40	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	32	mJ
P_D	Power dissipation	2.5	W
	Derate above $25^\circ C$	20	mW/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	$^\circ C$

Thermal Characteristics

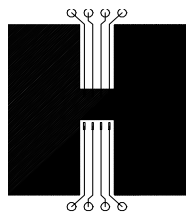
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Case (Note 1)	25	$^\circ C/W$

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

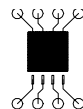
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		23		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}$ $V_{GS} = 0\text{V}$ $T_J = 125^\circ\text{C}$			1 250	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	1.2	1.7	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C		-4.9		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 8.5\text{A}$,		19	23	m Ω
		$V_{GS} = 4.5\text{V}$, $I_D = 7.5\text{A}$,		23	30	
		$V_{GS} = 10\text{V}$, $I_D = 8.5\text{A}$, $T_J = 125^\circ\text{C}$		26	32	
C_{iss}	Input Capacitance	$V_{DS} = 15\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$		475	635	pF
C_{oss}	Output Capacitance			100	135	pF
C_{rss}	Reverse Transfer Capacitance			65	100	pF
R_G	Gate Resistance		$f = 1\text{MHz}$		0.9	1.6
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{V}$, $I_D = 8.5\text{A}$ $V_{GS} = 10\text{V}$, $R_{GS} = 33\Omega$		5	10	ns
t_r	Rise Time			9	18	ns
$t_{d(off)}$	Turn-Off Delay Time			42	68	ns
t_f	Fall Time			21	34	ns
Q_g	Total Gate Charge		$V_{DS} = 15\text{V}$, $V_{GS} = 10\text{V}$ $I_D = 8.5\text{A}$		9.2	13
Q_g	Total Gate Charge	$V_{DS} = 15\text{V}$, $V_{GS} = 5\text{V}$ $I_D = 8.5\text{A}$		5.0	7	nC
Q_{gs}	Gate to Source Gate Charge			1.5		nC
Q_{gd}	Gate to Drain Charge			2.0		nC
V_{SD}	Source to Drain Diode Voltage		$I_{SD} = 8.5\text{A}$		0.9	1.25
		$I_{SD} = 2.1\text{A}$		0.8	1.0	V
t_{rr}	Reverse Recovery Time	$I_F = 8.5\text{A}$, $di/dt = 100\text{A}/\mu\text{s}$			33	ns
Q_{rr}	Reverse Recovery Charge				20	nC

Notes:

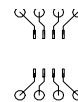
1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1 in² pad of 2 oz copper



b) 105°C/W when mounted on a .04 in² pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad

Scale 1 : 1 on letter size paper

2: Starting $T_J = 25^\circ\text{C}$, $L = 1\text{mH}$, $I_{AS} = 8\text{A}$, $V_{DD} = 27\text{V}$, $V_{GS} = 10\text{V}$.
 3: Pulse Test: Pulse Width <300 μs , Duty Cycle <2%.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

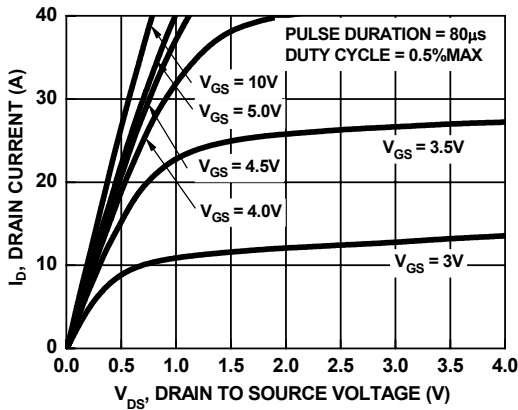


Figure 1. On Region Characteristics

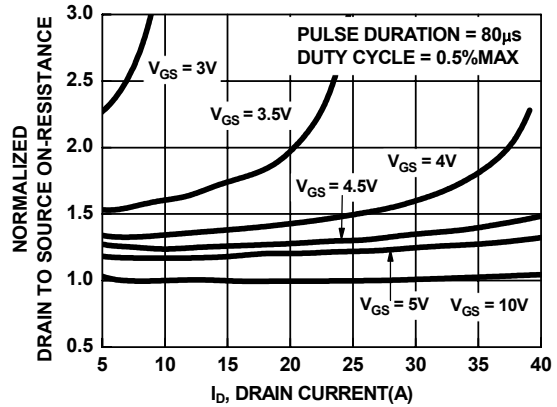


Figure 2. Normalized On-Resistance vs Drain current and Gate Voltage

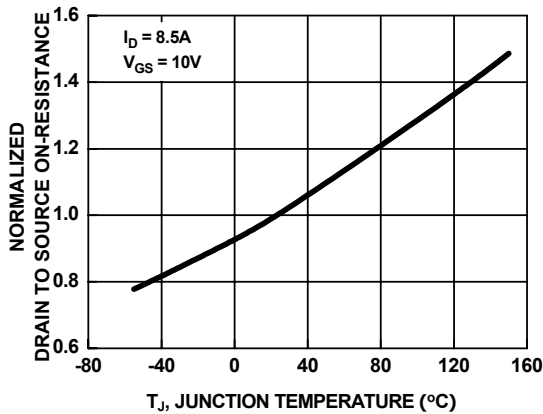


Figure 3. Normalized On Resistance vs Junction Temperature

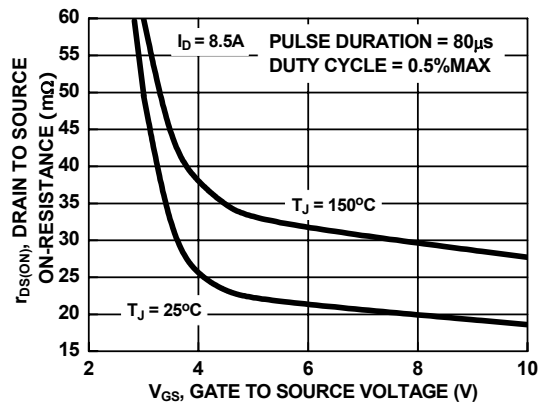


Figure 4. On-Resistance vs Gate to Source Voltage

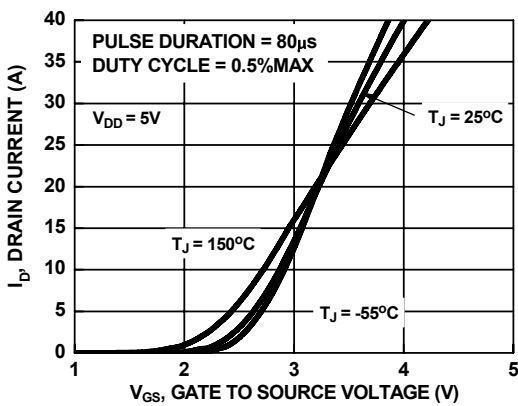


Figure 5. Transfer Characteristics

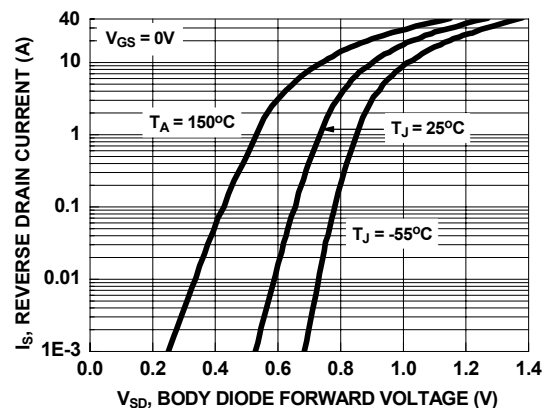


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

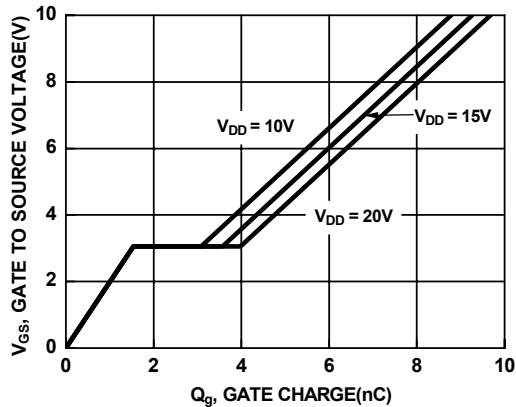


Figure 7. Gate Charge Characteristics

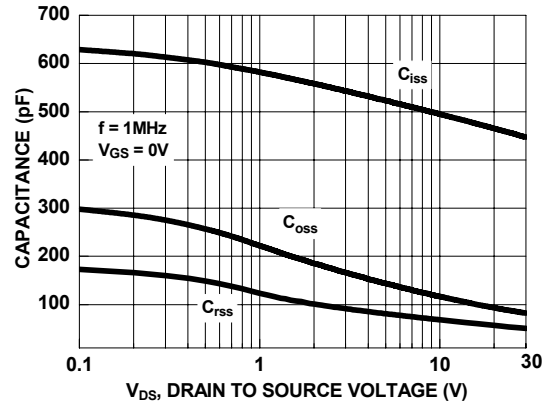


Figure 8. Capacitance vs Drain to Source Voltage

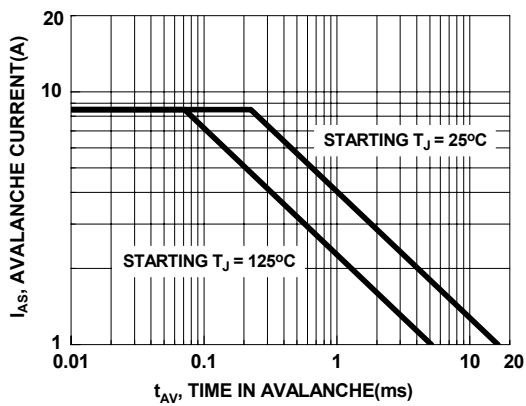


Figure 9. Unclamped Inductive Switching Capability

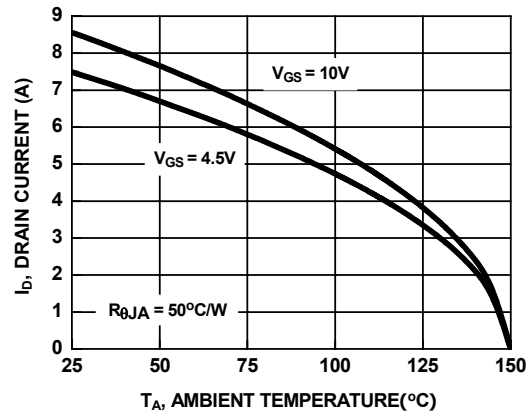


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

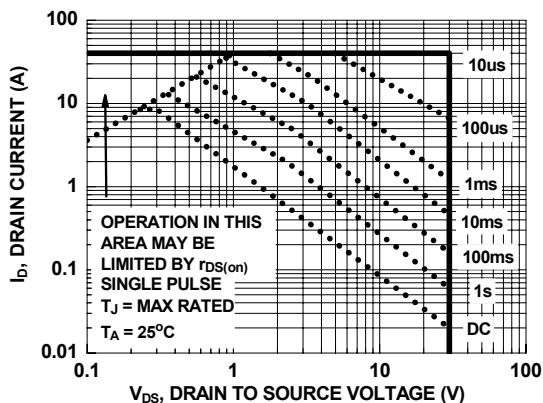


Figure 11. Forward Bias Safe Operating Area

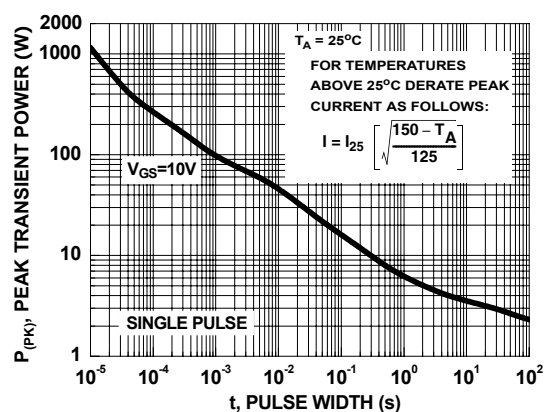
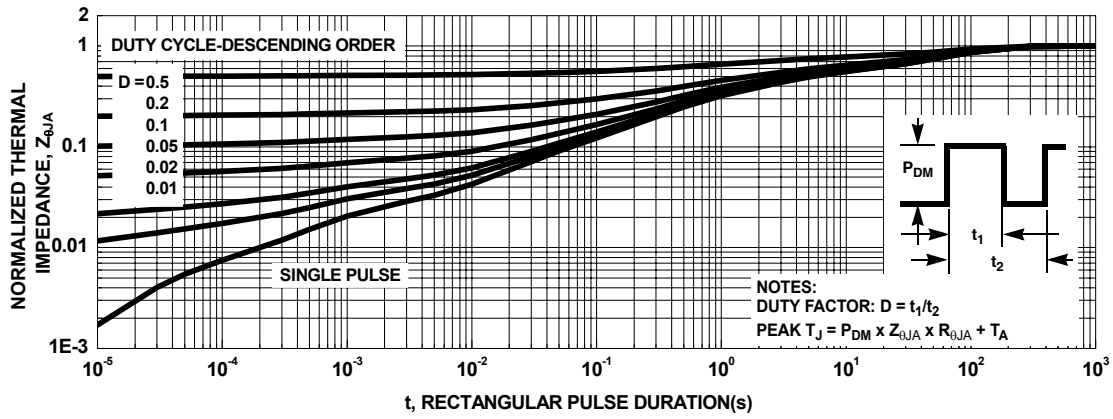


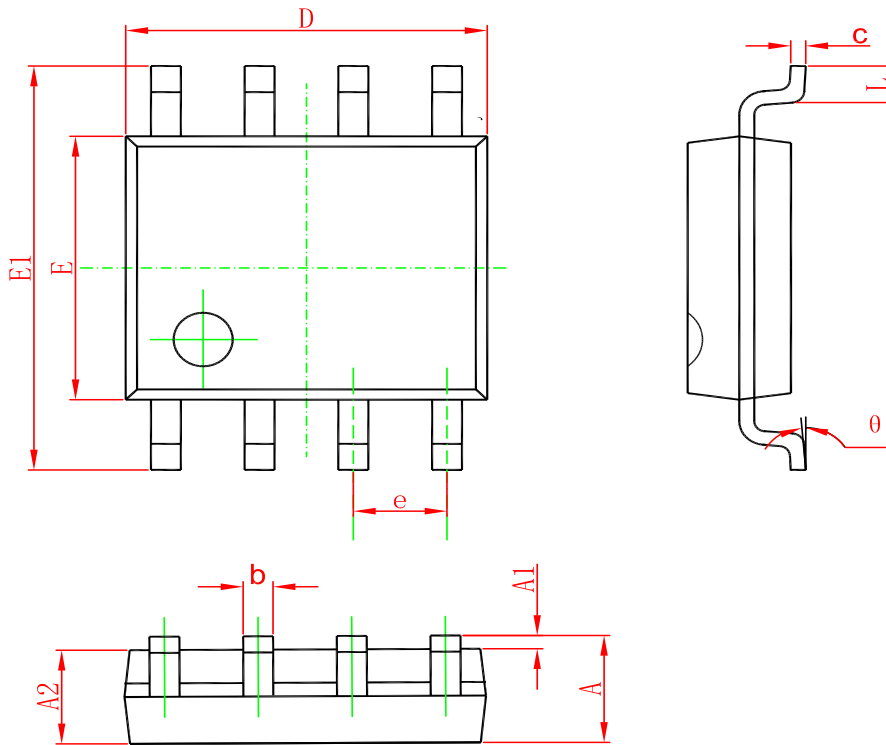
Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted



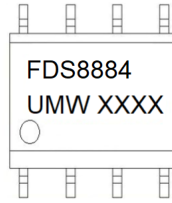
PACKAGE OUTLINE DIMENSIONS

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
theta	0°	8°	0°	8°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
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