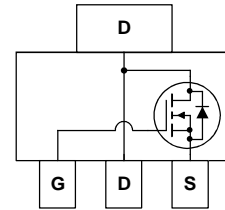## General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/ DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications. The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/ DC power supply designs with higher overall efficiency.



## Features

- $V_{DS(V)}$ = 100V
- $I_D$ = 3.7A ($V_{GS}$ = 10V)
- $R_{DS(ON)} < 120m\Omega$ ($V_{GS}$=10V)
- $R_{DS(ON)} < 130m\Omega$ ($V_{GS}$=6V)
- Fast switching speed
- Low gate charge (14nC typ)
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability in a widely used surface mount package

## Applications

- DC/DC converter
- Motor driving

## Absolute Maximum Ratings $T_A$=25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|--------|-----------|--|---------|-------|
| $V_{DSS}$ | Drain-Source Voltage | | 100 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±20 | V |
| $I_D$ | Drain Current – Continuous | (Note 1a) | 3.7 | A |
| | – Pulsed | | 20 | |
| $P_D$ | Maximum Power Dissipation | (Note 1a) | 3.0 | W |
| | | (Note 1b) | 1.3 | |
| | | (Note 1c) | 1.1 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +150 | °C |

## Thermal Characteristics

| | | | | |
|--------|-----------|--|---------|-------|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 42 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 12 | °C/W |

## Electrical Characteristics $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $W_{DSS}$ | Drain-Source Avalanche Energy | Single Pulse, $V_{DD}$ = 50 V, $I_D$ = 3.7 A | | | 90 | mJ |
| $I_{AR}$ | Drain-Source Avalanche Current | | | | 3.7 | A |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 100 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 µA, Referenced to 25°C | | 106 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 80 V, $V_{GS}$ = 0 V | | | 10 | µA |
| $I_{GSSF}$ | Gate–Body Leakage, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | | | 100 | nA |
| $I_{GSSR}$ | Gate–Body Leakage, Reverse | $V_{GS}$ = –20 V, $V_{DS}$ = 0 V | | | –100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2 | 2.5 | 4 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 250 µA, Referenced to 25°C | | –6 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = 10 V, $I_D$ = 3.7 A | | 88 | 120 | mΩ |
| | | $V_{GS}$ = 6 V, $I_D$ = 3.5 A | | 94 | 130 | |
| $I_{D(on)}$ | On–State Drain Current | $V_{GS}$ = 10 V, $V_{DS}$ = 10 V | 10 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 3.7 A | | 11 | | S |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 632 | | pF |
| $C_{oss}$ | Output Capacitance | | | 40 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 20 | | pF |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = 50 V, $I_D$ = 1 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 8.5 | 17 | ns |
| $t_r$ | Turn–On Rise Time | | | 2 | 4 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 23 | 37 | ns |
| $t_f$ | Turn–Off Fall Time | | | 4.5 | 9 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 50 V, $I_D$ = 3.7 A, $V_{GS}$ = 10 V | | 14 | 20 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | 2.4 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | 3.8 | | nC |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | | | 2.5 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2.5 A     (Note 2) | | 0.75 | 1.2 | V |

**Notes:**

**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 42°C/W when mounted on a 1in$^2$ pad of 2 oz copper



b) 95°C/W when mounted on a .0066 in$^2$ pad of 2 oz copper



c) 110°C/W when mounted on a minimum pad.

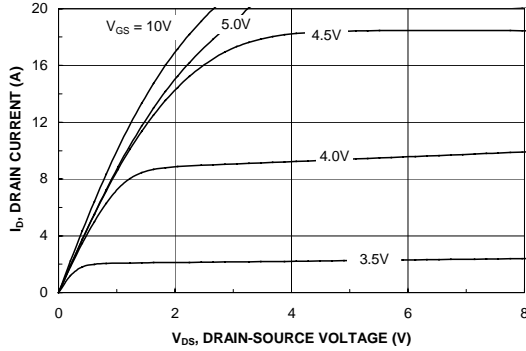## Typical Characteristics



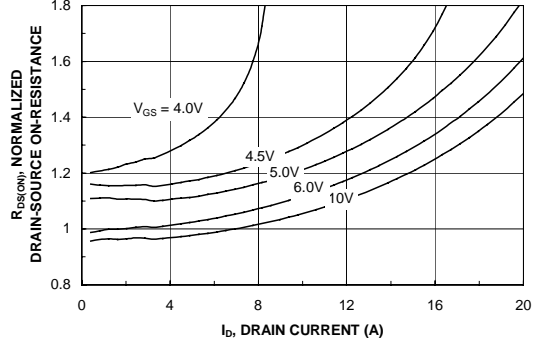Figure 1. On-Region Characteristics.



Figure 2. On-Resistance Variation with
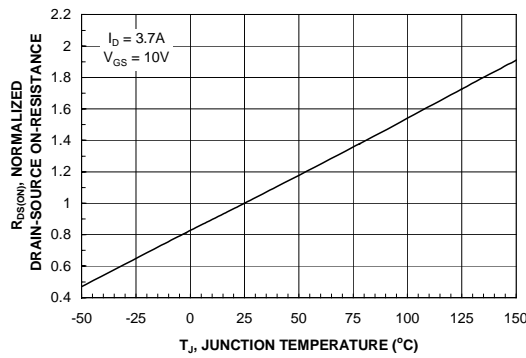Drain Current and Gate Voltage.



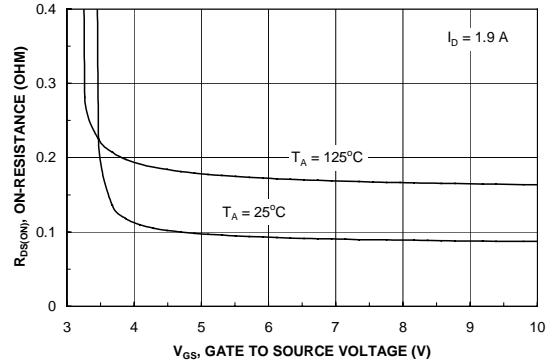Figure 3. On-Resistance Variation with
Temperature.



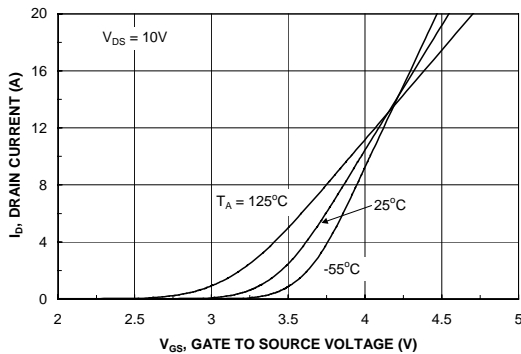Figure 4. On-Resistance Variation with
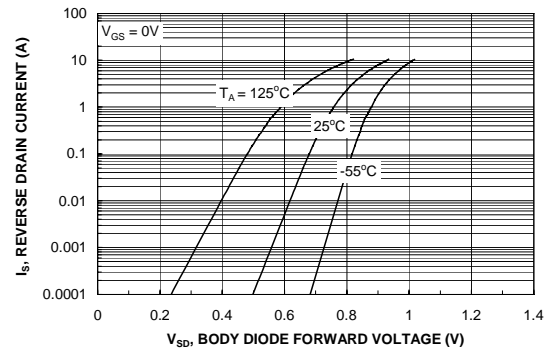Gate-to-Source Voltage.



Figure 5. Transfer Characteristics.



Figure 6. Body Diode Forward Voltage Variation
with Source Current and Temperature.
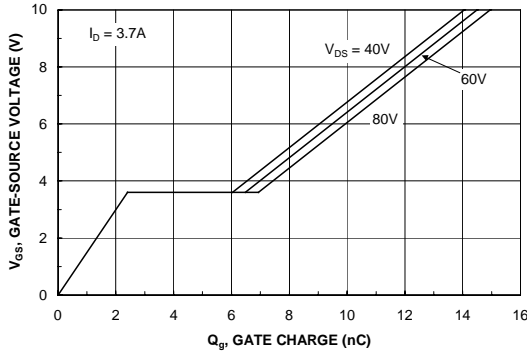
## Typical Characteristics
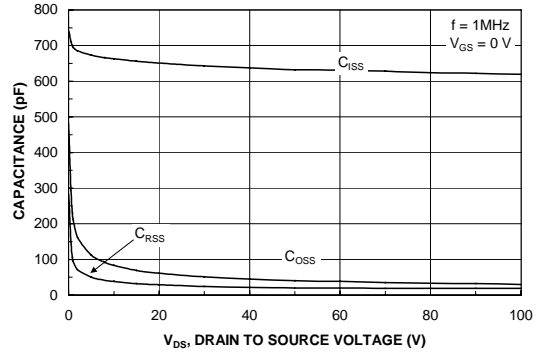


**Figure 7. Gate Charge Characteristics.**



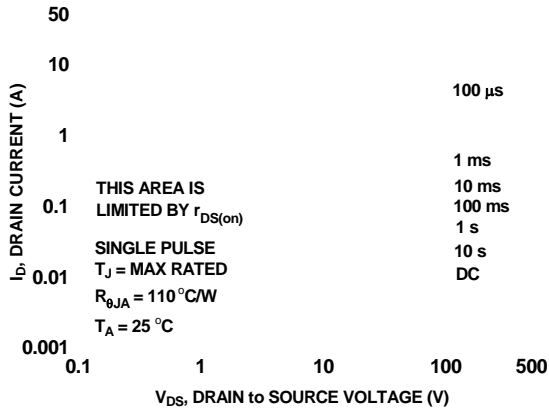**Figure 8. Capacitance Characteristics.**



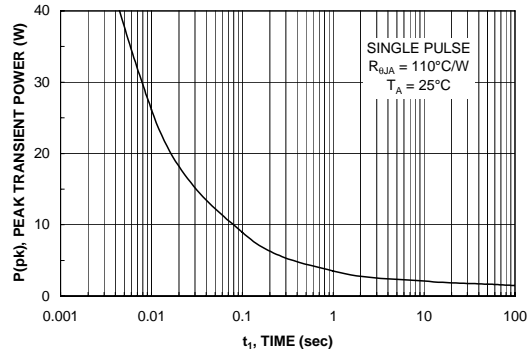**Figure 9. Maximum Safe Operating Area.**



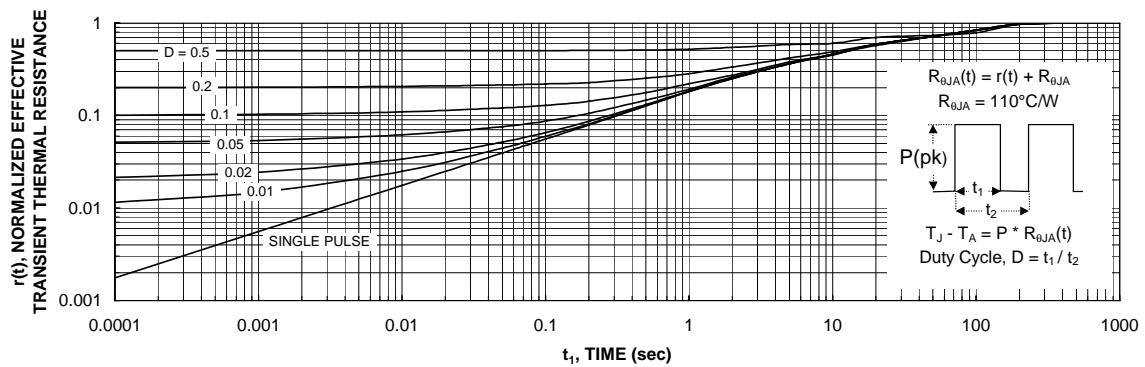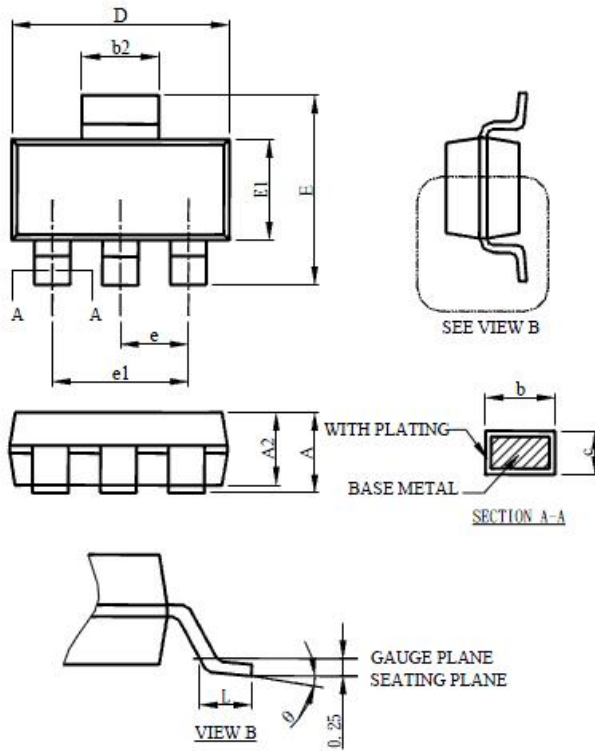**Figure 10. Single Pulse Maximum Power Dissipation.**



**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

■ **SOT223 封裝外形圖**



| SYMBOL | SOT-223 MILLIMETERS | |
|---|---|---|
| | MIN. | MAX. |
| A | | 1.80 |
| A1 | 0.02 | 0.10 |
| A2 | 1.55 | 1.65 |
| b | 0.66 | 0.84 |
| b2 | 2.90 | 3.10 |
| c | 0.23 | 0.33 |
| D | 6.30 | 6.70 |
| E | 6.70 | 7.30 |
| E1 | 3.30 | 3.70 |
| e | 2.30 BSC | |
| e1 | 4.60 BSC | |
| L | 0.90 | |
| θ | 0° | 8° |

Note:
1. Refer to JEDEC TO-261AA.

2. Dimension D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body.

3. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

**Marking**

**Ordering  information**

| Order code | Package | Baseqty | Deliverymode |
|:---:|:---:|:---:|:---:|
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