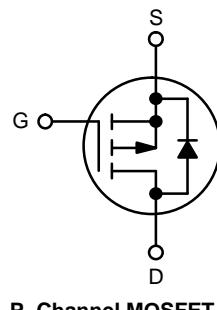


## Description

This P-Channel enhancement mode power MOSFET is produced using planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

## Features

- $V_{DS}(V) = -60V$
- $R_{DS(on)} = 26 \text{ m}\Omega$  ( $V_{GS} = -10V$ )
- $I_D = -47A$
- Low Gate Charge (Typ. 84 nC)
- Low  $C_{rss}$  (Typ. 320 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating



P-Channel MOSFET

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	FQP47P06	Unit
$V_{DSS}$	Drain-Source Voltage	-60	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	-47
		- Continuous ( $T_C = 100^\circ\text{C}$ )	-33.2
$I_{DM}$	Drain Current (Note 1)	- Pulsed	-188
$V_{GSS}$	Gate-Source Voltage	$\pm 25$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	820	mJ
$I_{AR}$	Avalanche Current (Note 1)	-47	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	16	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	-7.0	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	160	W
		- Derate above $25^\circ\text{C}$	1.06 W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 0.43 \text{ mH}$ ,  $I_{AS} = -47 \text{ A}$ ,  $V_{DD} = -25 \text{ V}$ ,  $R_G = 25 \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq -47 \text{ A}$ ,  $di/dt \leq 300 \text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$

## THERMAL CHARACTERISTICS

Symbol	Characteristic	FQP47P06	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.94	$^\circ\text{C}/\text{W}$
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink, Typ.	0.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	$^\circ\text{C}/\text{W}$

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0 \text{ V}$ , $I_D = -250 \mu\text{A}$	-60			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-0.06		$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -60 \text{ V}$ , $V_{GS} = 0 \text{ V}$			-1	$\mu\text{A}$
		$V_{DS} = -48 \text{ V}$ , $T_C = 150^\circ\text{C}$			-10	$\mu\text{A}$
$I_{GSSF}$	Gate–Body Leakage Current, Forward	$V_{GS} = -25 \text{ V}$ , $V_{DS} = 0 \text{ V}$			-100	nA
$I_{GSSR}$	Gate–Body Leakage Current, Reverse	$V_{GS} = 25 \text{ V}$ , $V_{DS} = 0 \text{ V}$			100	nA

**ON CHARACTERISTICS**

$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = -250 \mu\text{A}$	-1.1	-1.8	-2.5	V
$R_{DS(\text{on})}$	Static Drain–Source On–Resistance	$V_{GS} = -10 \text{ V}$ , $I_D = -23.5 \text{ A}$		21	26	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = -30 \text{ V}$ , $I_D = -23.5 \text{ A}$ (Note 4)		21		S

**DYNAMIC CHARACTERISTICS**

$C_{iss}$	Input Capacitance	$V_{DS} = -25 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1.0 \text{ MHz}$		2800	3600	pF
$C_{oss}$	Output Capacitance			1300	1700	pF
$C_{rss}$	Reverse Transfer Capacitance			320	420	pF

**SWITCHING CHARACTERISTICS**

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -30 \text{ V}$ , $I_D = -23.5 \text{ A}$ , $R_G = 25 \Omega$ (Note 4, 5)		50	110	ns
$t_r$	Turn–On Rise Time			450	910	ns
$t_{d(off)}$	Turn–Off Delay Time			100	210	ns
$t_f$	Turn–Off Fall Time			195	400	ns
$Q_g$	Total Gate Charge	$V_{DS} = -48 \text{ V}$ , $I_D = -47 \text{ A}$ , $V_{GS} = -10 \text{ V}$ (Note 4, 5)		84	110	nC
$Q_{gs}$	Gate–Source Charge			18		nC
$Q_{gd}$	Gate–Drain Charge			44		nC

**DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATING**

$I_S$	Maximum Continuous Drain–Source Diode Forward Current			-47	A
$I_{SM}$	Maximum Pulsed Drain–Source Diode Forward Current			-188	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}$ , $I_S = -47 \text{ A}$		-4.0	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0 \text{ V}$ , $I_S = -47 \text{ A}$ , $dI_F / dt = 100 \text{ A}/\mu\text{s}$ (Note 4)		130	ns
$Q_{rr}$	Reverse Recovery Charge			0.55	$\mu\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse width  $\leq 300 \mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

## TYPICAL CHARACTERISTICS

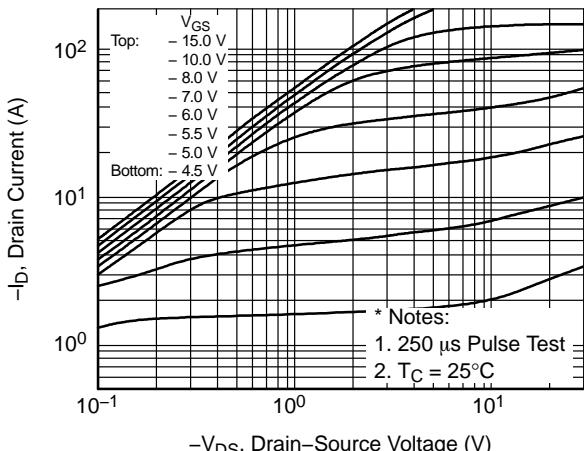


Figure 1. On-Region Characteristics

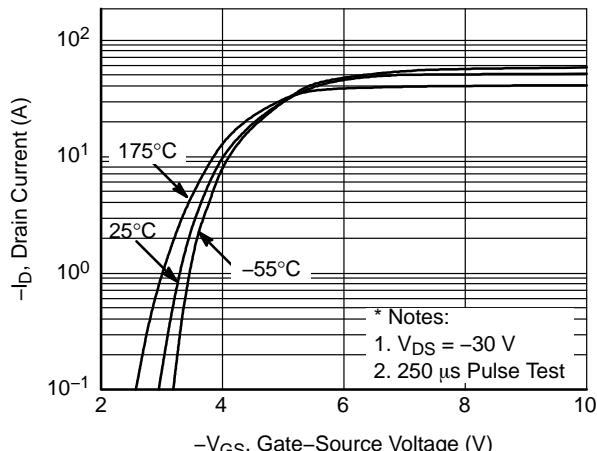


Figure 2. Transfer Characteristics

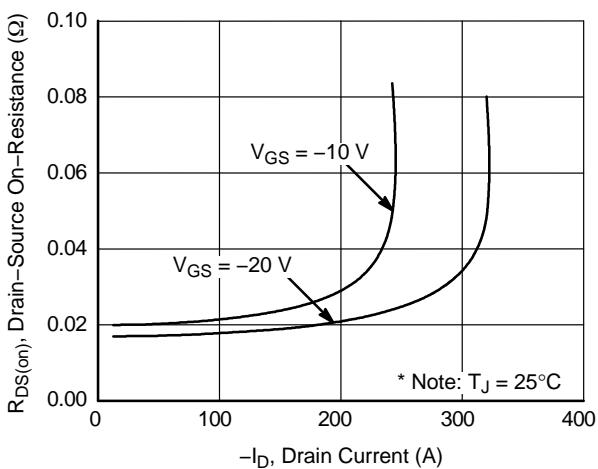


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

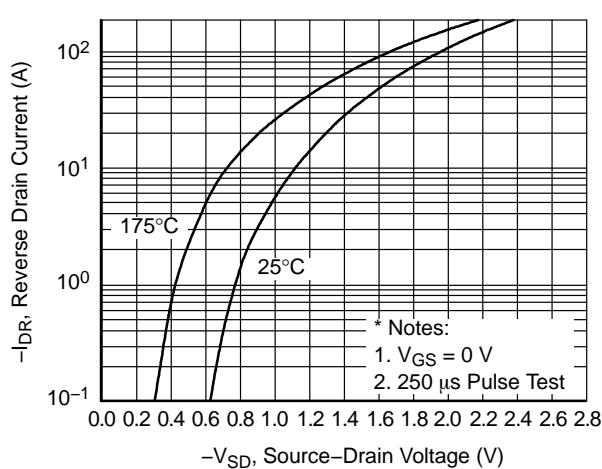


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

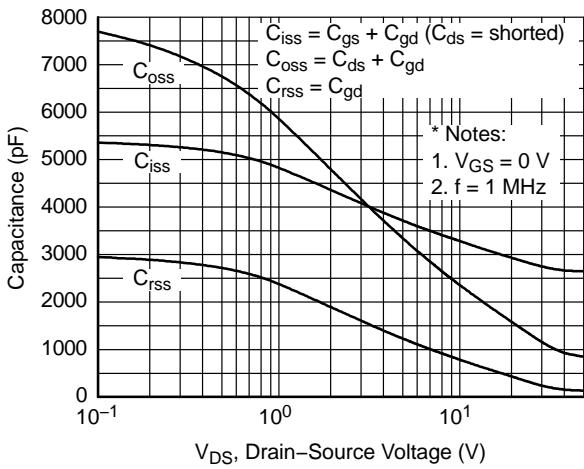


Figure 5. Capacitance Characteristics

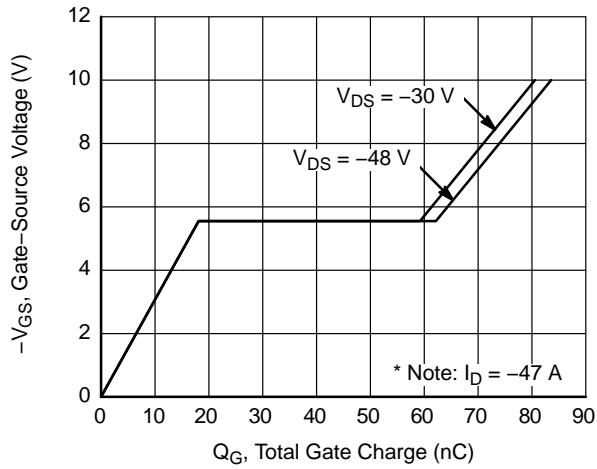
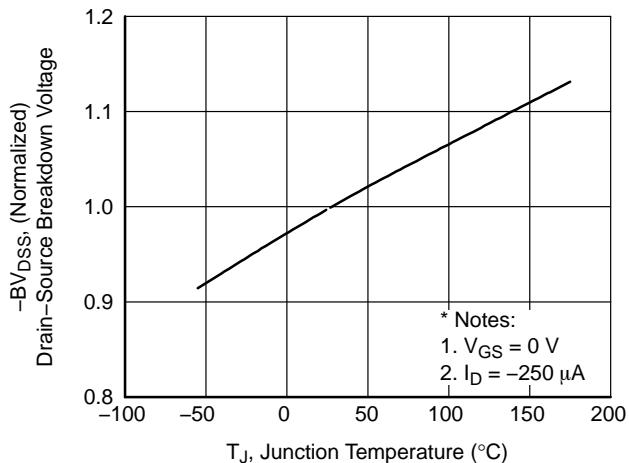
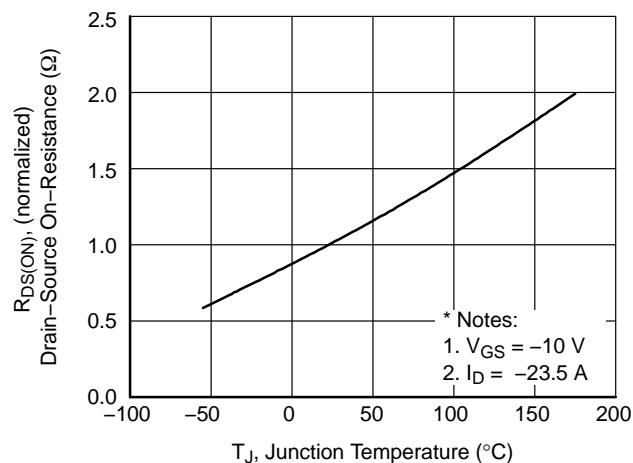


Figure 6. Gate Charge Characteristics

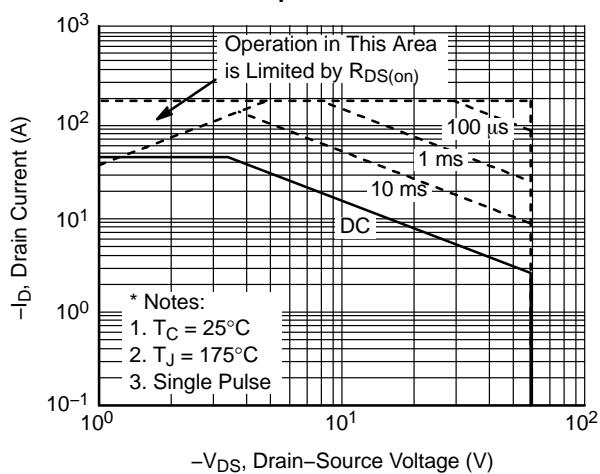
## TYPICAL CHARACTERISTICS (Continued)



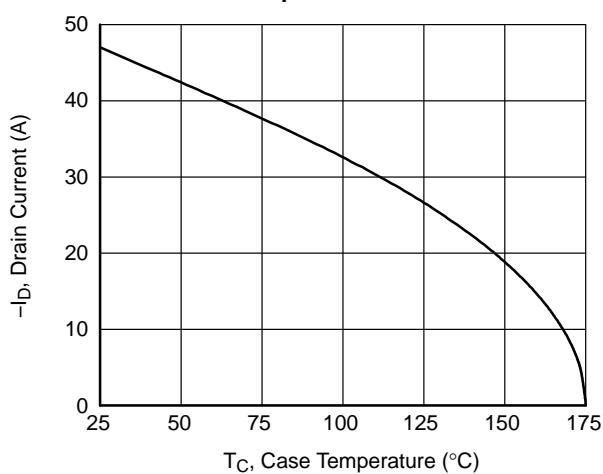
**Figure 7. Breakdown Voltage Variation vs. Temperature**



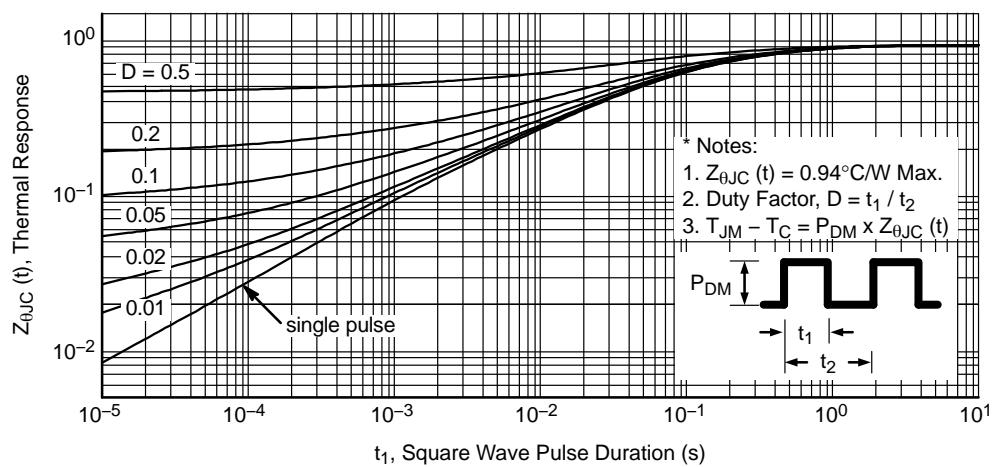
**Figure 8. On-Resistance Variation vs. Temperature**



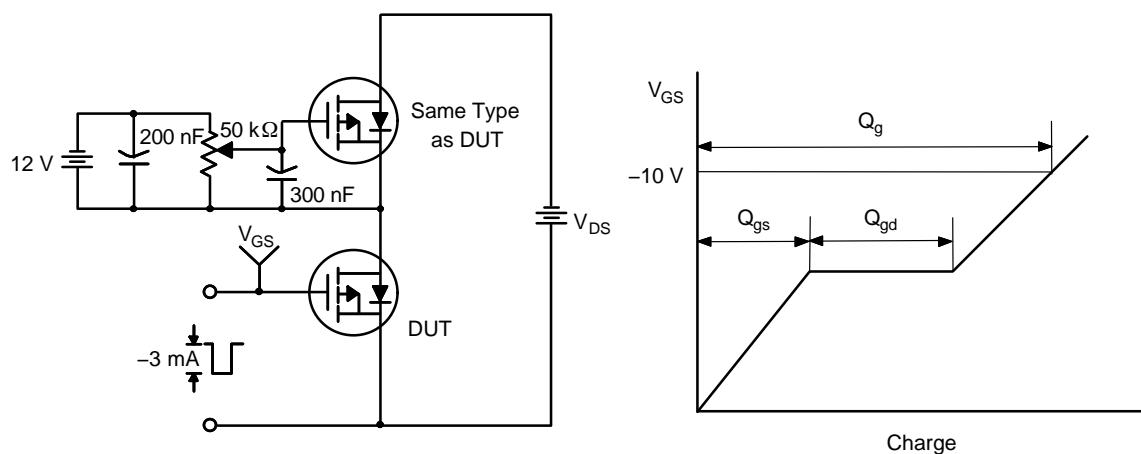
**Figure 9. Maximum Safe Operating Area**



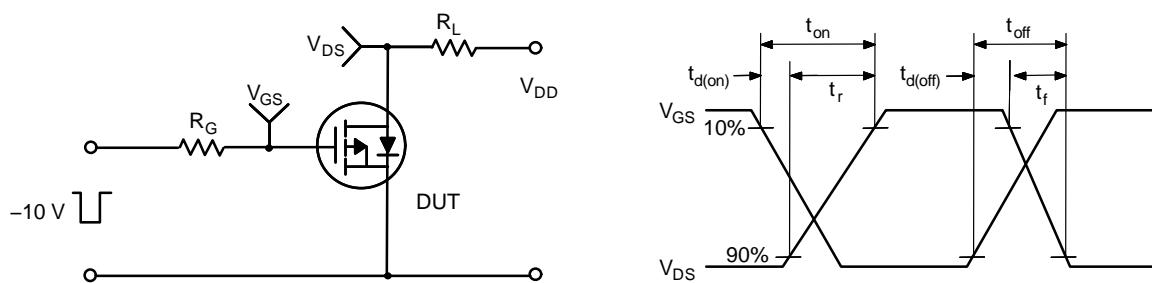
**Figure 10. Maximum Drain Current vs. Case Temperature**



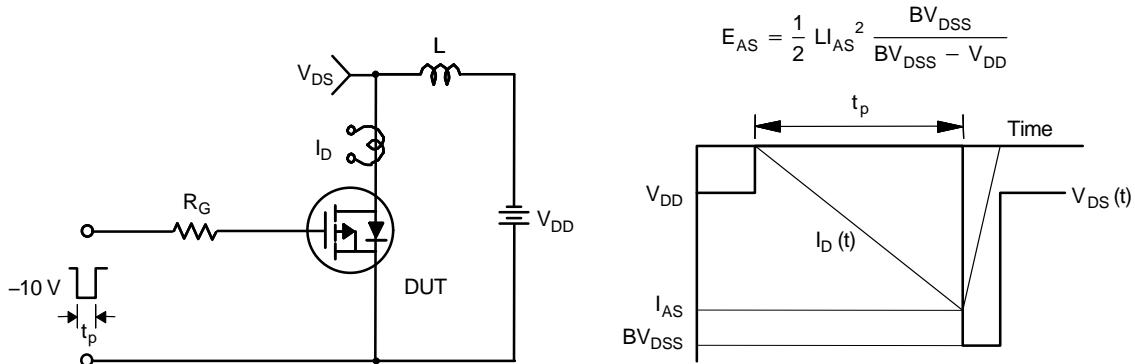
**Figure 11. Transient Thermal Response Curve**



**Figure 12. Gate Charge Test Circuit & Waveform**



**Figure 13. Resistive Switching Test Circuit & Waveforms**



**Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms**

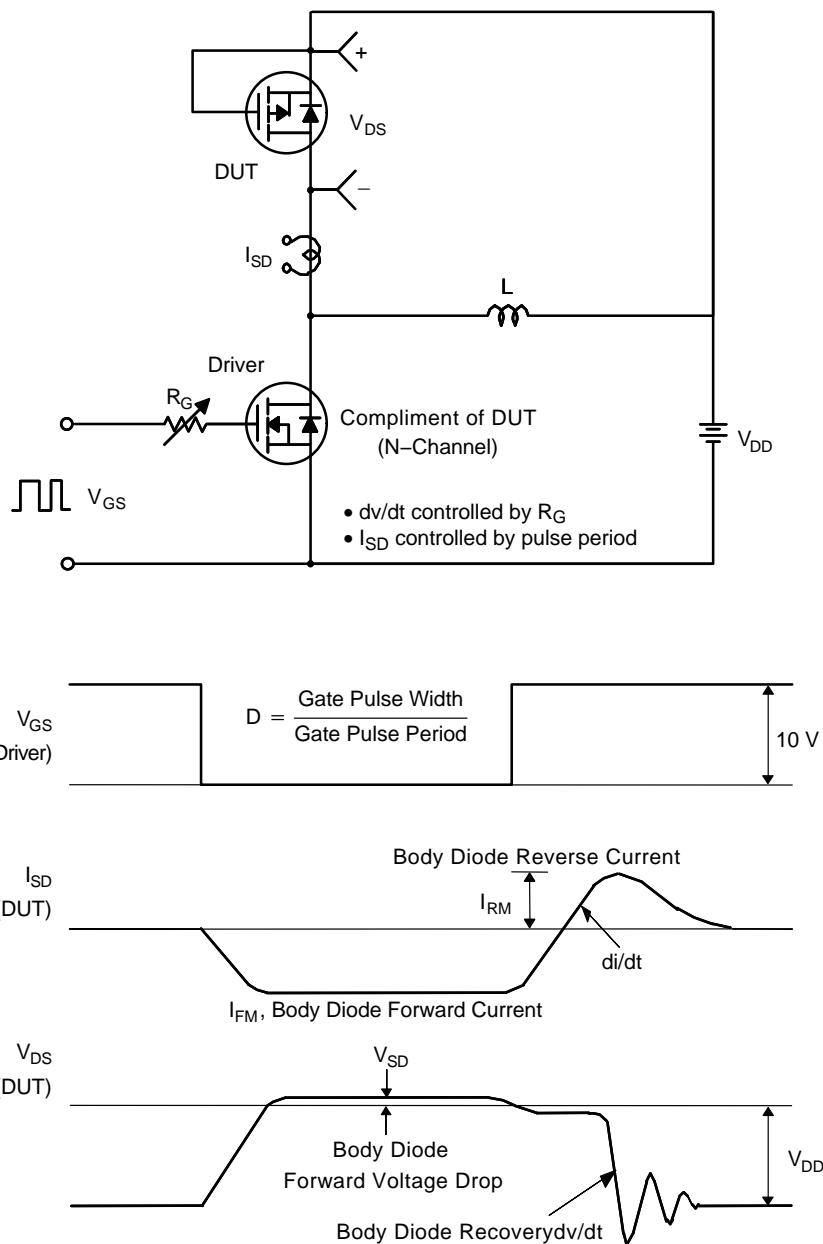
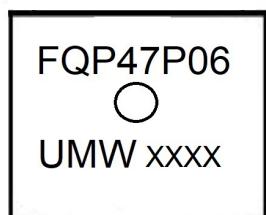


Figure 15. Peak Diode Recovery dv/dt Test Circuit &amp; Waveforms

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