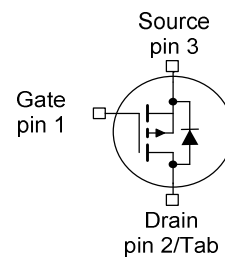


Features

- AEC qualified
- 175°C operating temperature
- Intended for reverse battery protection
- $V_{DS}(V) = -40V$
- $I_D = -50A$ ($V_{GS} = -10V$)
- $R_{DS(ON)} < 10.6m\Omega$ ($V_{GS} = -10V$)
- $R_{DS(ON)} < 17.2m\Omega$ ($V_{GS} = -4.5V$)



Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{°C}$, $V_{GS}=-10V^{(1)}$	-50	A
		$T_C=100\text{°C}$, $V_{GS}=-10V^{(2)}$	-40	
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	$T_C=25\text{°C}$	-200	
Avalanche energy, single pulse	E_{AS}	$I_D = -25A$	18	mJ
Avalanche current, single pulse	I_{AS}		-50	A
Gate source voltage	V_{GS}		$\pm 16^{(3)}$	V
Power dissipation	P_{tot}	$T_C=25\text{°C}$	58	W
Operating and storage temperature	T_j, T_{stg}		-55 ... +175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}				2.6	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint			62	
		6 cm ² cooling area ⁴⁾			40	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-1mA$	-40			V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-85\mu A$	-1.2	-1.7	-2.2	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=-32V, V_{GS}=0V, T_j=25^\circ\text{C}$		-0.03	-1	μA
		$V_{DS}=-32V, V_{GS}=0V, T_j=125^\circ\text{C}^{2)}$		-7	-70	
Gate-source leakage current	I_{GSS}	$V_{GS}=-16V, V_{DS}=0V$			-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-30A$		12.3	17.2	m Ω
		$V_{GS}=-10V, I_D=-50A$		8.2	10.6	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Input capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=-25V,$ $f=1MHz$		3000	3900	pF
Output capacitance	C_{oss}			1100	1400	
Reverse transfer capacitance	C_{rss}			37	74	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-20V,$ $V_{GS}=-10V, I_D=-50A,$ $R_G=3.5\Omega$		12		ns
Rise time	t_r			9		
Turn-off delay time	$t_{d(off)}$			46		
Fall time	t_f			39		
Gate to source charge	Q_{gs}	$V_{DD}=-32V, I_D=-50A,$ $V_{GS}=0$ to $-10V$		11	14	nC
Gate to drain charge	Q_{gd}			8	16	
Gate charge total	Q_g			45	59	
Gate plateau voltage	$V_{plateau}$			-3.6		
Diode continuous forward current ²⁾	I_S	$T_C=25^\circ C$			-50	A
Diode pulse current ²⁾	$I_{S,pulse}$				-200	
Diode forward voltage	V_{SD}	$V_{GS}=0V, I_F=-50A,$ $T_J=25^\circ C$		-1	-1.3	V
Reverse recovery time ²⁾	t_{rr}	$V_R=-20V, I_F=50A,$ $di_F/dt=-100A/\mu s$		40		ns
Reverse recovery charge ²⁾	Q_{rr}			32		

¹⁾ Current is limited by bondwire; with an $R_{thJC} = 2.6K/W$ the chip is able to carry 60A at 25°C.

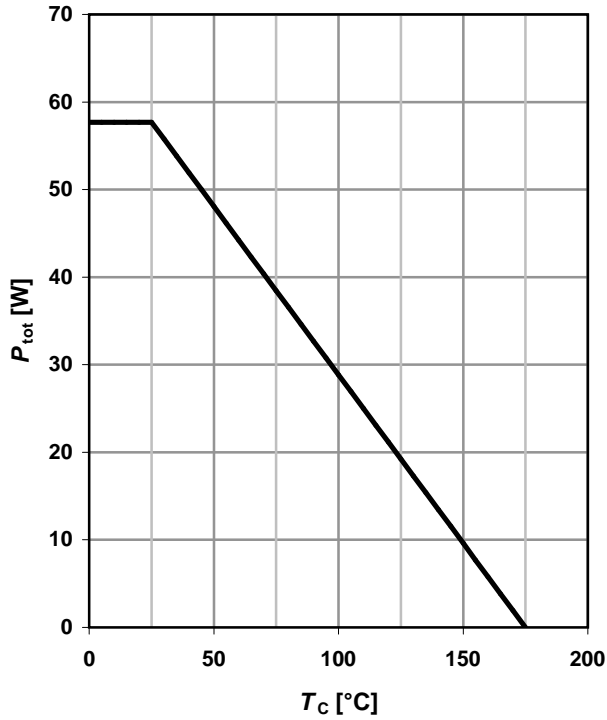
²⁾ Specified by design. Not subject to production test.

³⁾ $V_{GS}=+5V/-16V$ according AEC; $V_{GS}=+16V$ for max 168h at $T_J=175^\circ C$

⁴⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

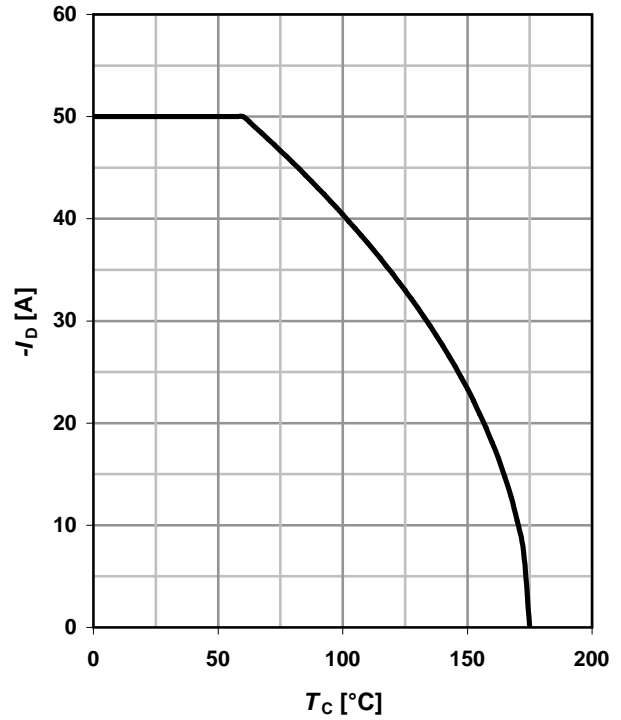
1 Power dissipation

$P_{tot} = f(T_C); V_{GS} \leq -6V$



2 Drain current

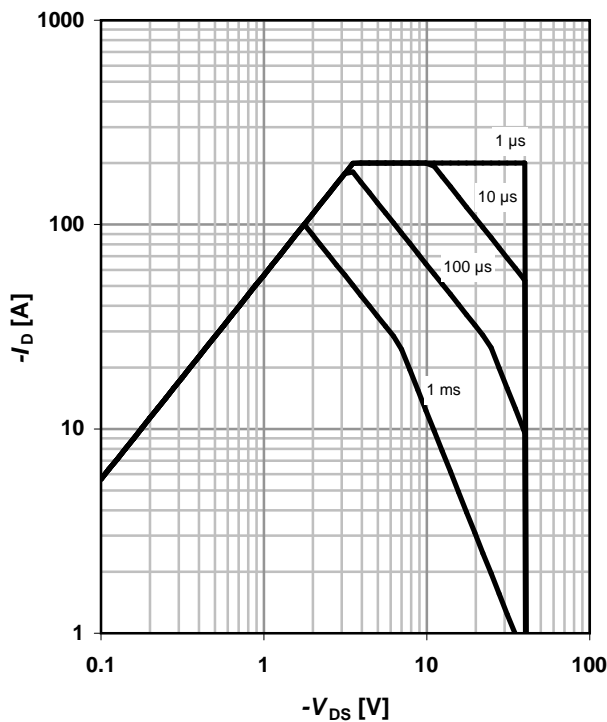
$I_D = f(T_C); V_{GS} \leq -6V$



3 Safe operating area

$I_D = f(V_{DS}); T_C = 25^\circ C; D = 0$

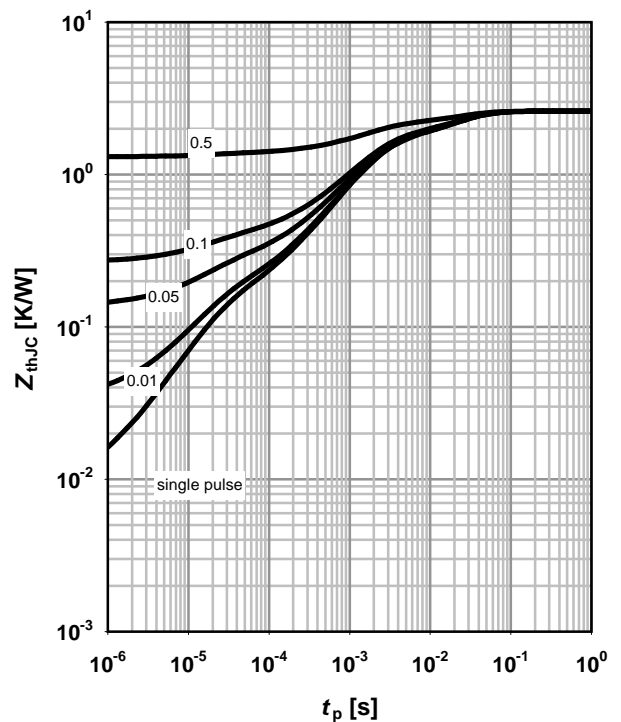
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

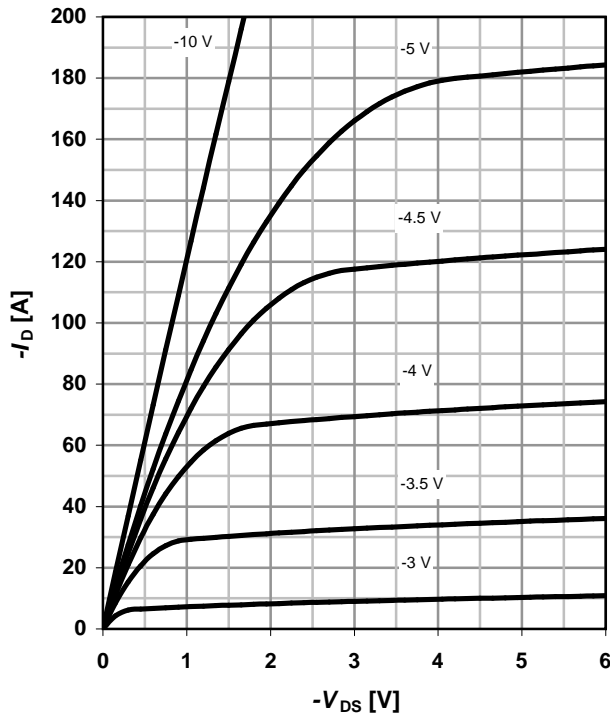
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

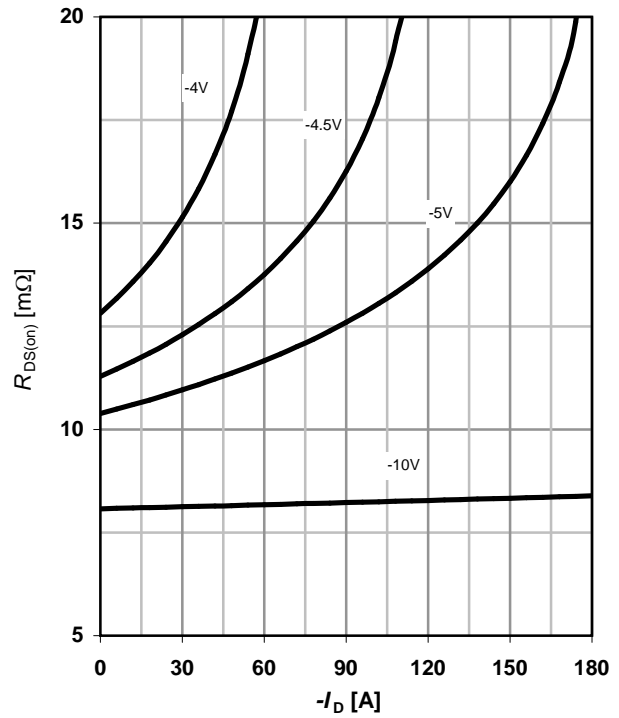
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

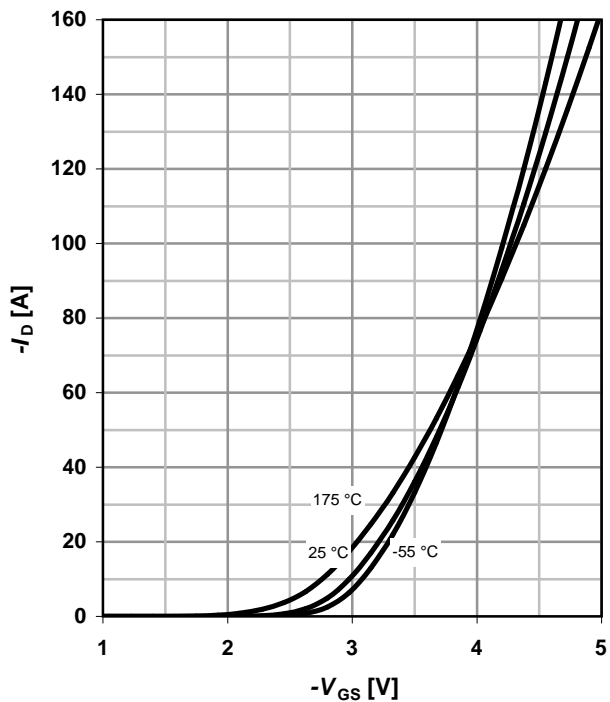
parameter: V_{GS}



7 Typ. transfer characteristics

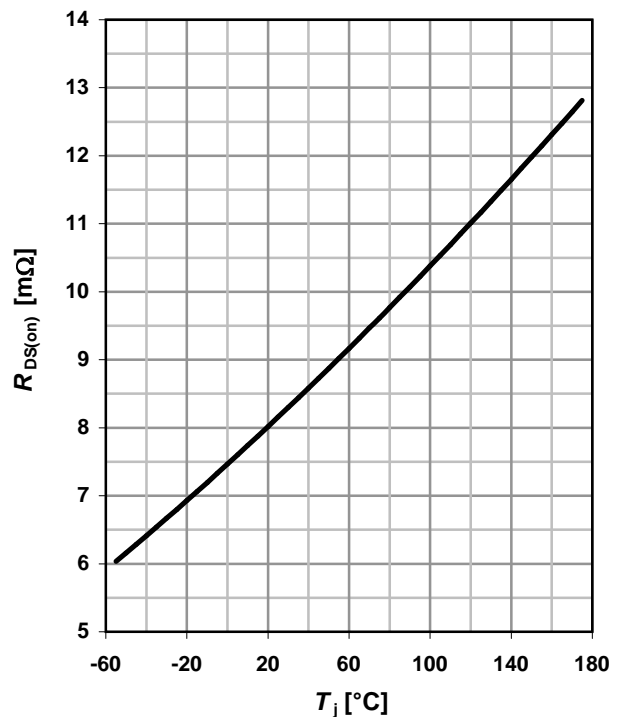
$I_D = f(V_{GS}); V_{DS} = -6V$

parameter: T_j



8 Typ. drain-source on-state resistance

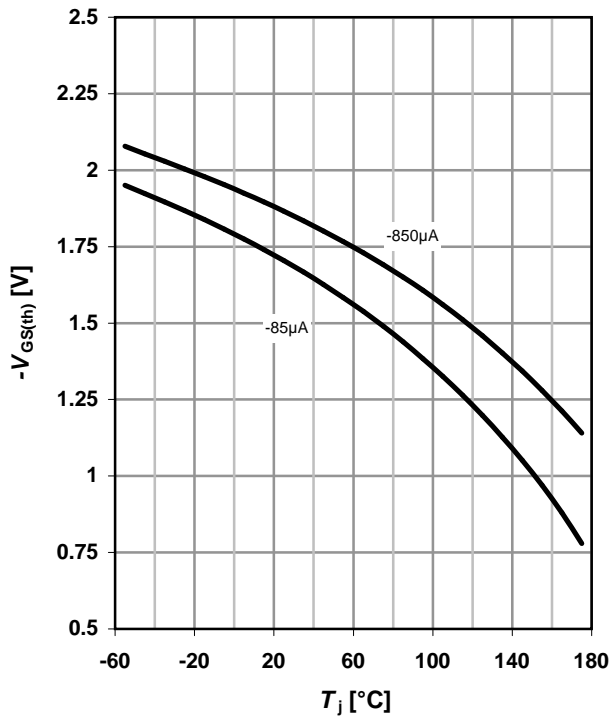
$R_{DS(on)} = f(T_j); I_D = -50A; V_{GS} = -10V$



9 Typ. gate threshold voltage

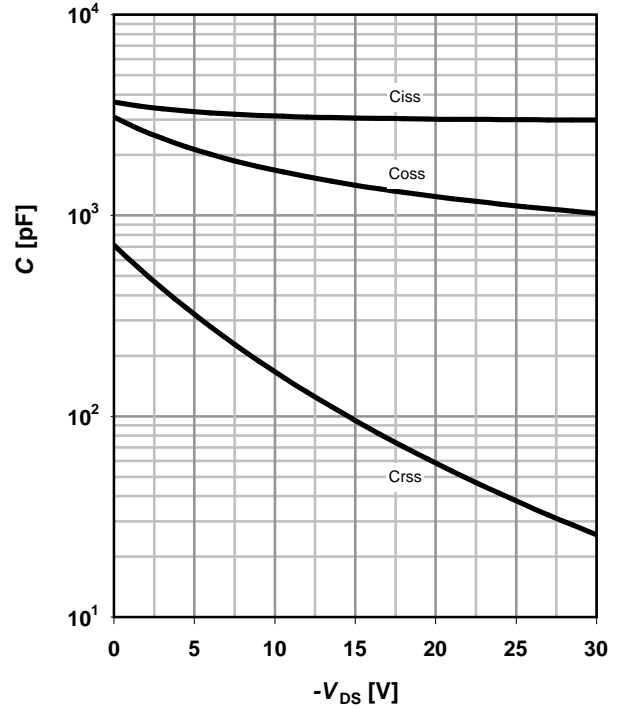
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

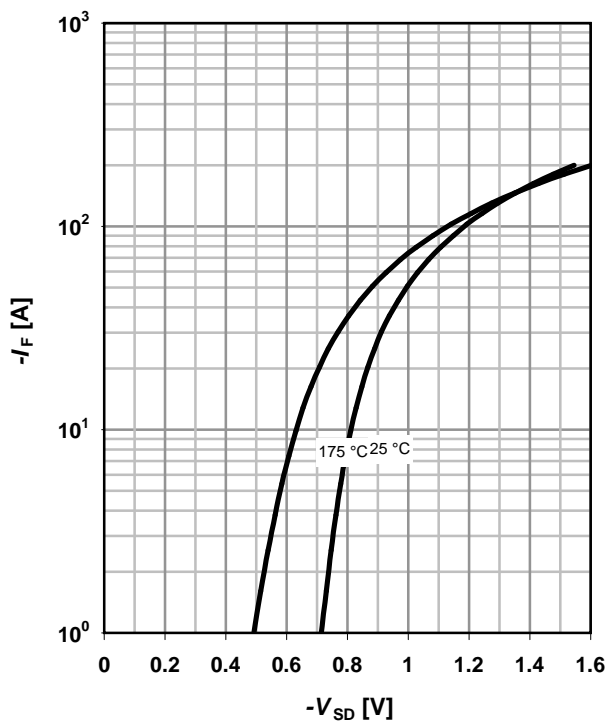
$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$



11 Typical forward diode characteristics

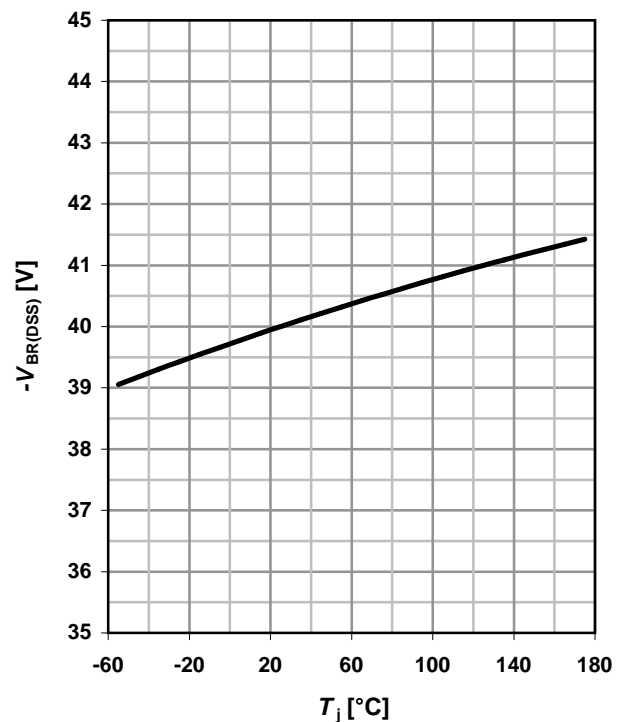
$I_F = f(V_{SD})$

parameter: T_j



12 Drain-source breakdown voltage

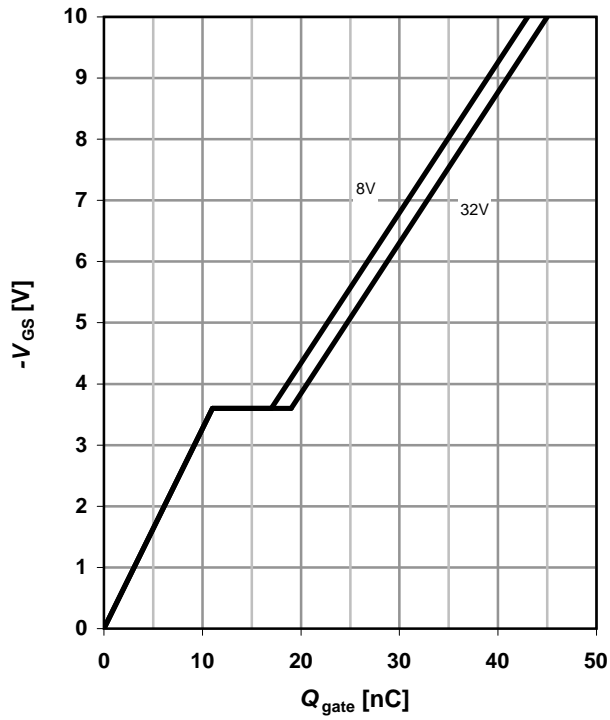
$V_{BR(DSS)} = f(T_j); I_D = -1mA$



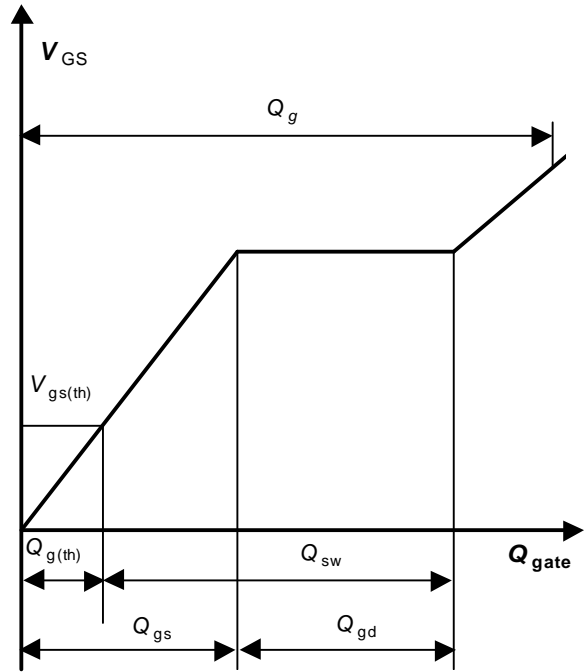
13 Typ. gate charge

$V_{GS} = f(Q_{gate}); I_D = -50A$ pulsed

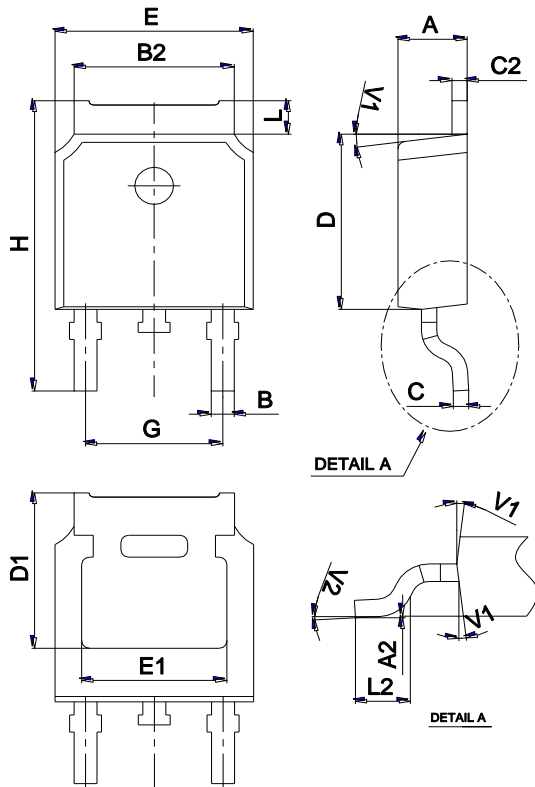
parameter: V_{DD}



14 Gate charge waveforms

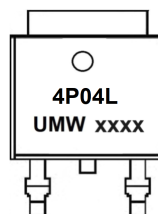


Package Mechanical Data TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW IPD50P04P4L11	TO-252	2500	Tape and reel

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