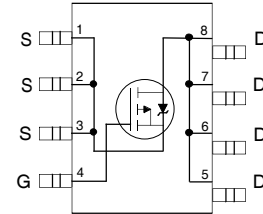


Description

The SOP-8 package is designed for vapor phase, infra red, or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.



Features

- $V_{DS(V)} = -30V$
- $I_D = -4.6A (V_{GS} = -10V)$
- $R_{DS(ON)} < 70m\Omega (V_{GS} = -10V)$
- $R_{DS(ON)} < 130m\Omega (V_{GS} = -4.5V)$
- Advanced Process Technology
- Ultra Low On-resistance
- Surface Mount
- Fast Switching
- Lead-free

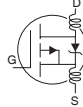
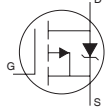
Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	-4.6	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	-3.7	
I_{DM}	Pulsed Drain Current ①	-15	
$P_D @ T_C = 25^\circ C$	Power Dissipation	2.5	W
	Linear Derating Factor	0.020	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ②	-3.0	V/nS
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance Ratings

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ④			50	°C/W

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-30	---	---	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	---	-0.024	---	V/°C	Reference to 25°C , $I_D = -1\text{mA}$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance			70	mΩ	$V_{GS} = -10V, I_D = -4.6A$ ③
				130		$V_{GS} = -4.5V, I_D = -2.0A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	---	-3.0	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	---	6.6	---	S	$V_{DS} = -15V, I_D = -4.6A$ ③
I_{DSS}	Drain-to-Source Leakage Current	---	---	-1.0	μA	$V_{DS} = -24V, V_{GS} = 0V$
		---	---	-5.0		$V_{DS} = -15V, V_{GS} = 0V, T_J = 70^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	---	---	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	---	---	100		$V_{GS} = 20V$
Q_g	Total Gate Charge	---	27	40	nC	$I_D = -4.6A$
Q_{gs}	Gate-to-Source Charge	---	5.2	---		$V_{DS} = -15V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	---	7.5	---		$V_{GS} = -10V$ ③
$t_{d(on)}$	Turn-On Delay Time	---	14	30	ns	$V_{DD} = -15V$
t_r	Rise Time	---	21	60		$I_D = -1.0A$
$t_{d(off)}$	Turn-Off Delay Time	---	97	150		$R_G = 6.0\Omega$
t_f	Fall Time	---	71	100		$R_D = 10\Omega$ ③
L_D	Internal Drain Inductance		2.5		nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	---	4.0			
C_{iss}	Input Capacitance	---	870		pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	---	720			$V_{DS} = -10V$
C_{riss}	Reverse Transfer Capacitance	---	220	---		$f = 1.0\text{MHz}$
I_S	Continuous Source Current (Body Diode)	---	---	-2.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	---	---	-15		
V_{SD}	Diode Forward Voltage	---	---	-1.2	V	$T_J = 25^\circ\text{C}, I_S = -1.25A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	---	70	100	ns	$T_J = 25^\circ\text{C}, I_F = -4.6A$
Q_{rr}	Reverse Recovery Charge	---	100	180	nC	$di/dt = 100A/\mu s$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② $I_{SD} \leq -4.6A, di/dt \leq 90A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
- ③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ④ Surface mounted on FR-4 board, $t \leq 10\text{sec}$.

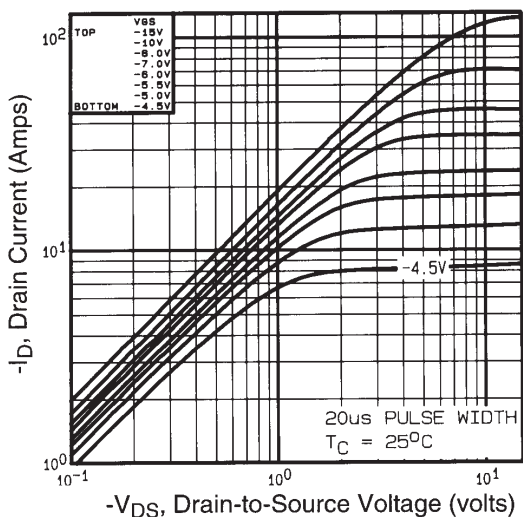


Fig 1. Typical Output Characteristics,

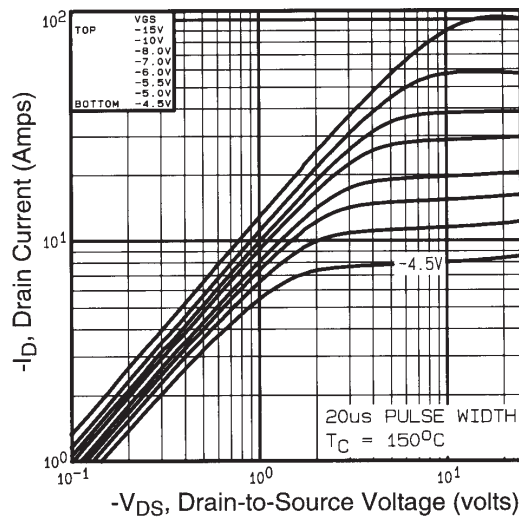


Fig 2. Typical Output Characteristics,

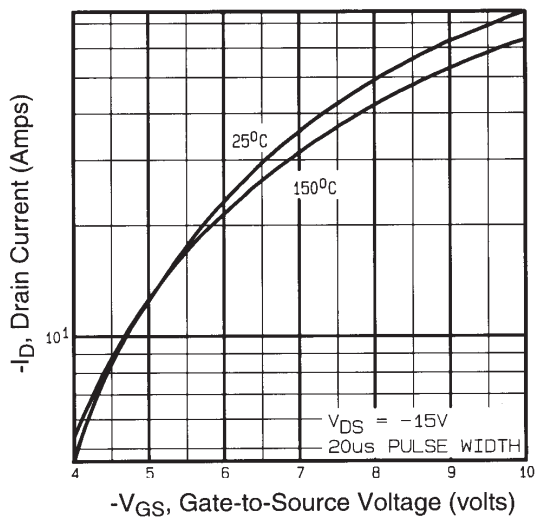


Fig 3. Typical Transfer Characteristics

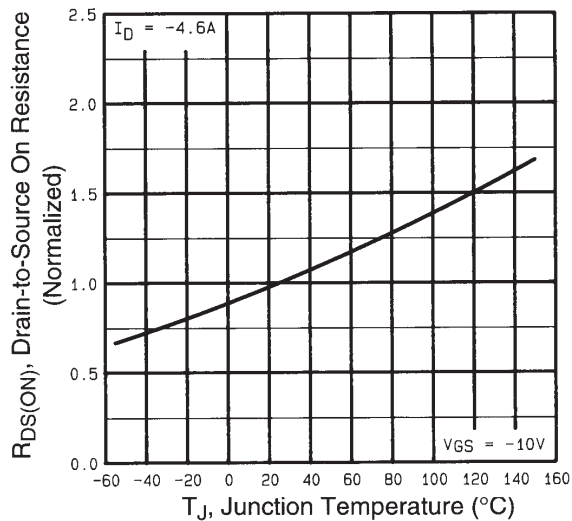


Fig 4. Normalized On-Resistance Vs. Temperature

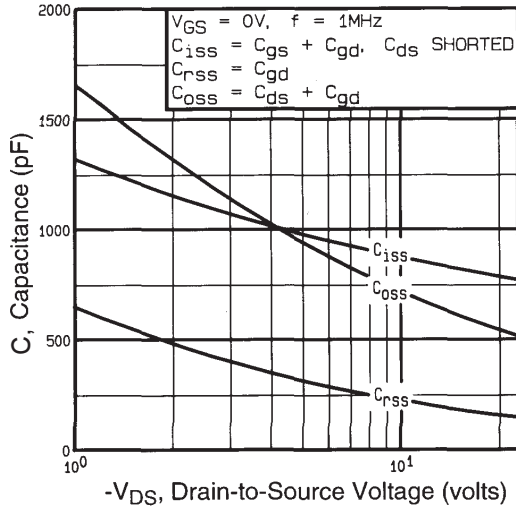


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

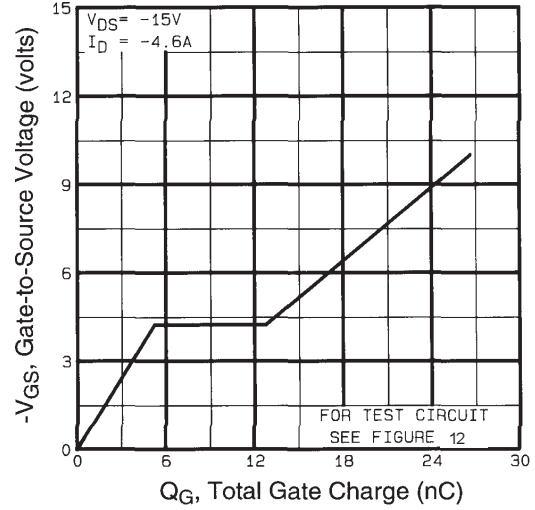


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

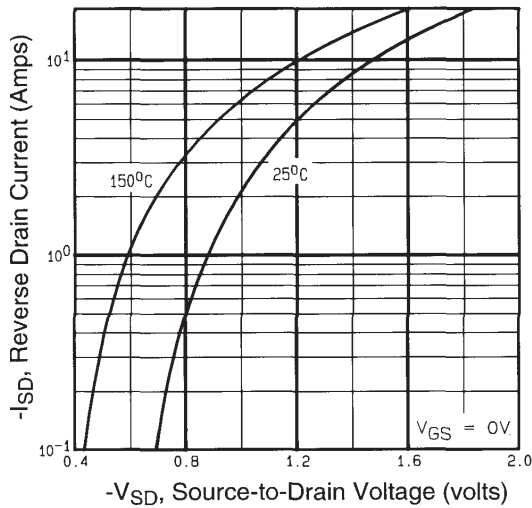


Fig 7. Typical Source-Drain Diode Forward Voltage

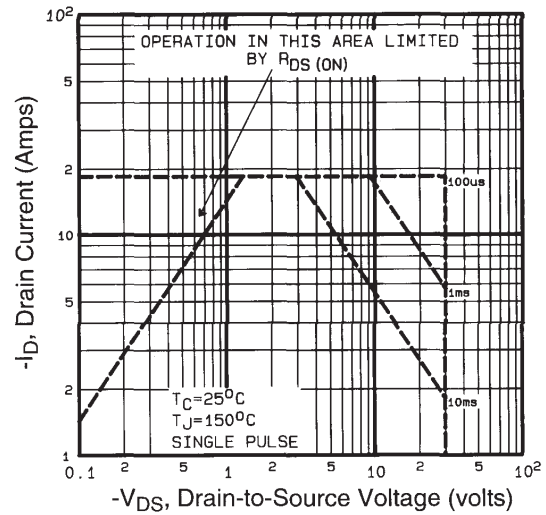


Fig 8. Maximum Safe Operating Area

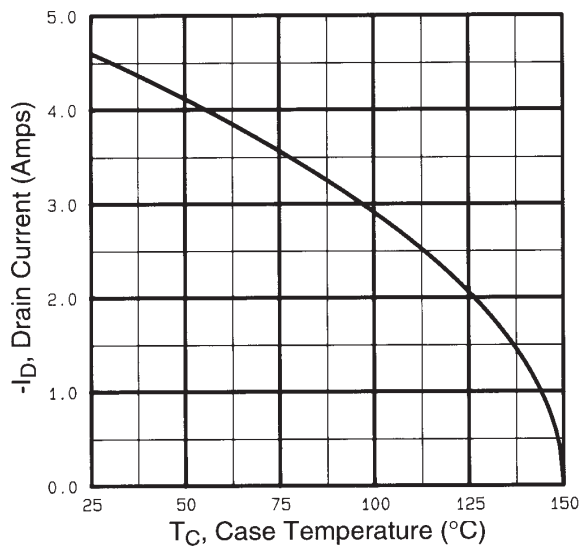


Fig 9. Maximum Drain Current Vs. Case Temperature

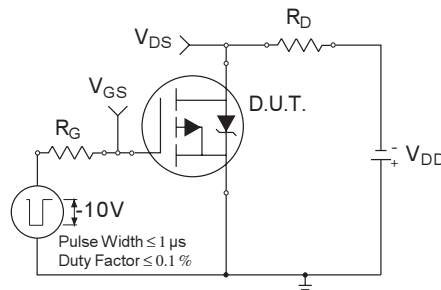


Fig 10a. Switching Time Test Circuit

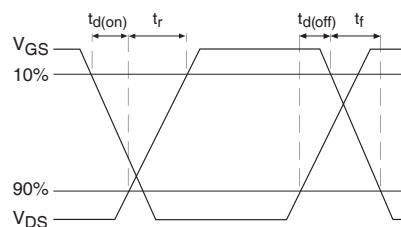


Fig 10b. Switching Time Waveforms

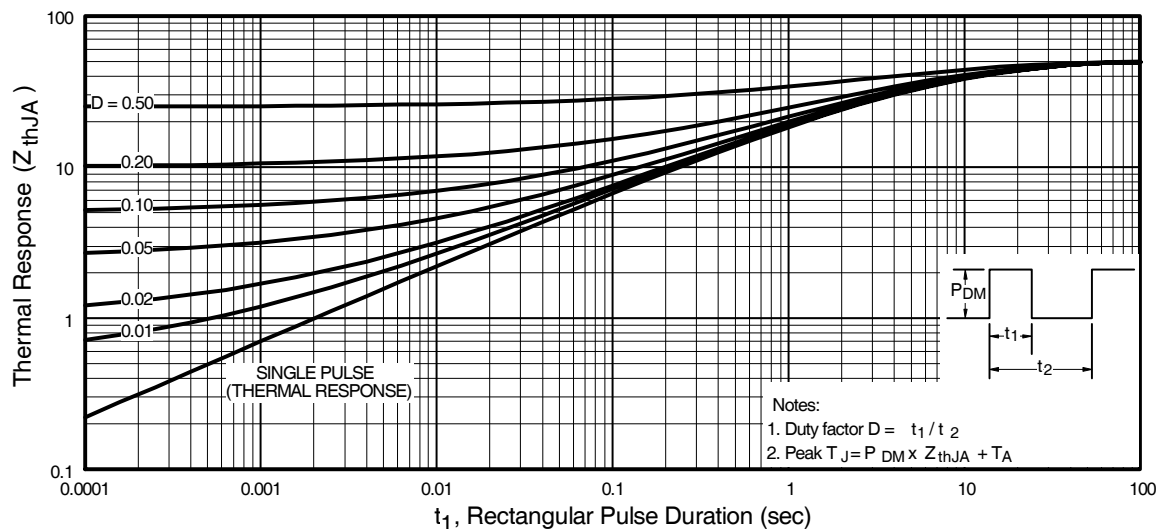
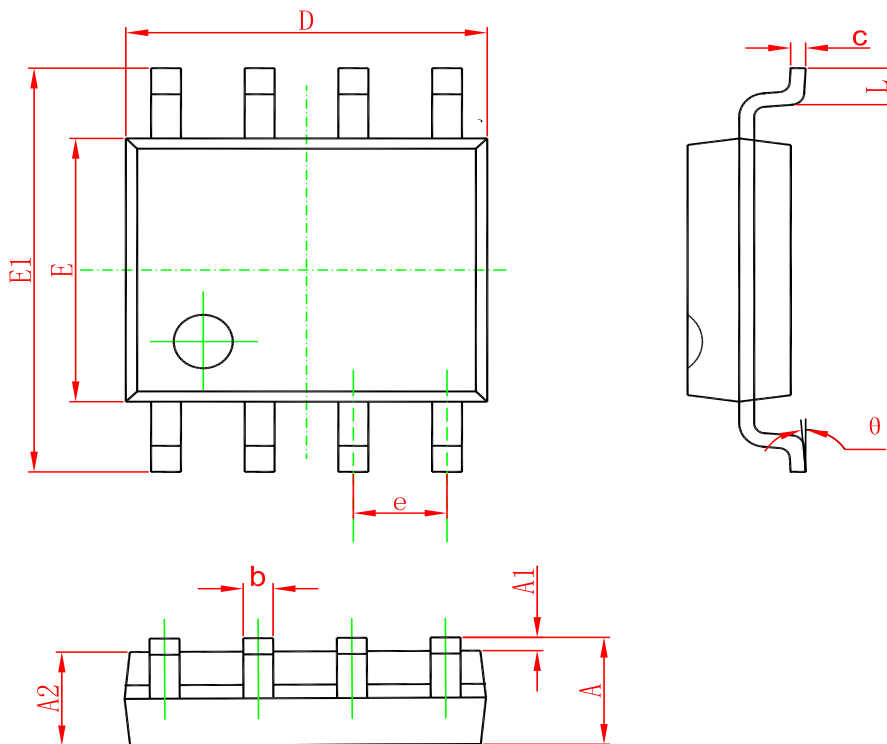


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

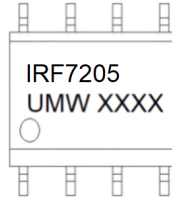
PACKAGE OUTLINE DIMENSIONS

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
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