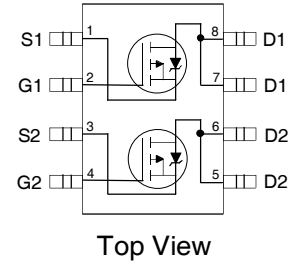


Features

- $V_{DS} (V) = -20V$
- $R_{DS(ON)} < 90m\Omega (V_{GS} = -4.5V)$
- $R_{DS(ON)} < 140 m\Omega (V_{GS} = -2.7V)$
- Generation V Technology
- Ultra Low On-Resistance
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching
- Lead-Free



Description

The SOP-8 has been modified through a customized leadframe for enhanced thermacharacierstics and multiple e-dle capability making it deal in a variety o powerapplications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phaseinfra red, or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_A = 25^\circ C$	10 Sec. Pulsed Drain Current, $V_{GS} @ -4.5V$	-4.7	A
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V$	-4.3	
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ -4.5V$	-3.4	
I_{DM}	Pulsed Drain Current ①	-17	
$P_D @ T_A = 25^\circ C$	Power Dissipation	2.0	W
	Linear Derating Factor	0.016	W/°C
V_{GS}	Gate-to-Source Voltage	± 12	V
dv/dt	Peak Diode Recovery dv/dt ②	-5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance Ratings

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient④		62.5	°C/W

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-20			V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient		-0.012		V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1\text{mA}$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	1		90 140	m Ω	$V_{GS} = -4.5V, I_D = -2.2A$ ③ $V_{GS} = -2.7V, I_D = -1.8A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	-0.70			V	$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	4.0			S	$V_{DS} = -16V, I_D = -2.2A$
I_{DSS}	Drain-to-Source Leakage Current			-1.0 -25	μA	$V_{DS} = -16V, V_{GS} = 0V$ $V_{DS} = -16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage			-100	nA	$V_{GS} = -12V$
	Gate-to-Source Reverse Leakage			100	nA	$V_{GS} = 12V$
Q_g	Total Gate Charge			22	nC	$I_D = -2.2A$
Q_{gs}	Gate-to-Source Charge			3.3	nC	$V_{DS} = -16V$
Q_{gd}	Gate-to-Drain ("Miller") Charge			9.0	nC	$V_{GS} = -4.5V$, See Fig. 6 and 12 ③
$t_{d(on)}$	Turn-On Delay Time		8.4		ns	$V_{DD} = -10V$
t_r	Rise Time		26		ns	$I_D = -2.2A$
$t_{d(off)}$	Turn-Off Delay Time		51		ns	$R_G = 6.0\Omega$
t_f	Fall Time		33		ns	$R_G = 4.5\Omega$, See Fig. 10 ③
L_D	Internal Drain Inductance		4.0		nH	Between lead tip and center of die contact
L_S	Internal Source Inductance		6.0		nH	
C_{iss}	Input Capacitance		610		pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance		310		pF	$V_{DS} = -15V$
C_{rss}	Reverse Transfer Capacitance		170		pF	$f = 1.0\text{MHz}$, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)			-2.5	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①			-17	A	
V_{SD}	Diode Forward Voltage			-1.0	V	$T_J = 25^\circ\text{C}, I_S = -1.8A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time		56	84	ns	$T_J = 25^\circ\text{C}, I_F = -2.2A$
Q_{rr}	Reverse Recovery Charge		71	110	nC	$di/dt = 100A/\mu s$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② $I_{SD} \leq -2.2A, di/dt \leq -50A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
- ③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

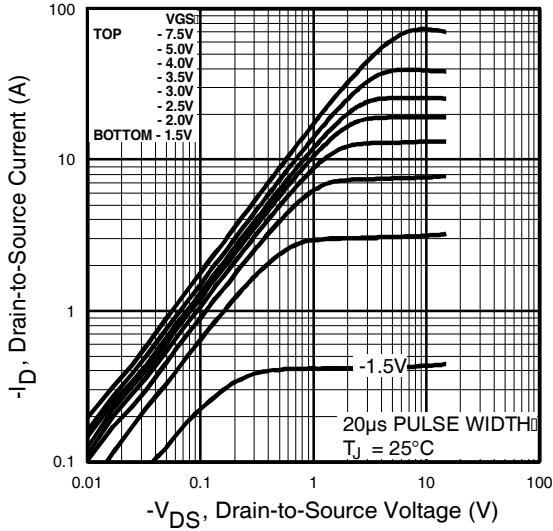


Fig 1. Typical Output Characteristics

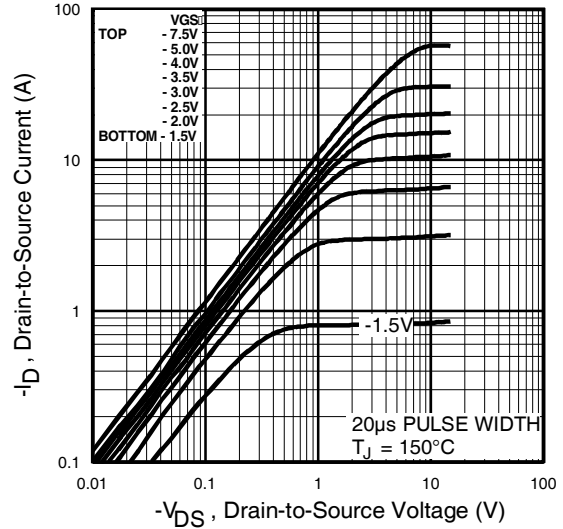


Fig 2. Typical Output Characteristics

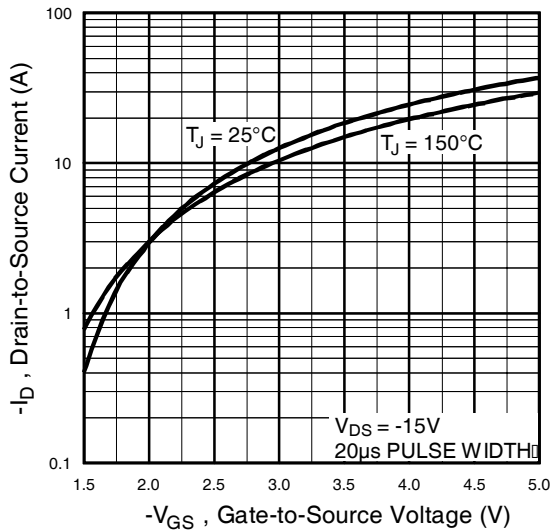


Fig 3. Typical Transfer Characteristics

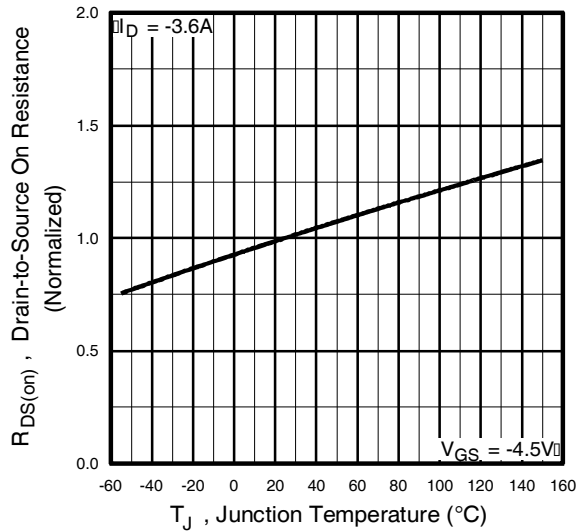


Fig 4. Normalized On-Resistance Vs. Temperature

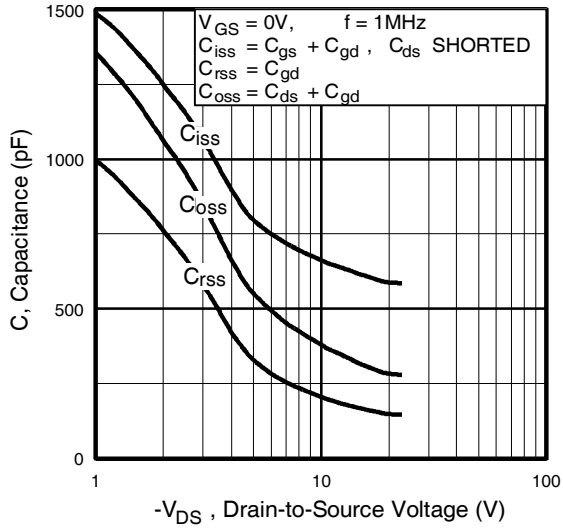


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

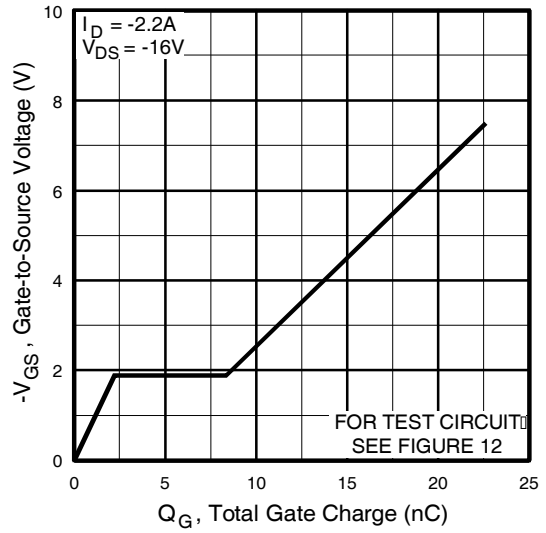


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

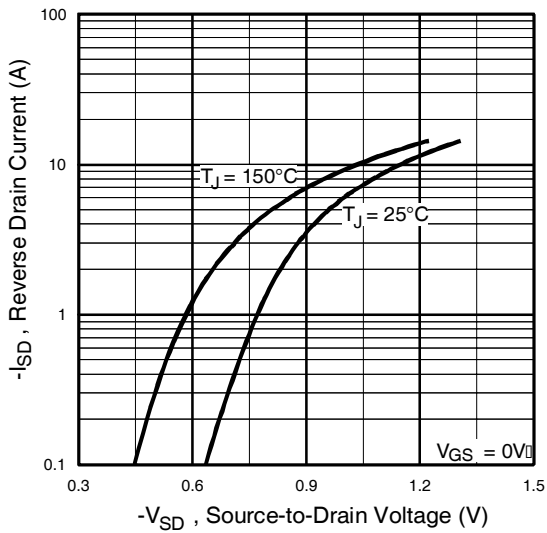


Fig 7. Typical Source-Drain Diode Forward Voltage

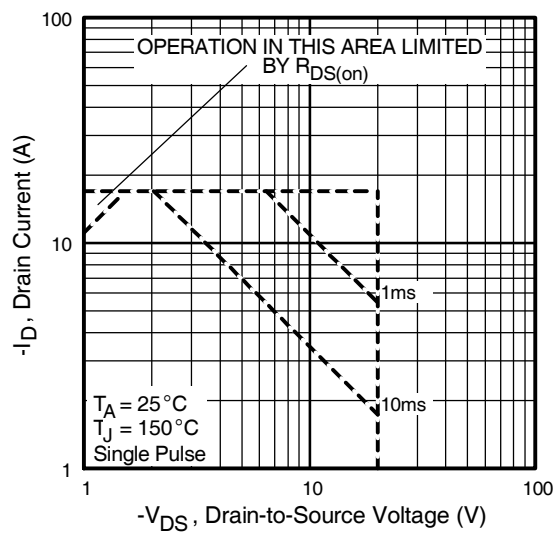


Fig 8. Maximum Safe Operating Area

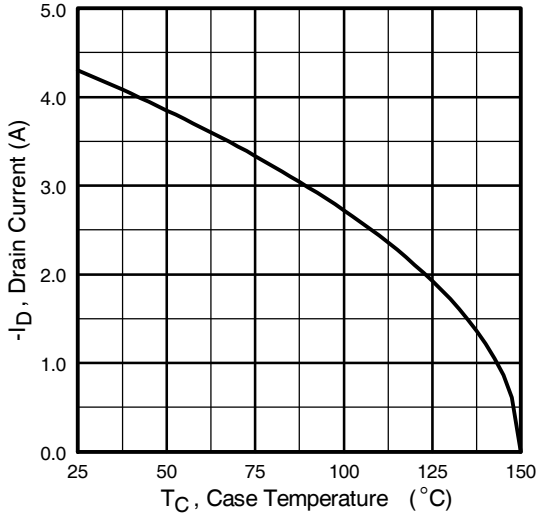


Fig 9. Maximum Drain Current Vs. Ambient Temperature

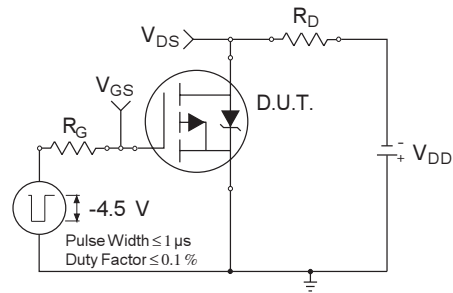


Fig 10a. Switching Time Test Circuit

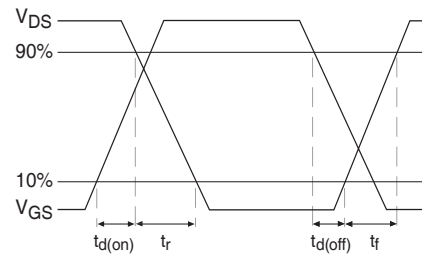


Fig 10b. Switching Time Waveforms

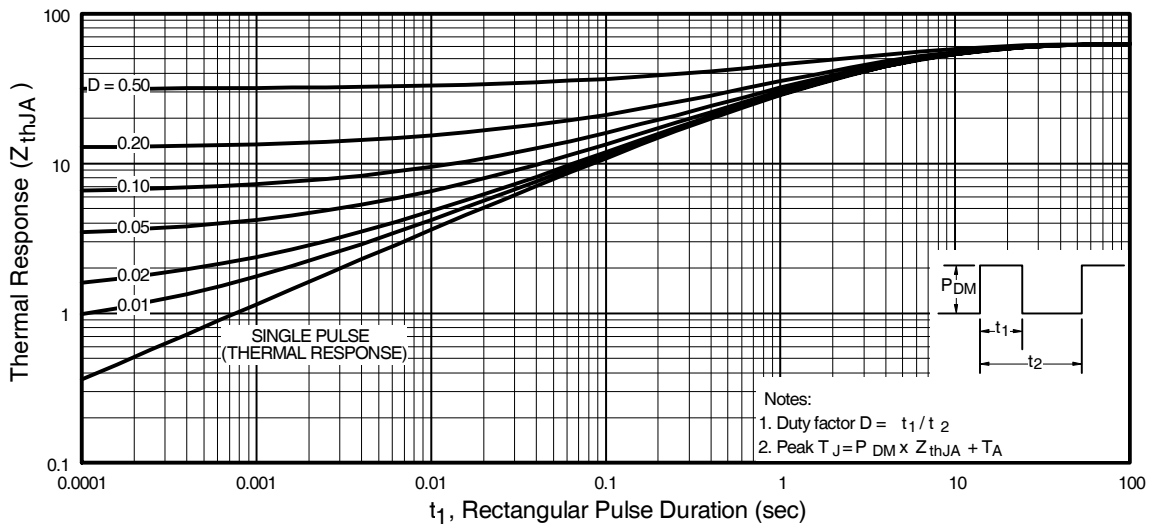


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

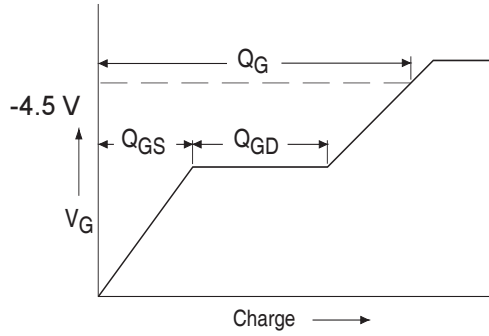


Fig 12a. Basic Gate Charge Waveform

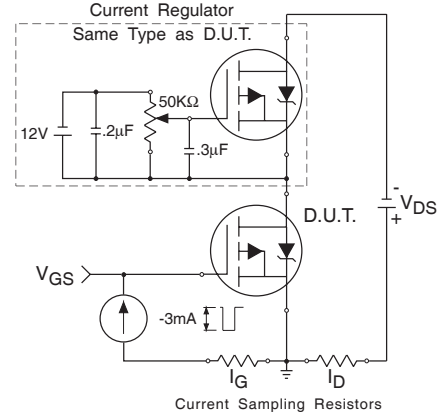
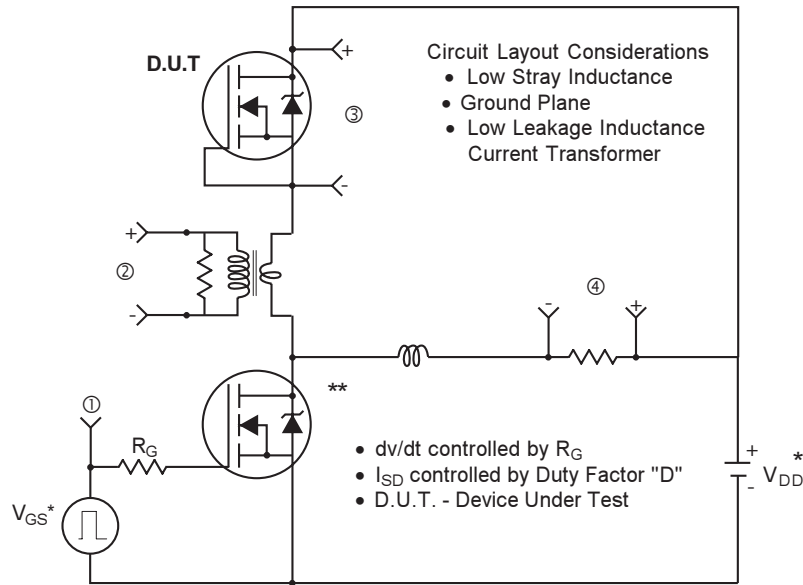


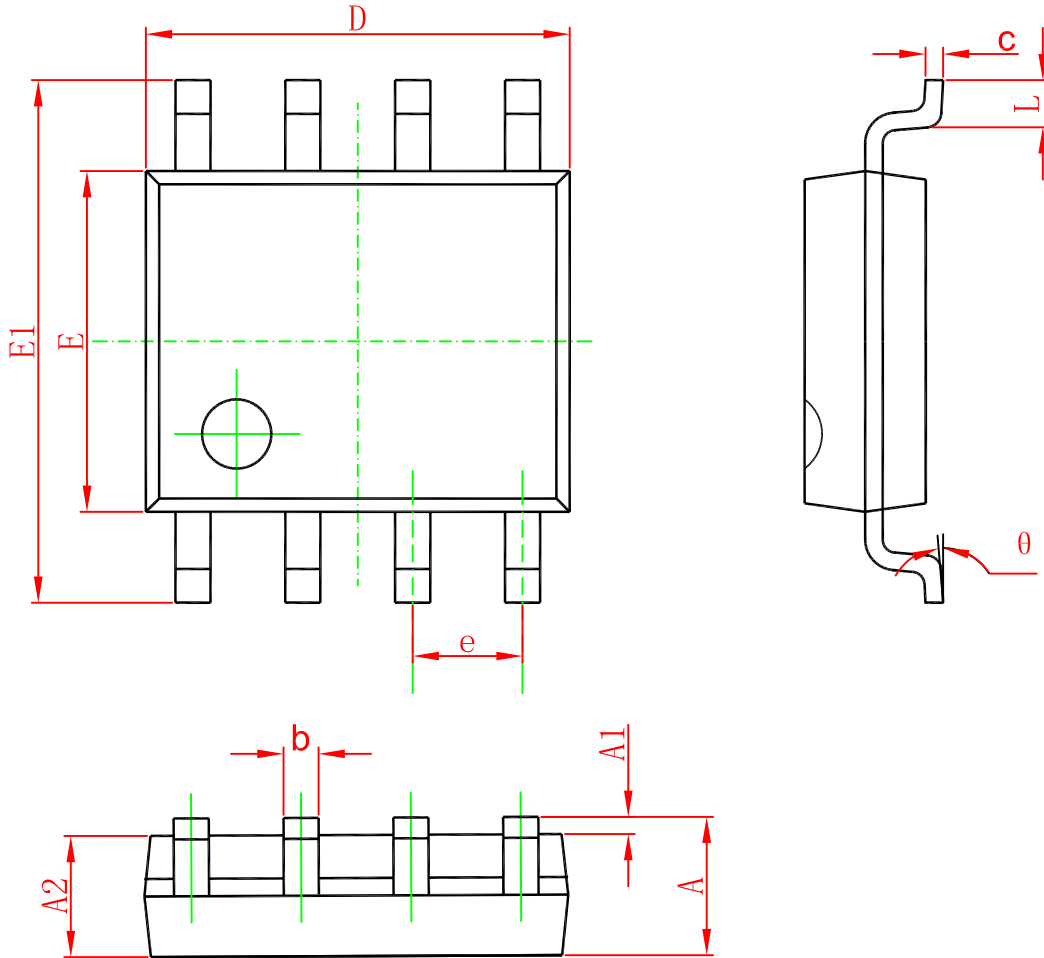
Fig 12b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



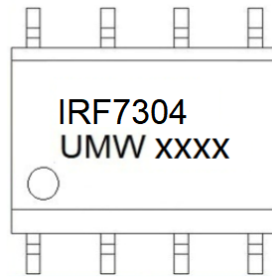
* Reverse Polarity for P-Channel
** Use P-Channel Driver for P-Channel Measurements

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
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[DMN2990UFB-7B](#) [SSM3K35CT,L3F](#) [IPLK60R1K0PFD7ATMA1](#) [2N7002W-G](#) [MCAC30N06Y-TP](#) [IPWS65R035CFD7AXKSA1](#)
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