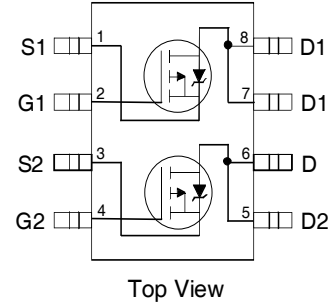


Features

- $V_{DS} (V) = -30V$
- $R_{DS(ON)} < 58m\Omega$ ($V_{GS} = -10V$)
- $R_{DS(ON)} < 98m\Omega$ ($V_{GS} = -4.5V$)
- Generation V Technology
- Ultra Low On-Resistance
- Surface Mount
- Fully Avalanche Rated
- Lead-Free



Description

The SOP-8 has been modified through a customized eadrame for enhanced thermacharacterstics and multiple die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques

Absolute Maximum Ratings ($T_A = 25^\circ C$ Unless Otherwise Noted)

		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ^①	$T_A = 25^\circ C$	I_D	-4.9	A
	$T_A = 70^\circ C$		-3.9	
Pulsed Drain Current		I_{DM}	-30	
Continuous Source Current (Diode Conduction)		I_S	-2.5	
Maximum Power Dissipation ^②	$T_A = 25^\circ C$	P_D	2.0	W
	$T_A = 70^\circ C$		1.3	
Single Pulse Avalanche Energy		E_{AS}	140	mJ
Avalanche Current		I_{AR}	-2.8	A
Repetitive Avalanche Energy		E_{AR}	0.20	mJ
Peak Diode Recovery dv/dt ^③		dv/dt	-5.0	V/ ns
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to + 150	$^\circ C$

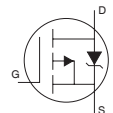
Thermal Resistance Ratings

Parameter	Symbol	Limit	Units
Maximum Junction-to-Ambient ^④	$R_{\theta JA}$	62.5	$^\circ C/W$

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	-30			V	V _{GS} = 0V, I _D = -250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient		0.022		V/°C	Reference to 25°C, I _D = -1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance		42 77	60 100	mΩ	V _{GS} = -10V, I _D = -4.9A ④ V _{GS} = -4.5V, I _D = -3.6A ④
V _{GS(th)}	Gate Threshold Voltage	-1.0			V	V _{DS} = V _{GS} , I _D = -250μA
g _{fs}	Forward Transconductance		7.7		S	V _{DS} = -15V, I _D = -4.9A
I _{DSS}	Drain-to-Source Leakage Current			-1.0 -25	μA	V _{DS} = -24V, V _{GS} = 0V V _{DS} = -24V, V _{GS} = 0V, T _J = 55°C
I _{GSS}	Gate-to-Source Forward Leakage			100	nA	V _{GS} = -20V
	Gate-to-Source Reverse Leakage			-100		V _{GS} = 20V
Q _g	Total Gate Charge		23	34	nC	I _D = -4.9A
Q _{gs}	Gate-to-Source Charge		3.8	5.7		V _{DS} = -15V
Q _{gd}	Gate-to-Drain ("Miller") Charge		5.9	8.9		V _{GS} = -10V, See Fig. 10 ④
t _{d(on)}	Turn-On Delay Time		13	19	ns	V _{DD} = -15V
t _r	Rise Time		13	20		I _D = -1.0A
t _{d(off)}	Turn-Off Delay Time		34	51		R _G = 6.0Ω
t _f	Fall Time		32	48		R _D = 15Ω ④
C _{iss}	Input Capacitance		710		pF	V _{GS} = 0V
C _{oss}	Output Capacitance		380			V _{DS} = -25V
C _{rss}	Reverse Transfer Capacitance		180			f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)			-2.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①			-30		
V _{SD}	Diode Forward Voltage		-0.78	-1.0	V	T _J = 25°C, I _S = -1.7A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time		44	66	ns	T _J = 25°C, I _F = -1.7A
Q _{rr}	Reverse Recovery Charge		42	63	nC	di/dt = 100A/μs ③

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting T_J = 25°C, L = 35mH
R_G = 25Ω, I_{AS} = -2.8A.
- ③ I_{SD} ≤ -2.8A, di/dt ≤ 150A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ Surface mounted on FR-4 board, t ≤ 10sec.

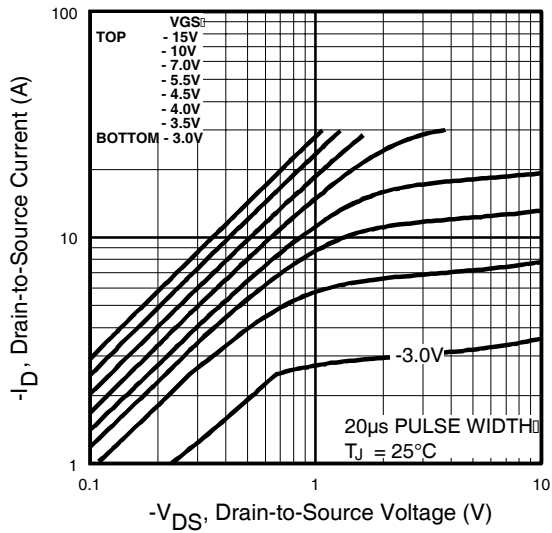


Fig 1. Typical Output Characteristics

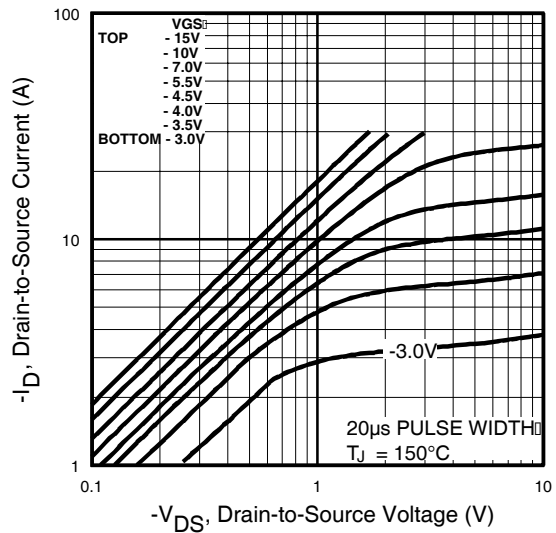


Fig 2. Typical Output Characteristics

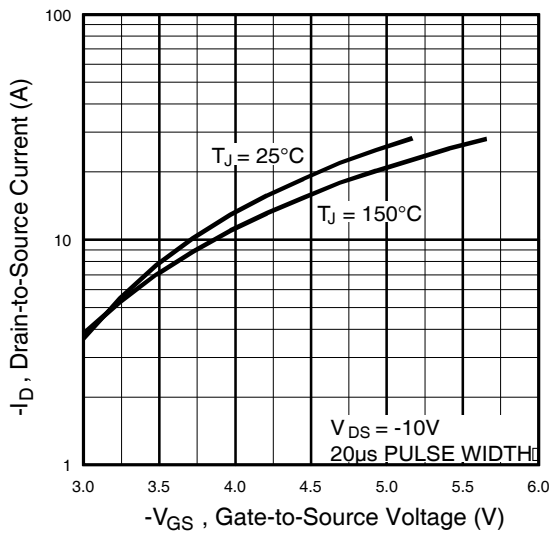


Fig 3. Typical Transfer Characteristics

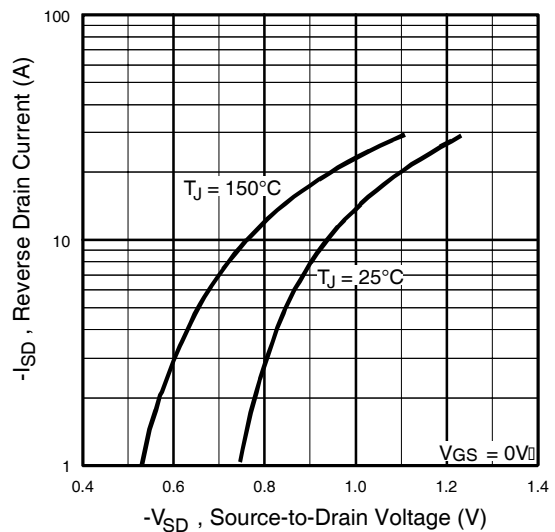


Fig 4. Typical Source-Drain Diode Forward Voltage

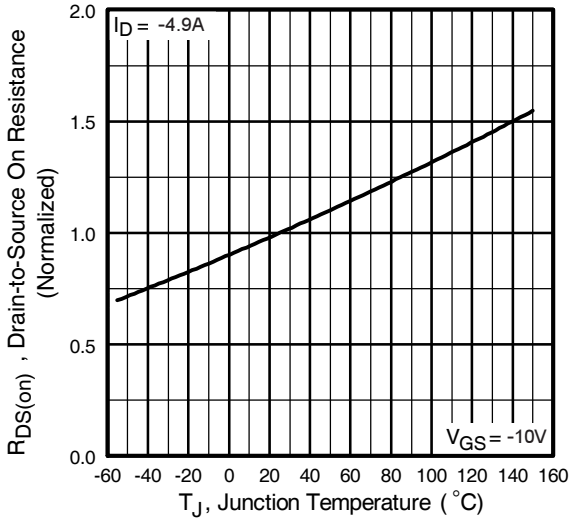


Fig 5. Normalized On-Resistance Vs. Temperature

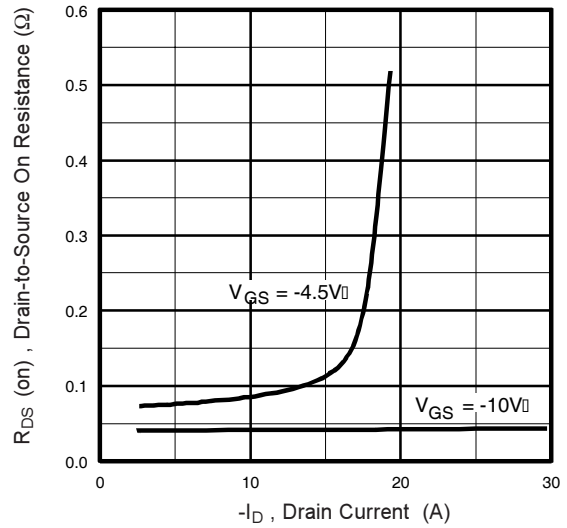


Fig 6. Typical On-Resistance Vs. Drain Current

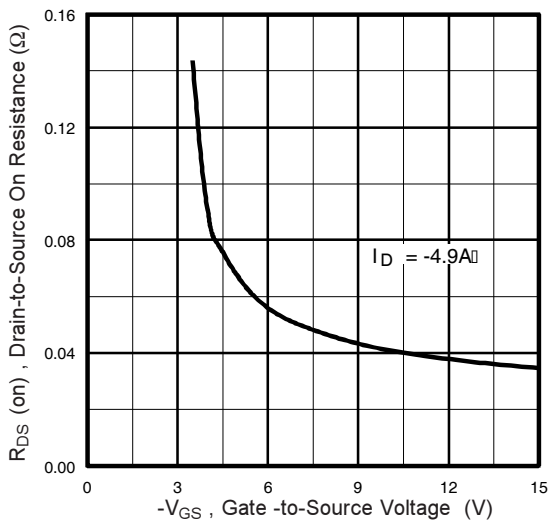


Fig 7. Typical On-Resistance Vs. Gate Voltage

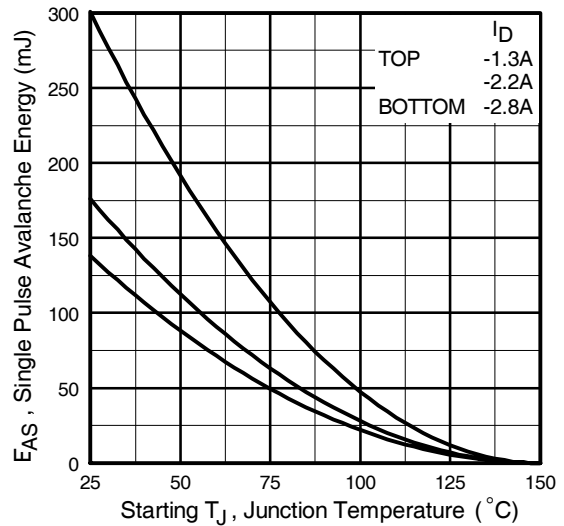


Fig 8. Maximum Avalanche Energy Vs. Drain Current

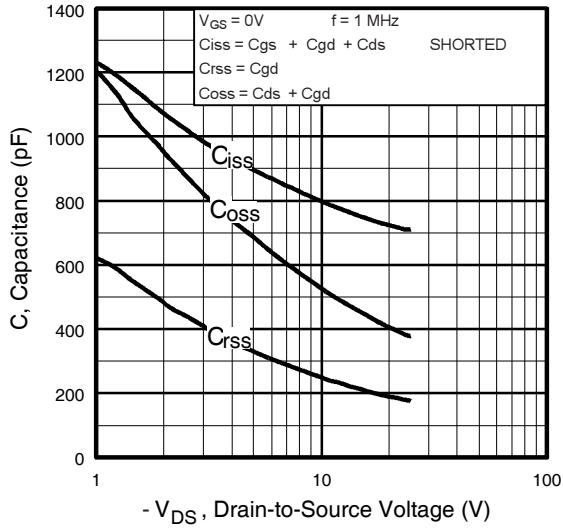


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

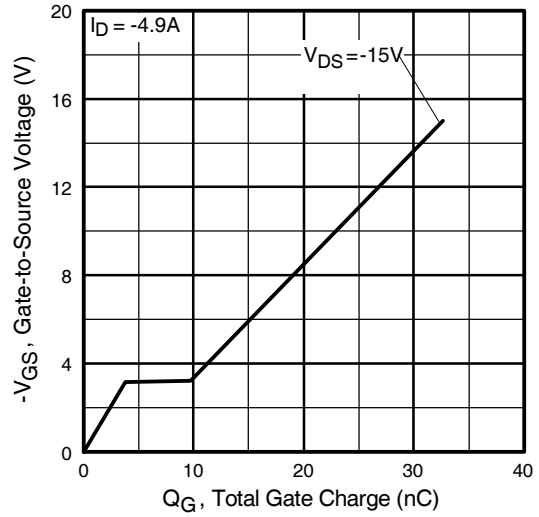


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

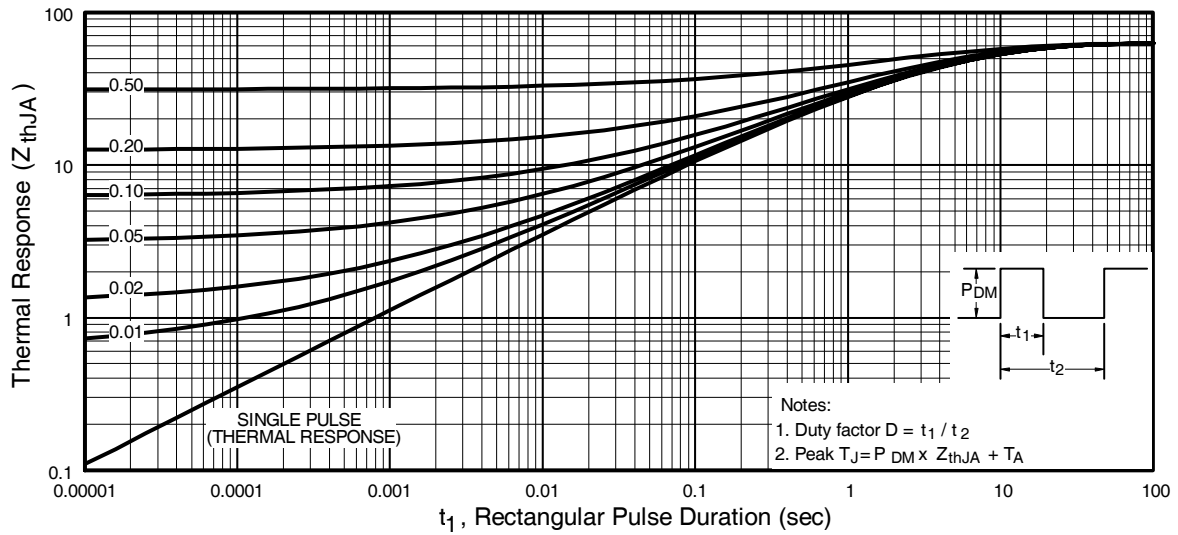
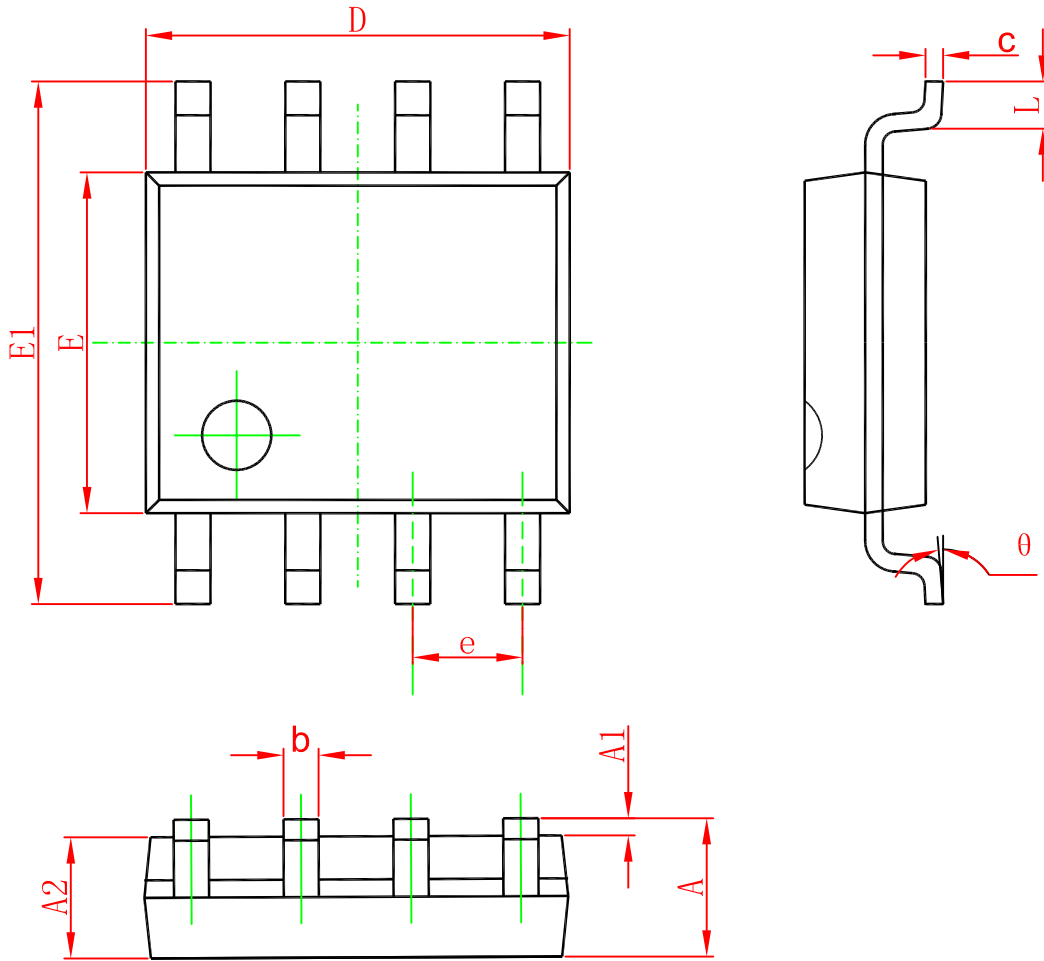


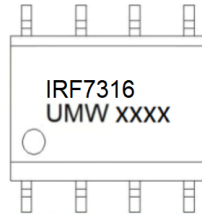
Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Marking



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