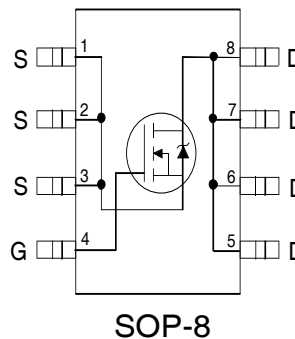


Features

- $V_{DS} (V) = 20V$
- $R_{DS(ON)} < 22\ m\Omega$ ($V_{GS} = 4.5V$)
- Compatible with Existing Surface Mount Techniques
- RoHS Compliant, Halogen-Free

Benefits

- Multi-Vendor Compatibility
- Easier Manufacturing
- Environmentally
- Increased Reliability



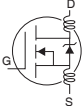
Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_A = 25^\circ C$	10 Sec. Pulsed Drain Current, $V_{GS} @ 4.5V$	10	A
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$	8.7	
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V$	7.0	
I_{DM}	Pulsed Drain Current [Ⓞ]	35	
$P_D @ T_A = 25^\circ C$	Power Dissipation	2.5	W
	Linear Derating Factor	0.02	W/°C
V_{GS}	Gate-to-Source Voltage	± 12	V
dv/dt	Peak Diode Recovery dv/dt [Ⓞ]	5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

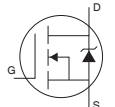
Thermal Resistance Ratings

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient [Ⓞ]		50	°C/W

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	20			V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient		0.044		V/°C	Reference to 25°C, I _D = 1mA
R _{DS(ON)}	Static Drain-to-Source On-Resistance			22 30	mΩ	V _{GS} = 4.5V, I _D = 4.1A ③ V _{GS} = 2.7V, I _D = 3.5A ③
V _{GS(th)}	Gate Threshold Voltage	0.70			V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	11			S	V _{DS} = 15V, I _D = 4.1A
I _{DSS}	Drain-to-Source Leakage Current			1.0 25	μA	V _{DS} = 16V, V _{GS} = 0V V _{DS} = 16V, V _{GS} = 0V, T _J = 125 °C
I _{GSS}	Gate-to-Source Forward Leakage			100	nA	V _{GS} = 12V
	Gate-to-Source Reverse Leakage			-100	nA	V _{GS} = -12V
Q _g	Total Gate Charge			48	nC	I _D = 4.1A
Q _{gs}	Gate-to-Source Charge			5.1	nC	V _{DS} = 16V
Q _{gd}	Gate-to-Drain ("Miller") Charge			20	nC	V _{GS} = 4.5V, See Fig. 6 and 12 ③
t _{d(on)}	Turn-On Delay Time		13		ns	V _{DD} = 10V I _D = 4.1A R _G = 6.0Ω R _D = 2.4Ω, See Fig. 10 ③
t _r	Rise Time		72			
t _{d(off)}	Turn-Off Delay Time		65			
L	Internal Drain Inductance		2.5			
t _{fD}	Fall Time		92		nH	Between lead tip and center of die contact 
L _S	Internal Source Inductance		4.0			
C _{iss}	Input Capacitance		1600		pF	V _{GS} = 0V V _{DS} = 15V f = 1.0MHz, See Fig.
C _{oss}	Output Capacitance		690			
C _{rss}	Reverse Transfer Capacitance		310			

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)			3.1	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①			35		
V _{SD}	Diode Forward Voltage			1.0	V	T _J = 25°C, I _S = 2.0A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time		39	59	ns	T _J = 25°C, I _F = 4.1A
Q _{rr}	Reverse Recovery Charge		42	63	nC	di/dt = 100A/μs ③
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② I_{SD} ≤ 4.1A, di/dt ≤ 100A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 150°C
- ③ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ④ Surface mounted on FR-4 board, t ≤ 10sec.

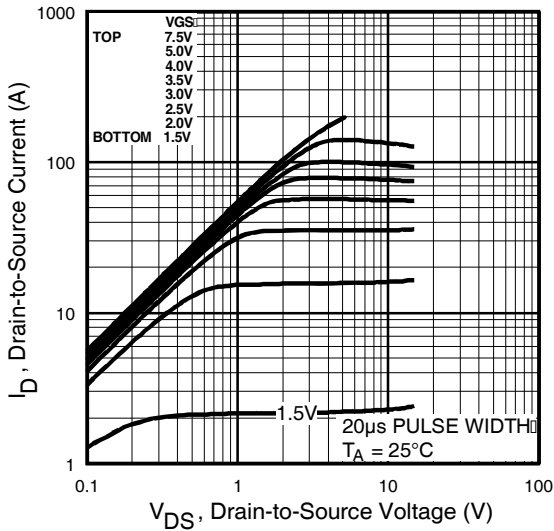


Fig 1. Typical Output Characteristics

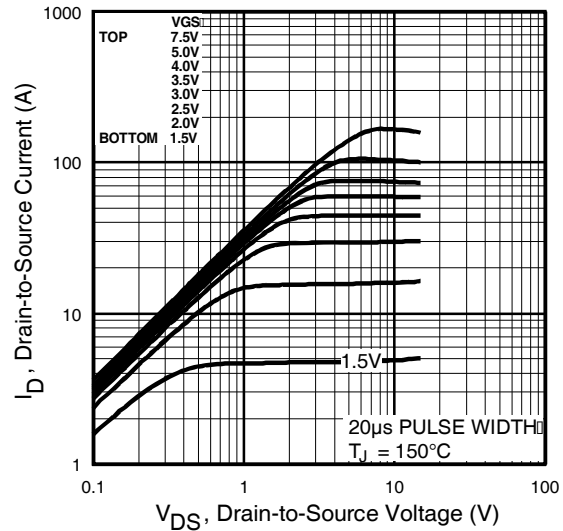


Fig 2. Typical Output Characteristics

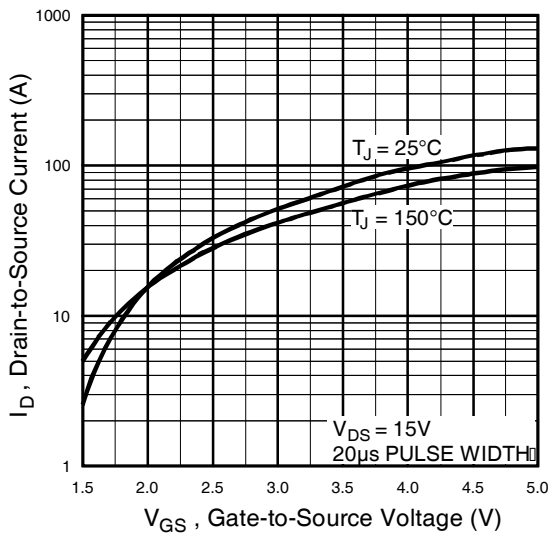


Fig 3. Typical Transfer Characteristics

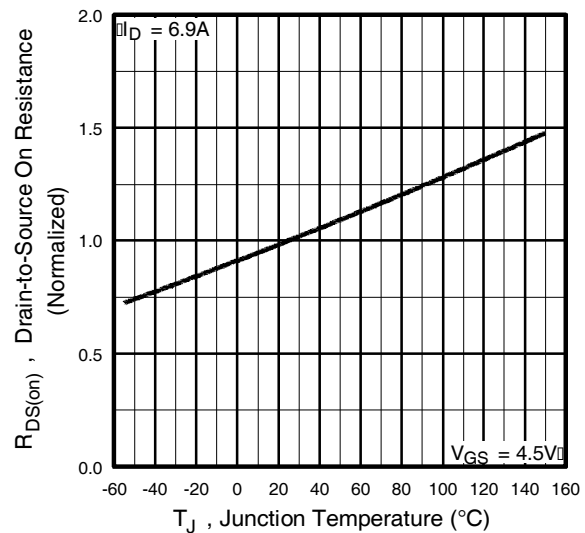


Fig 4. Normalized On-Resistance Vs. Temperature

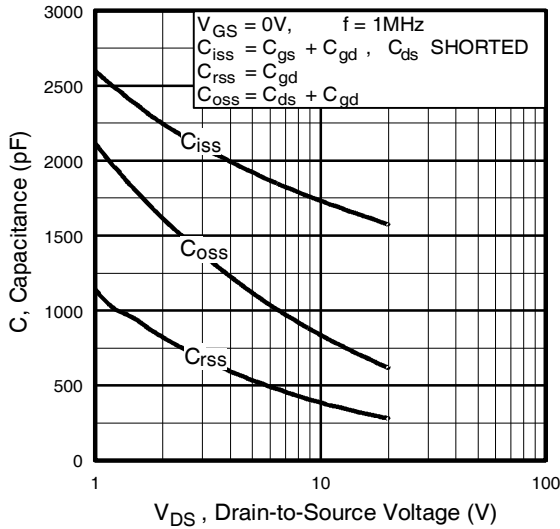


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

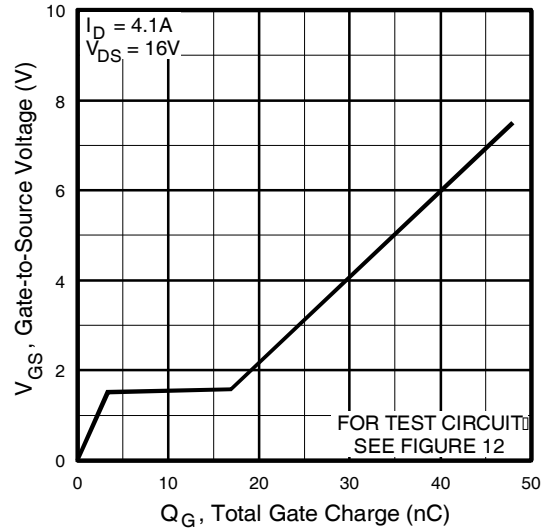


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

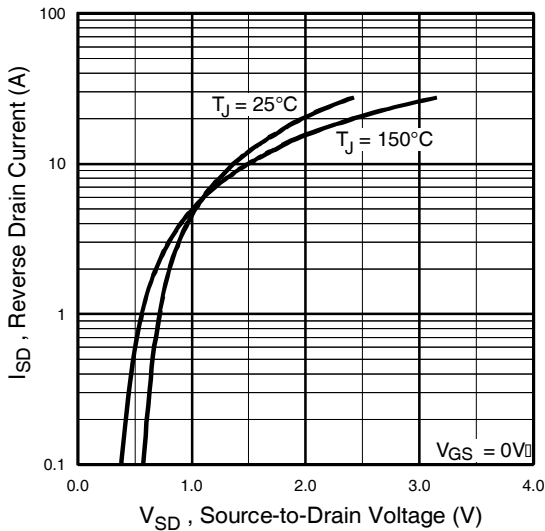


Fig 7. Typical Source-Drain Diode Forward Voltage

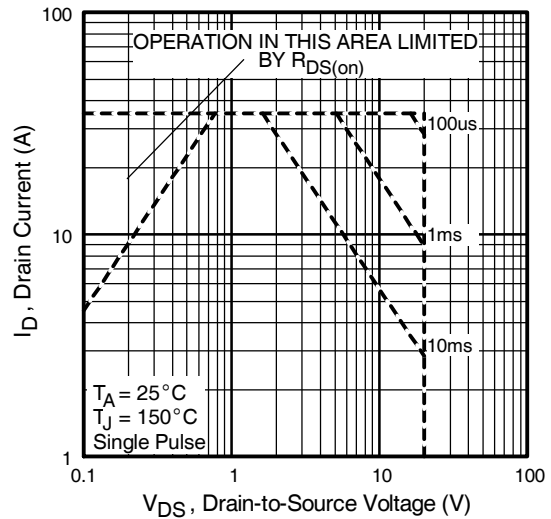


Fig 8. Maximum Safe Operating Area

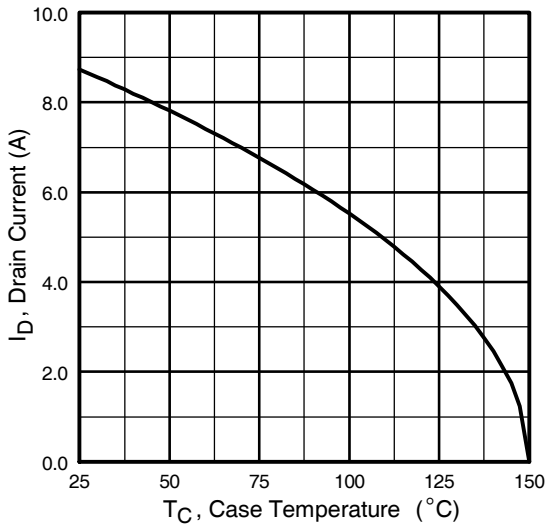


Fig 9. Maximum Drain Current Vs. Ambient Temperature

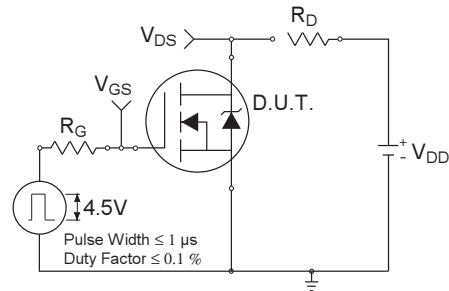


Fig 10a. Switching Time Test Circuit

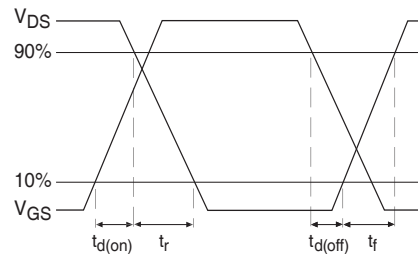


Fig 10b. Switching Time Waveforms

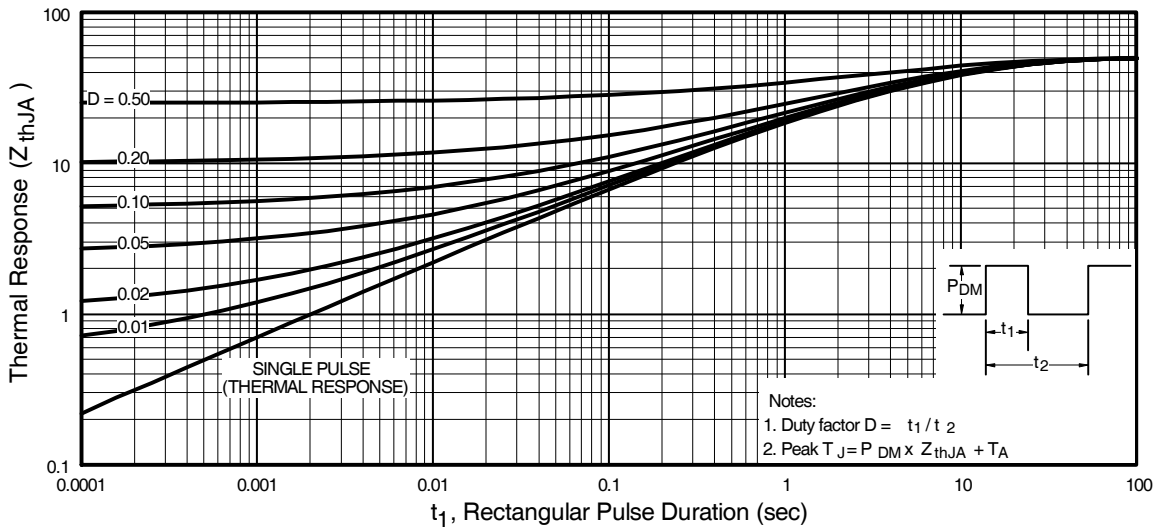


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

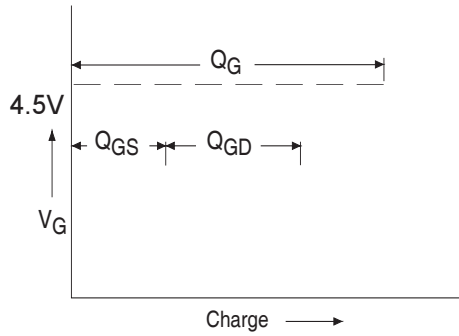


Fig 12a. Basic Gate Charge Waveform

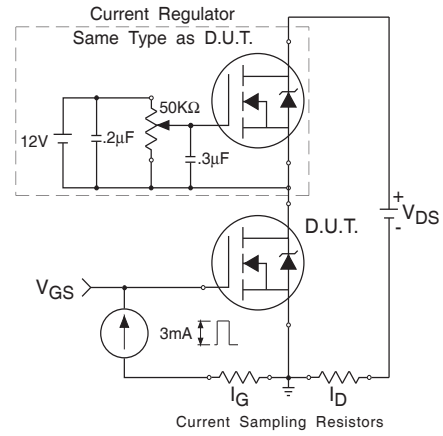
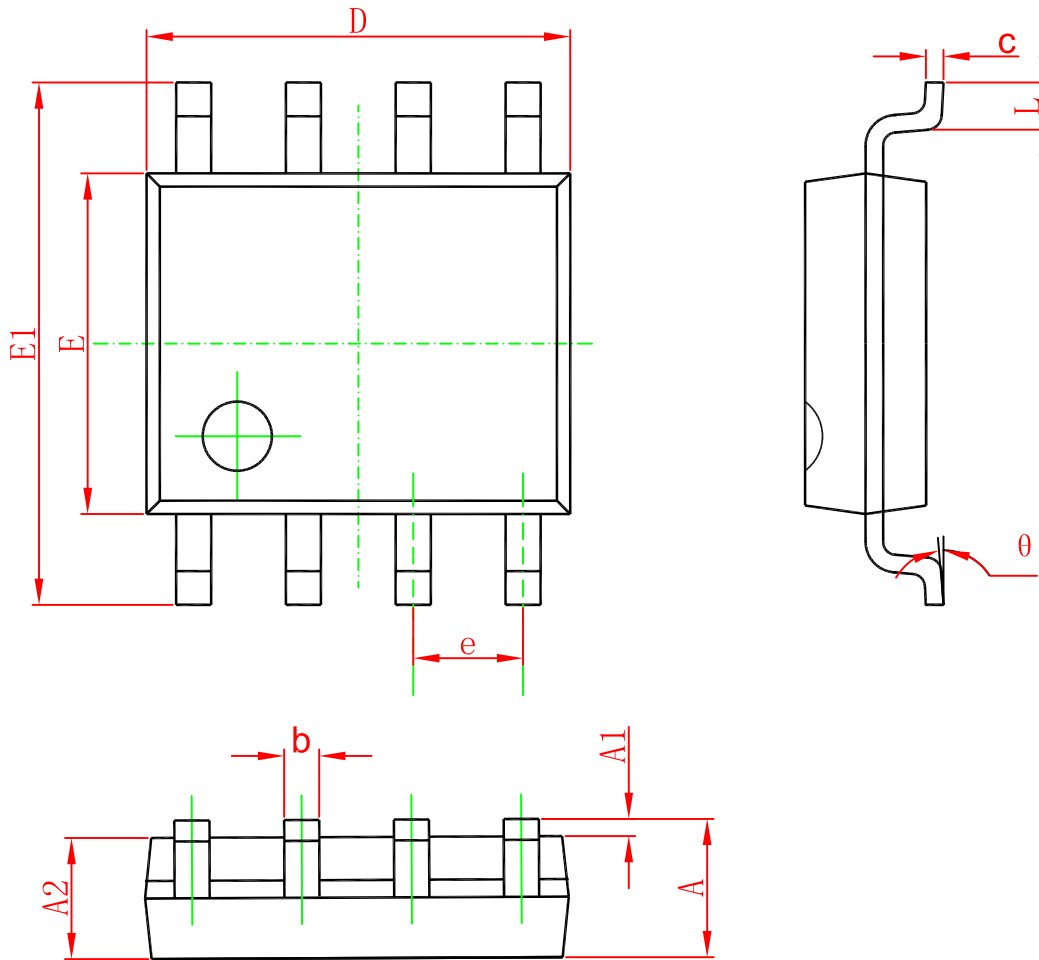


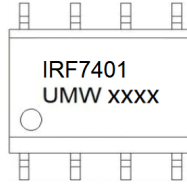
Fig 12b. Gate Charge Test Circuit

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
theta	0°	8°	0°	8°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
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