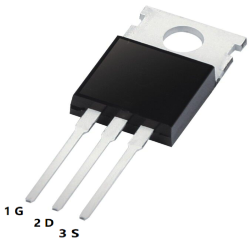
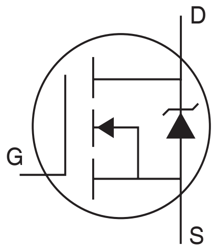
Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free
- Halogen-Free



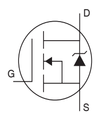
- V_{DS} = 100V
- I_D =120A
- $R_{DS(ON)}$ (at V_{GS}=10V) <6mΩ

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	127①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	90①	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V(Wire Bond Limited)	120	
I_{DM}	Pulsed Drain Current ②	560	
P_D @T_C = 25°C	Maximum Power Dissipation	250	W
	Linear Derating Factor	1.7	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ④	18	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	130	mJ
I_{AR}	Avalanche Current ①	See Fig. 14, 15, 22a, 22b,	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧		0.6	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.50		
$R_{\theta JA}$	Junction-to-Ambient ⑧⑨		62	

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100			V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient		0.11		V/°C	Reference to 25°C, I_D = 5mA②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance		4.8	6.0	mΩ	V_{GS} = 10V, I_D = 75A ⑤
$V_{GS(th)}$	Gate Threshold Voltage	2.0		4.0	V	V_{DS} = V_{GS}, I_D = 150μA
I_{DSS}	Drain-to-Source Leakage Current			20	μA	V_{DS} = 100V, V_{GS} = 0V
				250		V_{DS} = 80V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage			100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage			-100		V_{GS} = -20V
R_G	Internal Gate Resistance		0.7		Ω	
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
gfs	Forward Transconductance	150			S	V_{DS} = 50V, I_D = 75A
Q_g	Total Gate Charge		120	170	nC	I_D = 75A
Q_{gs}	Gate-to-Source Charge		29			V_{DS} =50V
Q_{gd}	Gate-to-Drain ("Miller") Charge		35			V_{GS} = 10V ⑤
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})		85			I_D = 75A, V_{DS} =0V, V_{GS} = 10V
$t_{d(on)}$	Turn-On Delay Time		20		ns	V_{DD} = 65V
t_r	Rise Time		60			I_D = 75A
$t_{d(off)}$	Turn-Off Delay Time		55			R_G = 2.7Ω
t_f	Fall Time		57			V_{GS} = 10V ⑤
C_{iss}	Input Capacitance		6860		pF	V_{GS} = 0V
C_{oss}	Output Capacitance		490			V_{DS} = 50V
C_{rss}	Reverse Transfer Capacitance		220			ƒ = 1.0MHz, See Fig. 5
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)		570			V_{GS} = 0V, V_{DS} = 0V to 80V ⑦, See Fig. 11
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)⑥		920			V_{GS} = 0V, V_{DS} = 0V to 80V ⑥
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
I_S	Continuous Source Current (Body Diode)			127①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②			560	A	
V_{SD}	Diode Forward Voltage			1.3	V	T_J = 25°C, I_S = 75A, V_{GS} = 0V ⑤
t_{rr}	Reverse Recovery Time		40		ns	T_J = 25°C V_R = 85V,
		49				T_J = 125°C I_F = 75A
Q_{rr}	Reverse Recovery Charge		58		nC	T_J = 25°C di/dt = 100A/μs ⑤
			89			T_J = 125°C
I_{RRM}	Reverse Recovery Current		2.5		A	T_J = 25°C
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 120A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by T_{Jmax}, starting T_J = 25°C, L = 0.047mH R_G = 25Ω, I_{AS} = 75A, V_{GS} =10V. Part not recommended for use above the Eas value and test conditions.

④ I_{SD} ≤ 75A, di/dt ≤ 600A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C.

⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑧ $R_θ$ is measured at T_J approximately 90°C.

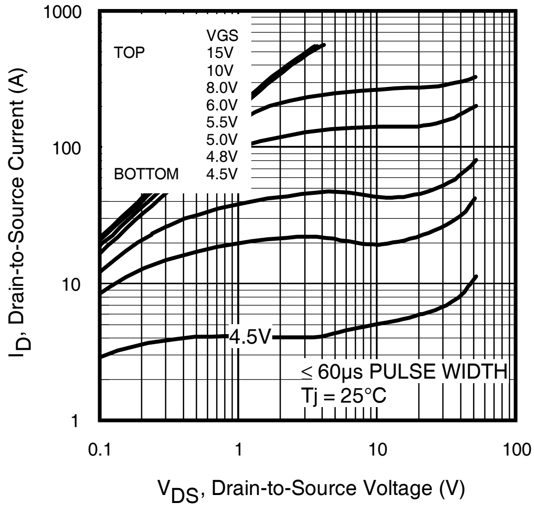


Fig 1. Typical Output Characteristics

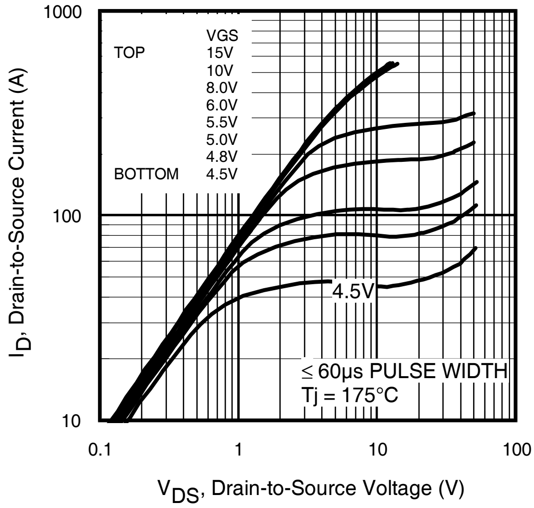


Fig 2. Typical Output Characteristics

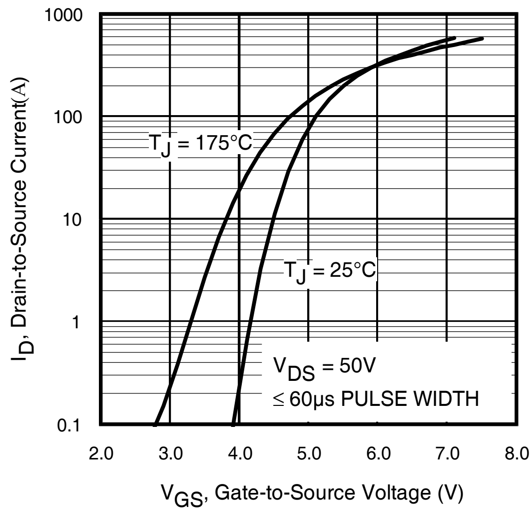


Fig 3. Typical Transfer Characteristics

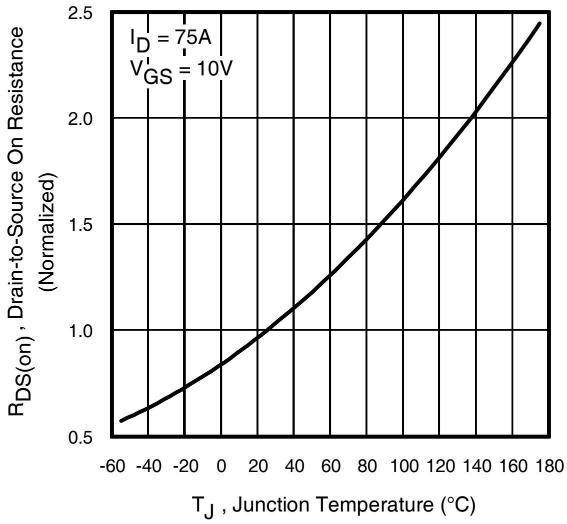


Fig 4. Normalized On-Resistance vs. Temperature

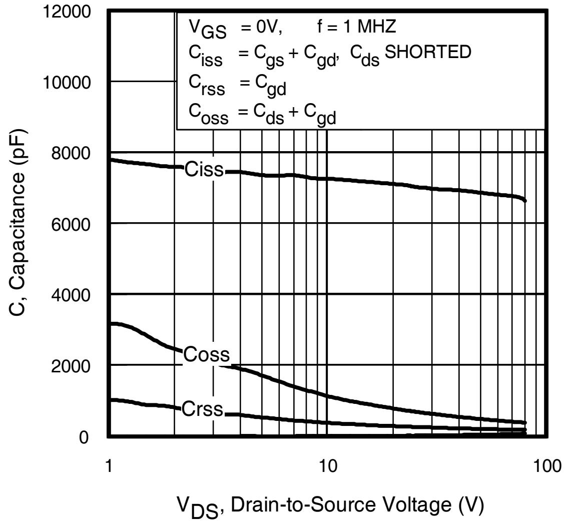


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

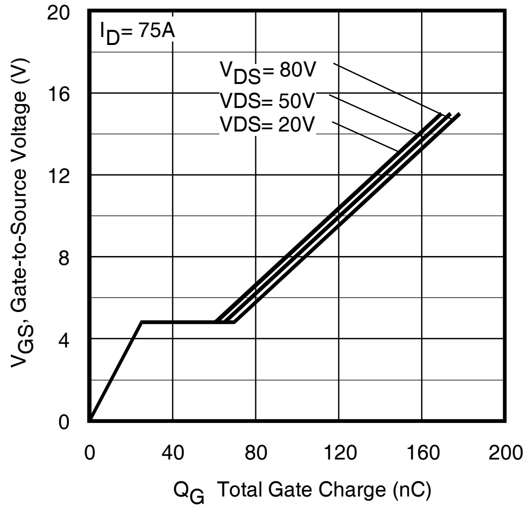


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

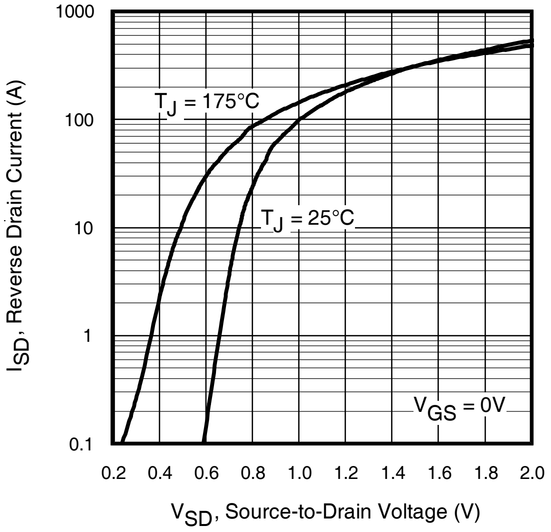


Fig 7. Typical Source-Drain Diode Forward Voltage

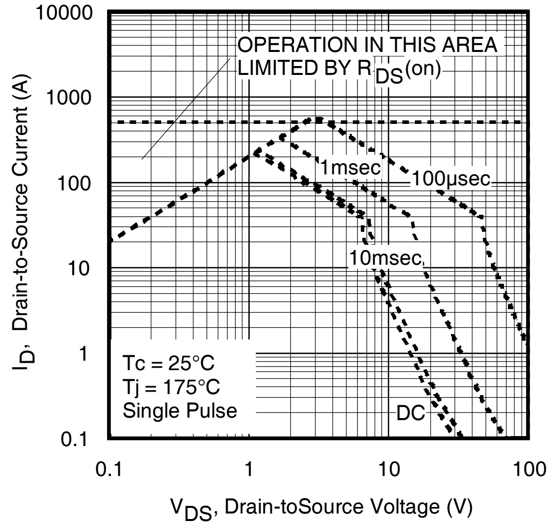


Fig 8. Maximum Safe Operating Area

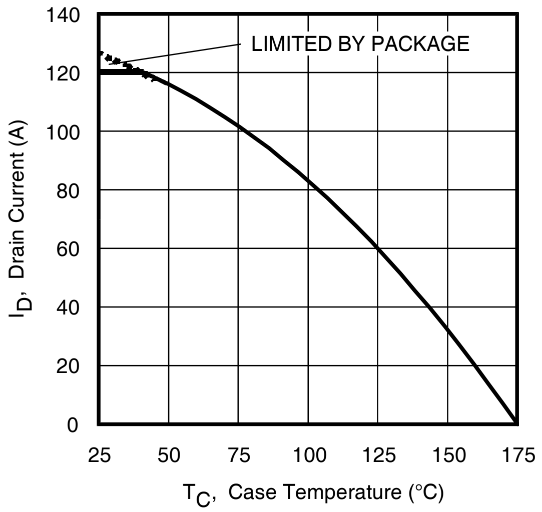


Fig 9. Maximum Drain Current vs. Case Temperature

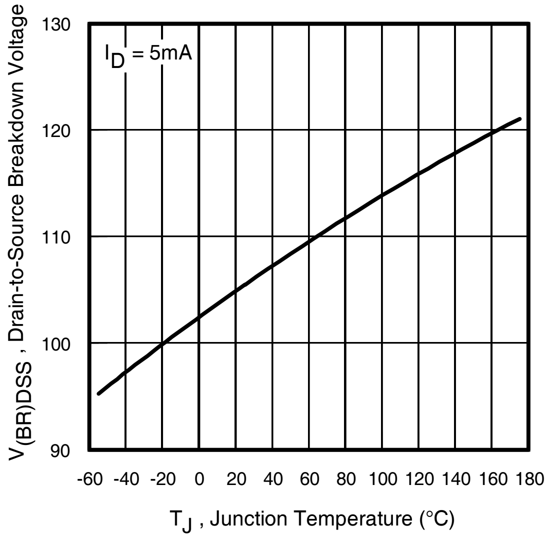


Fig 10. Drain-to-Source Breakdown Voltage

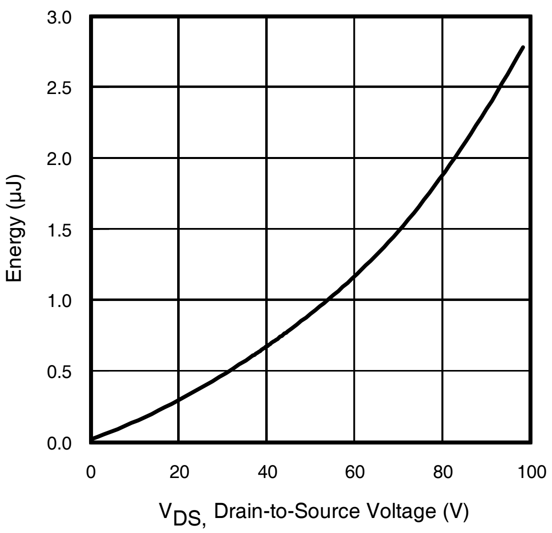


Fig 11. Typical C_{OSS} Stored Energy

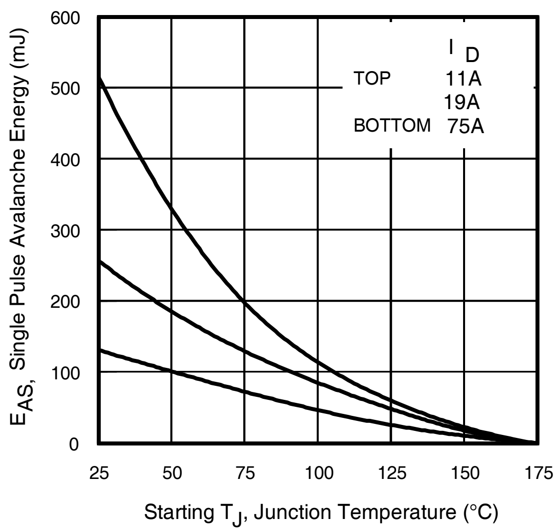


Fig 12. Maximum Avalanche Energy Vs. DrainCurrent

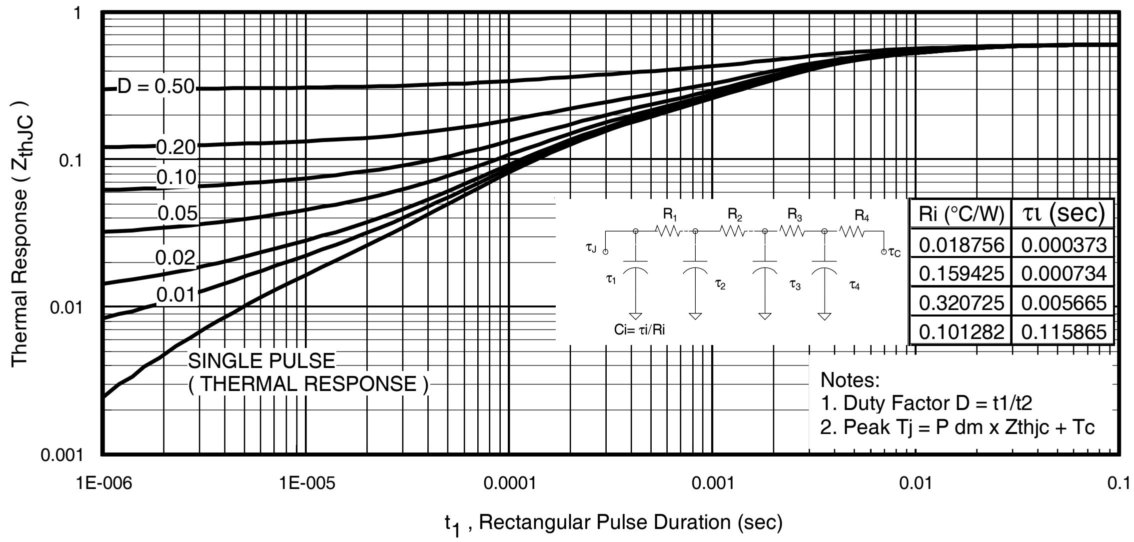


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

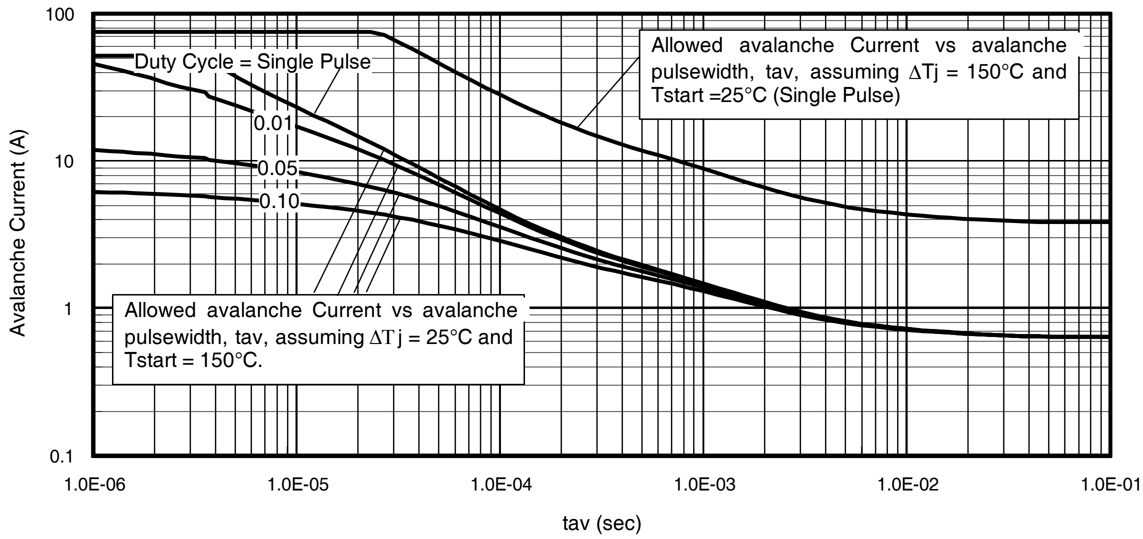


Fig 14. Typical Avalanche Current vs.Pulsewidth

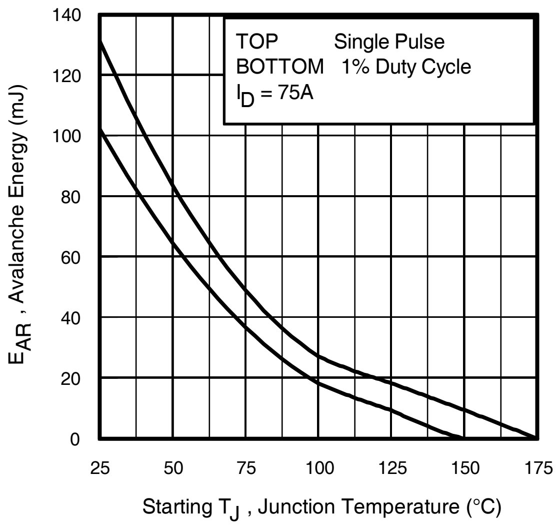


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

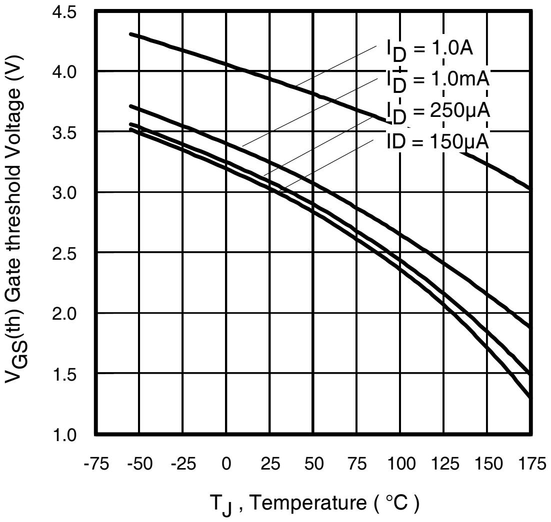


Fig 16. Threshold Voltage Vs. Temperature

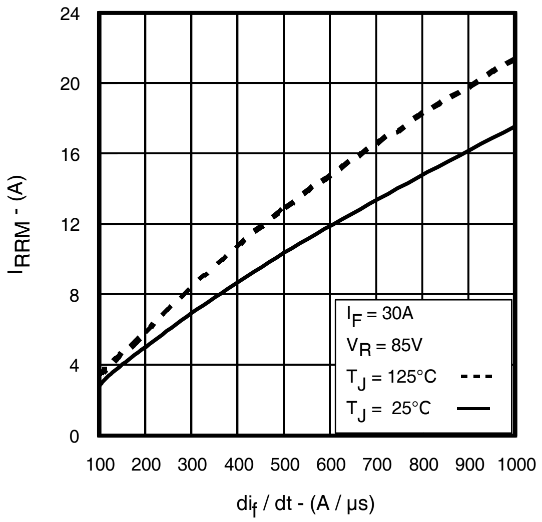


Fig. 17 - Typical Recovery Current vs. di_f/dt

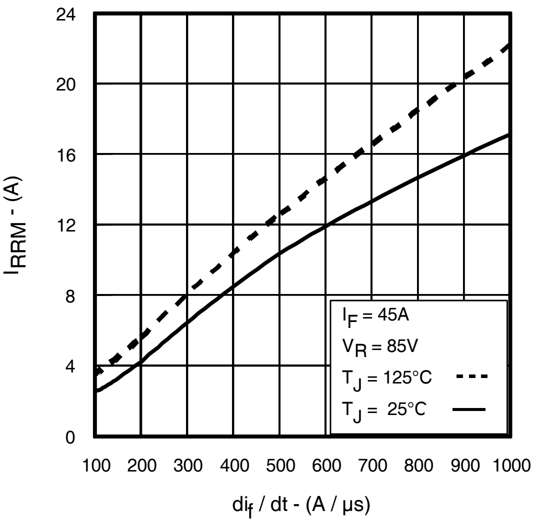


Fig. 18 - Typical Recovery Current vs. di_f/dt

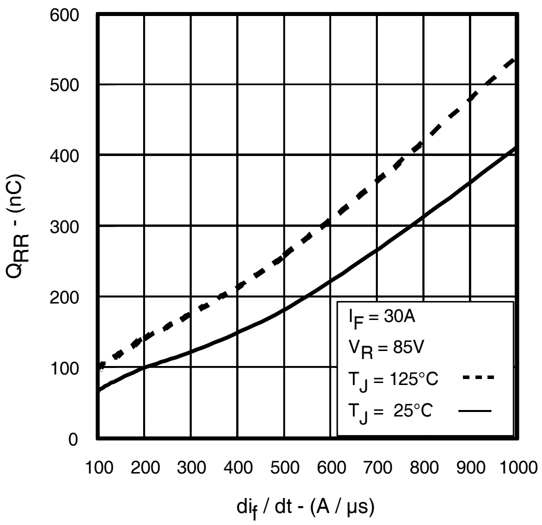


Fig. 19 - Typical Stored Charge vs. di_f/dt

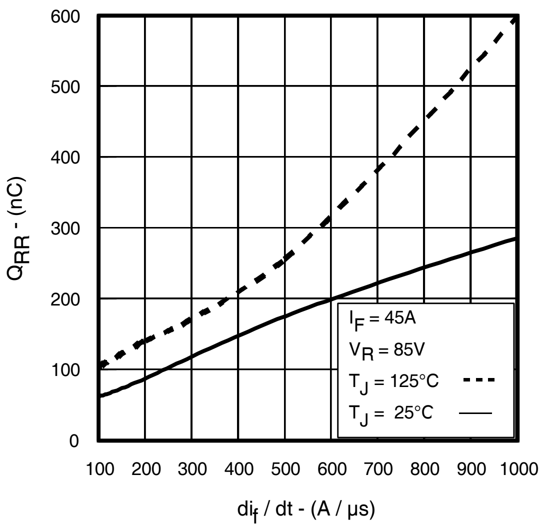


Fig. 20 - Typical Stored Charge vs. di_f/dt

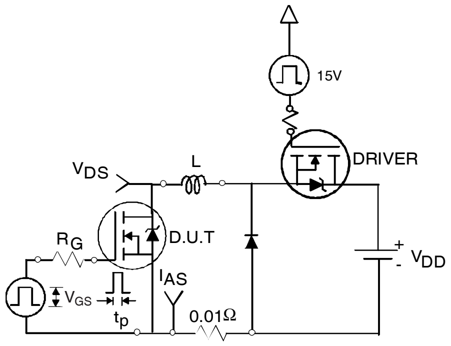


Fig 21a. Unclamped Inductive Test Circuit

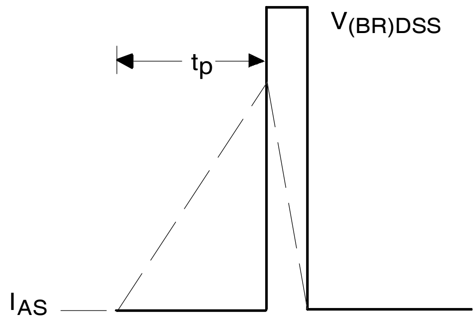


Fig 21b. Unclamped Inductive Waveforms

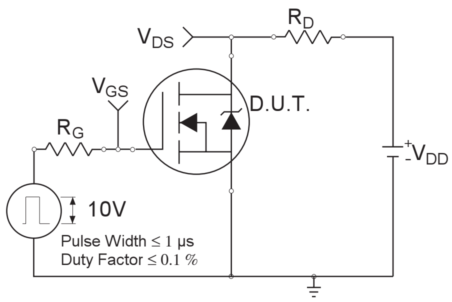


Fig 22a. Switching Time Test Circuit

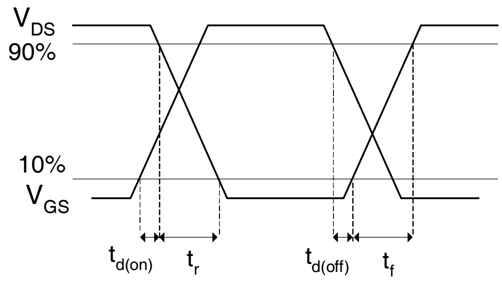


Fig 22b. Switching Time Waveforms

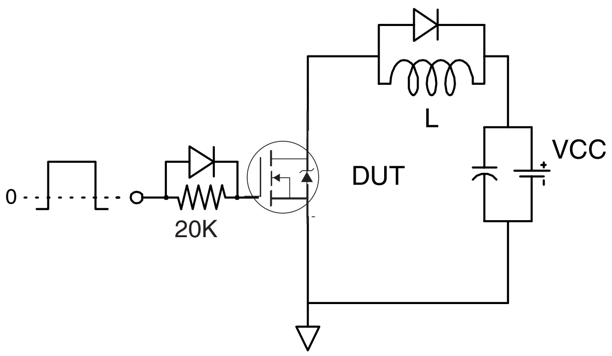


Fig 23a. Gate Charge Test Circuit

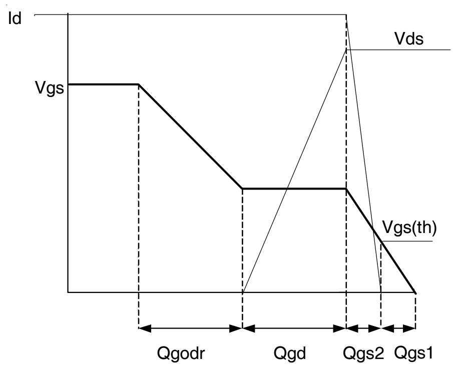
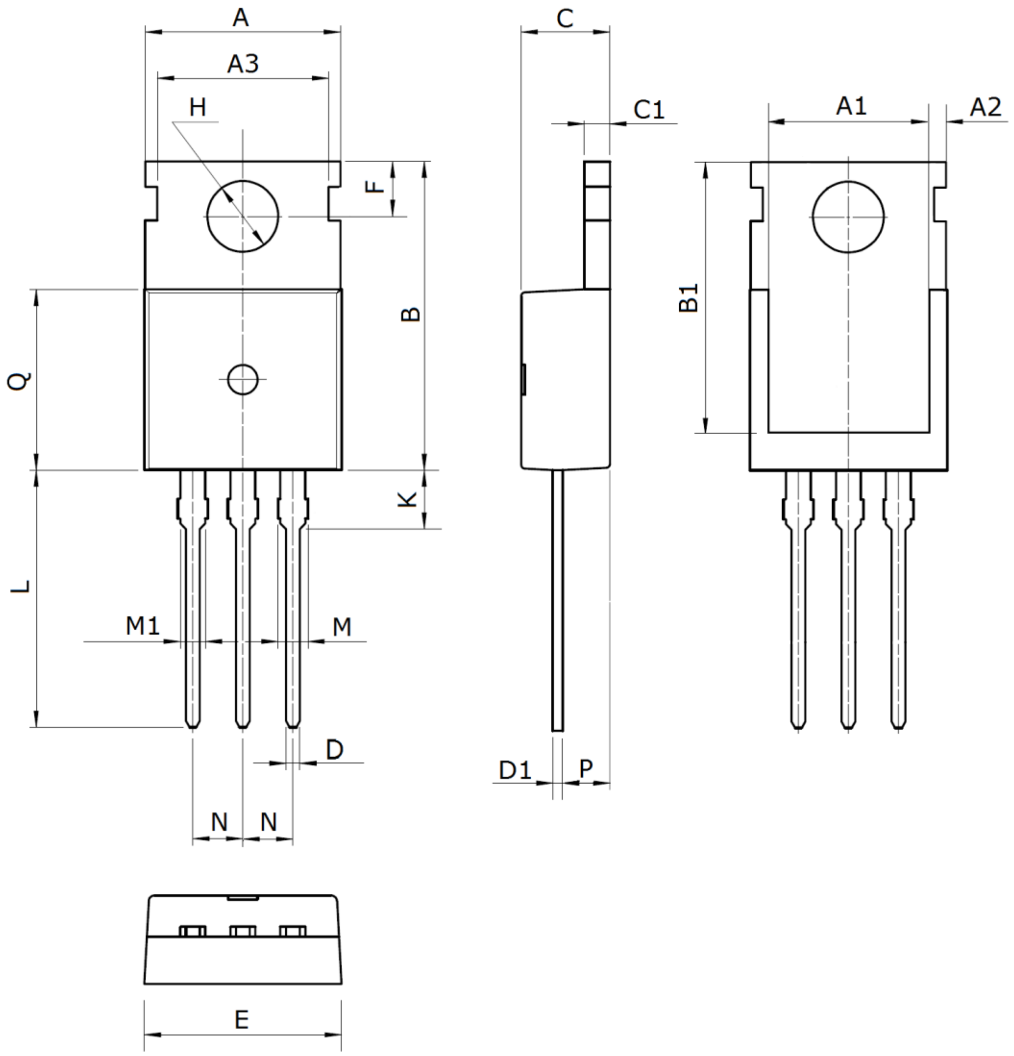


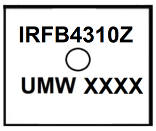
Fig 23b. Gate Charge Waveform

Package Mechanical Data TO-220



Symbol	Dimensions （mm）	Symbol	Dimensions (mm)	Symbol	Dimensions (mm)
A	10.0±0.3	C1	1.3±0.2	L	13.2±0.4
A1	8.0±0.2	D	0.8±0.2	M	1.38±0.1
A2	0.94±0.1	D1	0.5±0.1	M1	1.28±0.1
A3	8.7±0.1	E	10.0±0.3	N	2.54(typ)
B	15.6±0.4	F	2.8 ±0.1	P	2.4±0.3
B1	13.2 ±0.2	H	3.6±0.1	Q	9.15±0. 25
C	4.5±0. 2	K	3.1±0.2		

Marking



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