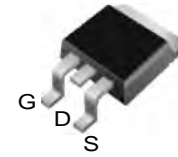


Applications

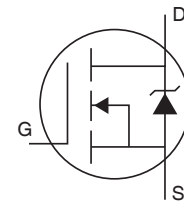
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



TO-263

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free
- RoHS Compliant, Halogen-Free
- $V_{DS} = 100V$
- I_D (at $V_{GS} = 10V$) = 97A
- $R_{DS(ON)}$ (at $V_{GS} = 10V$) < 9m Ω



Absolute Maximum Ratings

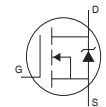
Symbol	Parameter	Max.		Units
I_D @ $T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	97		A
I_D @ $T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	69		
I_{DM}	Pulsed Drain Current ①	390		
P_D @ $T_C = 25^\circ C$	Maximum Power Dissipation	230		W
	Linear Derating Factor	1.5		W/ $^\circ C$
V_{GS}	Gate-to-Source Voltage	± 20		V
dv/dt	Peak Diode Recovery ③	16		V/ns
T_J	Operating Junction and	-55 to + 175		$^\circ C$
T_{STG}	Storage Temperature Range			
	Soldering Temperature, for 10 seconds (1.6mm from case)	300		
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)		
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	242		mJ
I_{AR}	Avalanche Current	See Fig. 14, 15, 22a, 22b,		A
E_{AR}	Repetitive Avalanche Energy ④			mJ
Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑤		0.65	$^\circ C/W$
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface, TO-220	0.50		
$R_{\theta JA}$	Junction-to-Ambient, TO-220 ⑥		62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount), D ² Pak ⑦ ⑧		40	

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	100			V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient		0.12		V/°C	Reference to 25°C, I _D = 5mA①
R _{DS(on)}	Static Drain-to-Source On-Resistance		7.2	9.0	mΩ	V _{GS} = 10V, I _D = 58A ④
V _{GS(th)}	Gate Threshold Voltage	2.0		4.0	V	V _{DS} = V _{GS} , I _D = 150μA
I _{DSS}	Drain-to-Source Leakage Current			20	μA	V _{DS} = 100V, V _{GS} = 0V
				250		V _{DS} = 80V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage			100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage			-100		V _{GS} = -20V
R _G	Internal Gate Resistance		0.70		Ω	
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	140			S	V _{DS} = 10V, I _D = 58A
Q _g	Total Gate Charge		83	120	nC	I _D = 58A
Q _{gs}	Gate-to-Source Charge		19			V _{DS} = 50V
Q _{gd}	Gate-to-Drain ("Miller") Charge		27			V _{GS} = 10V ④
Q _{sync}	Total Gate Charge Sync. (Q _g - Q _{gd})		56			I _D = 58A, V _{DS} = 0V, V _{GS} = 10V ④
t _{d(on)}	Turn-On Delay Time		16		ns	V _{DD} = 65V
t _r	Rise Time		52			I _D = 58A
t _{d(off)}	Turn-Off Delay Time		43			R _G = 2.7Ω
t _f	Fall Time		57			V _{GS} = 10V ④
C _{iss}	Input Capacitance		4820		pF	V _{GS} = 0V
C _{oss}	Output Capacitance		340			V _{DS} = 50V
C _{rss}	Reverse Transfer Capacitance		170			f = 1.0MHz, See Fig.5
C _{oss eff. (ER)}	Effective Output Capacitance (Energy Related) ⑥		420			V _{GS} = 0V, V _{DS} = 0V to 80V ⑥, See Fig.11
C _{oss eff. (TR)}	Effective Output Capacitance (Time Related) ⑤		690			V _{GS} = 0V, V _{DS} = 0V to 80V ⑤
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)			97	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①			390	A	
V _{SD}	Diode Forward Voltage			1.3	V	T _J = 25°C, I _S = 58A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time		38	57	ns	T _J = 25°C V _R = 85V, T _J = 125°C I _F = 58A
Q _{rr}	Reverse Recovery Charge		53	80	nC	T _J = 25°C T _J = 125°C di/dt = 100A/μs ④
I _{RRM}	Reverse Recovery Current		2.5		A	T _J = 25°C
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.143mH
R_G = 25Ω, I_{AS} = 58A, V_{GS} = 10V. Part not recommended for use above this value.
- ③ I_{SD} ≤ 58A, di/dt ≤ 610A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C.
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ C_{oss eff. (TR)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑥ C_{oss eff. (ER)} is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑦ R_θ is measured at T_J approximately 90°C.



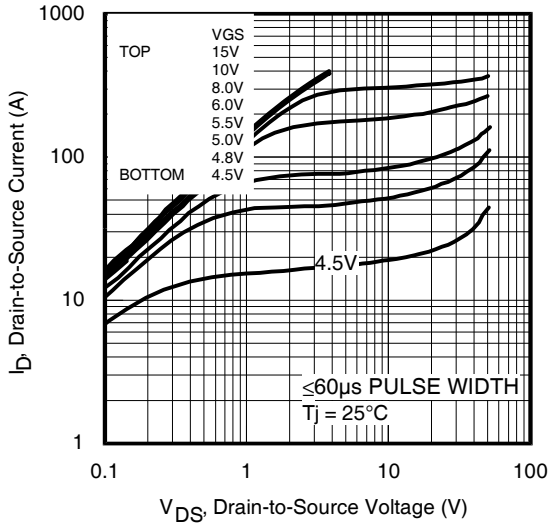


Fig 1. Typical Output Characteristics

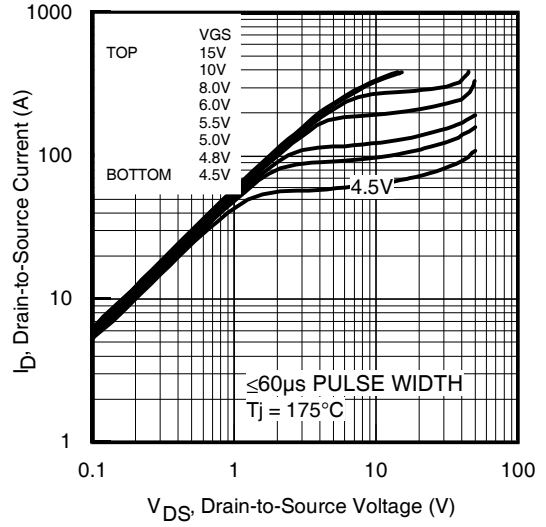


Fig 2. Typical Output Characteristics

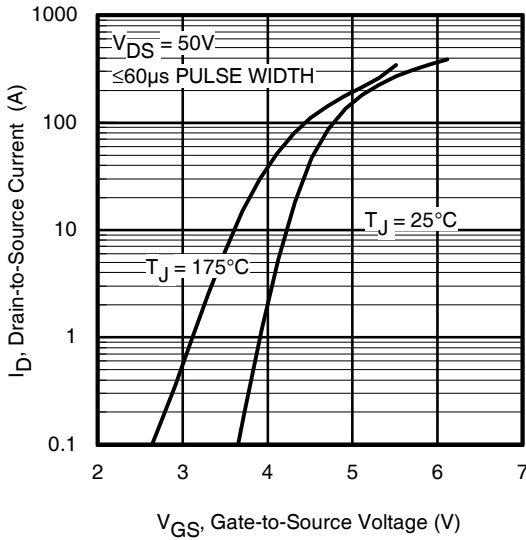


Fig 3. Typical Transfer Characteristics

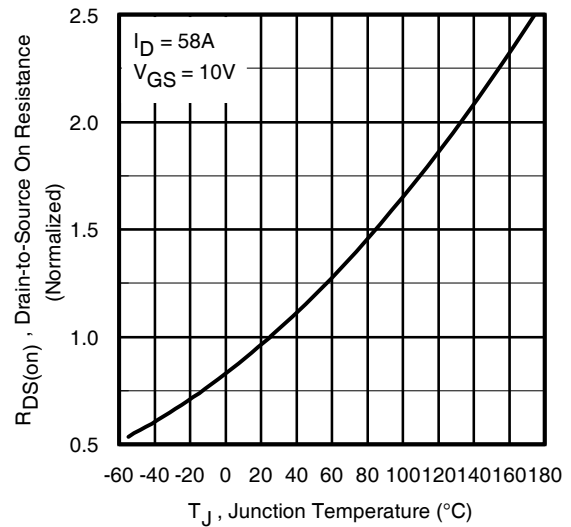


Fig 4. Normalized On-Resistance vs. Temperature

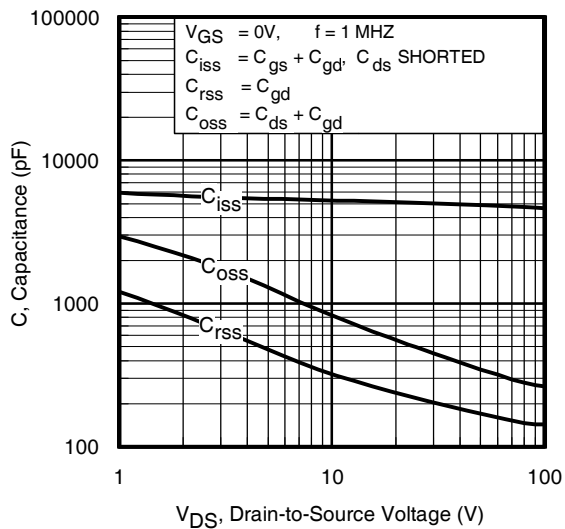


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

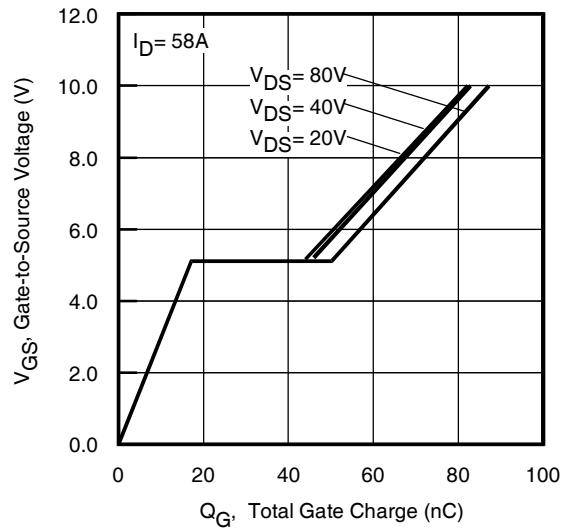


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

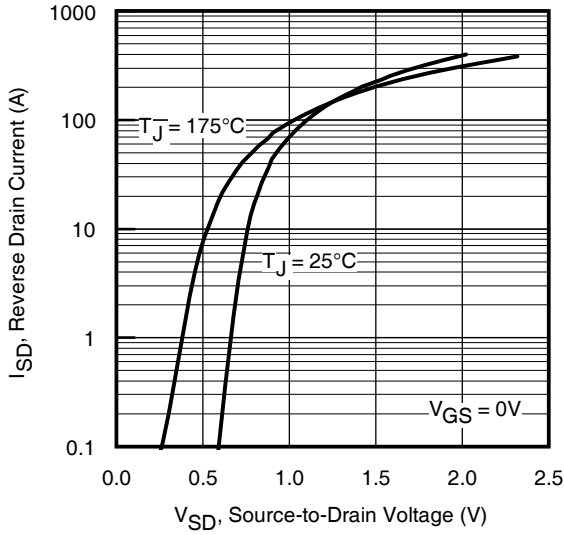


Fig 7. Typical Source-Drain Diode Forward Voltage

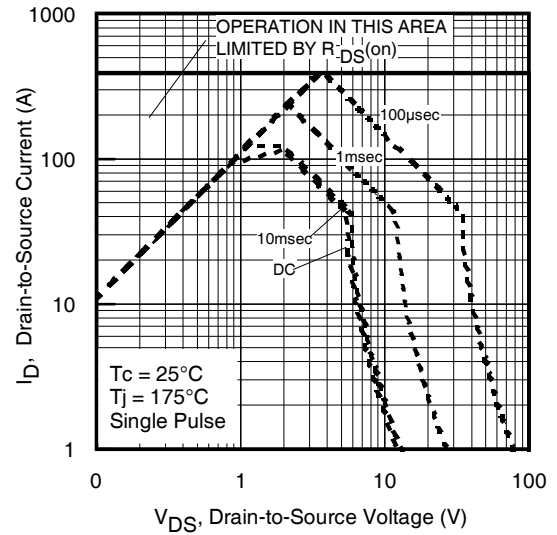


Fig 8. Maximum Safe Operating Area

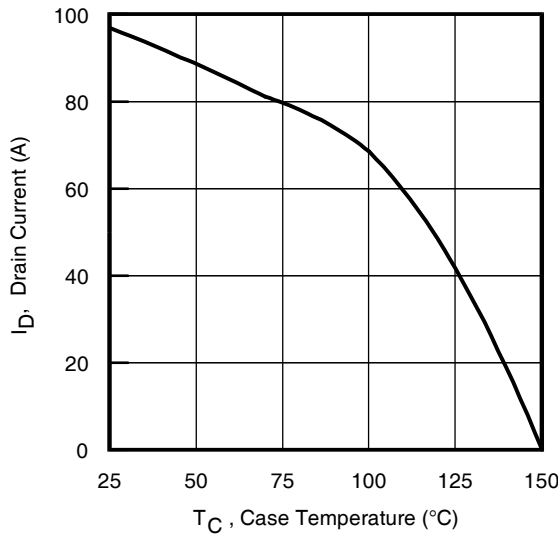


Fig 9. Maximum Drain Current vs. Case Temperature

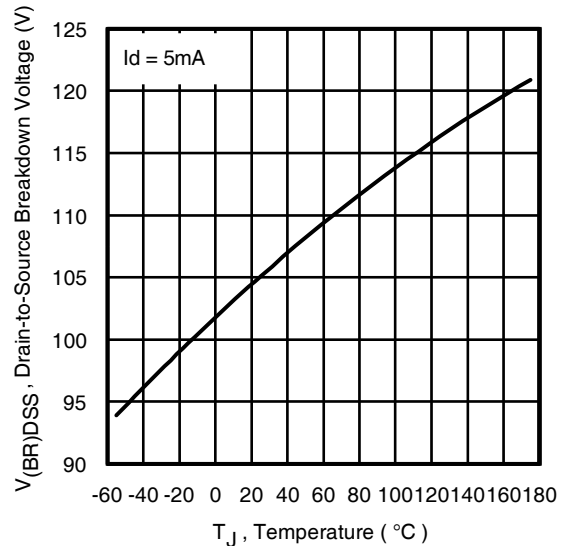


Fig 10. Drain-to-Source Breakdown Voltage

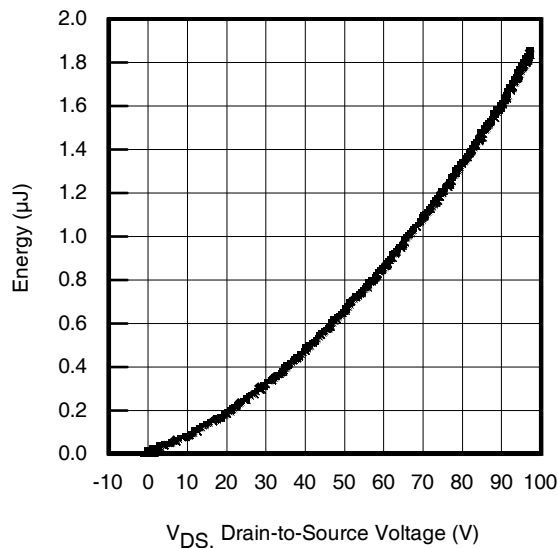


Fig 11. Typical C_{OSS} Stored Energy

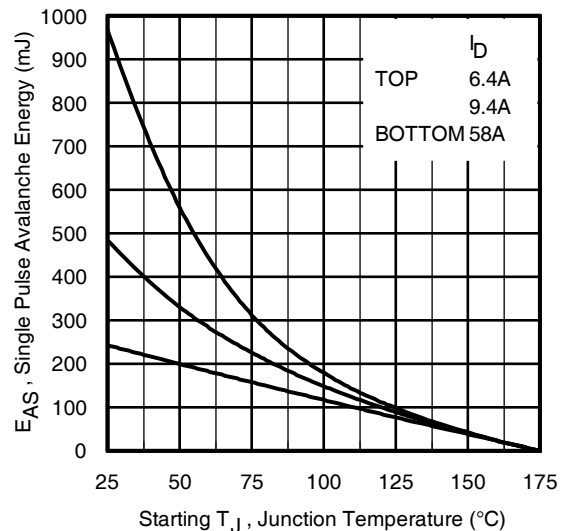


Fig 12. Maximum Avalanche Energy vs. Drain Current

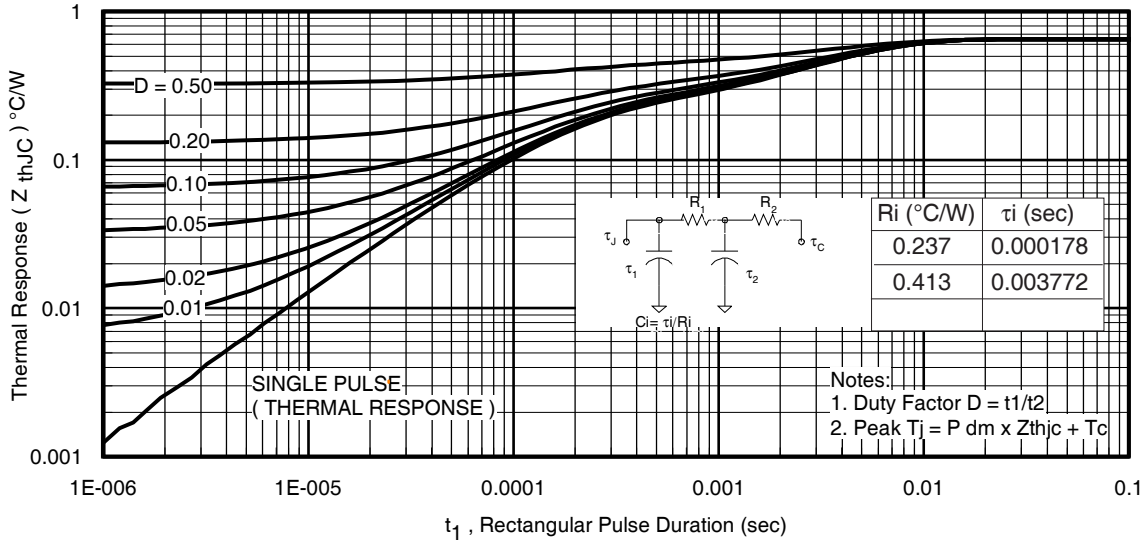


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

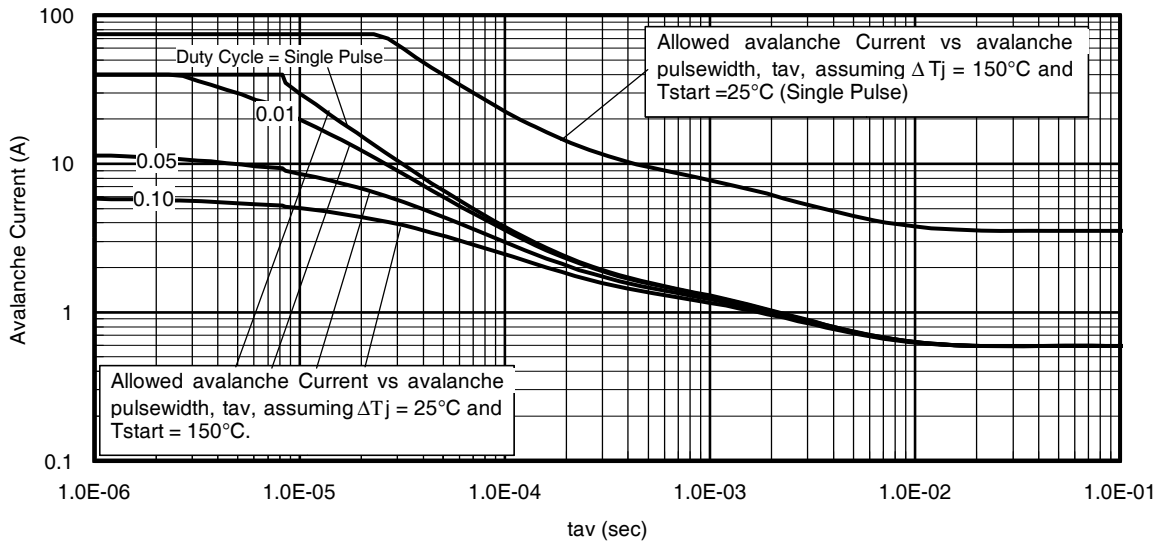


Fig 14. Typical Avalanche Current vs. Pulsewidth

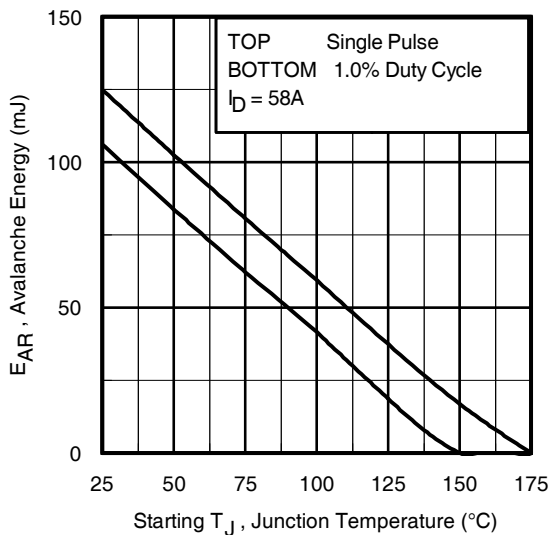


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

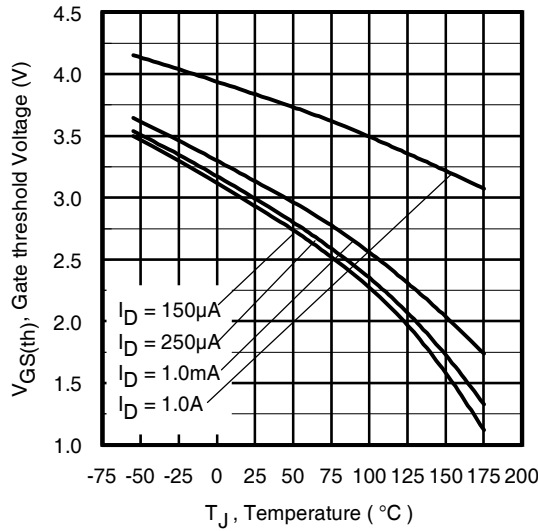


Fig. 16. Threshold Voltage vs. Temperature

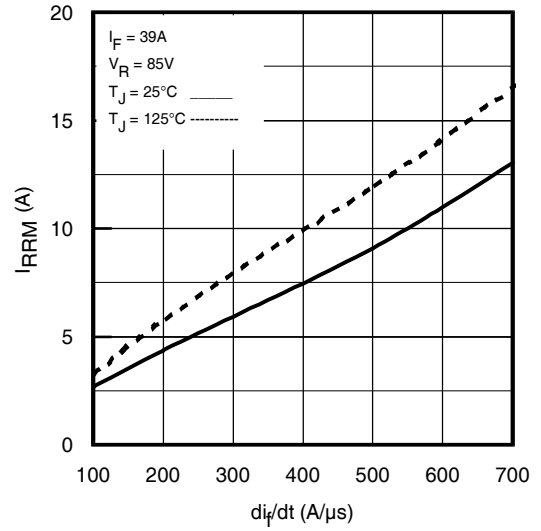


Fig. 17 - Typical Recovery Current vs. di_f/dt

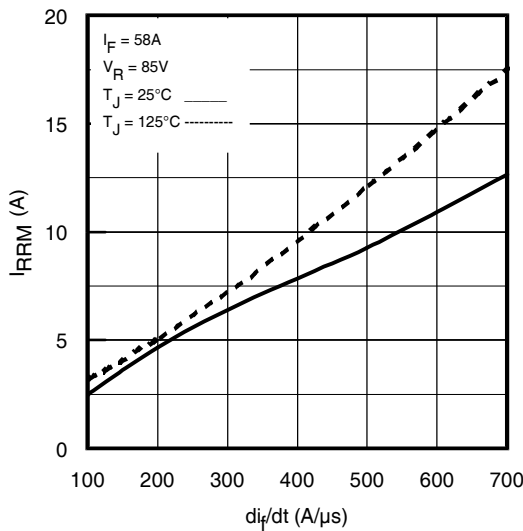


Fig. 18 - Typical Recovery Current vs. di_f/dt

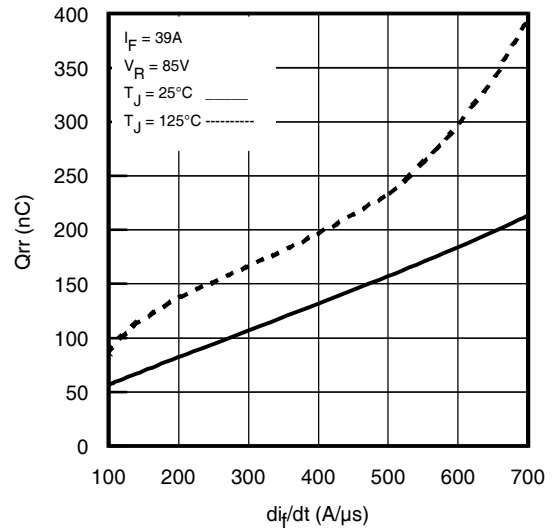


Fig. 19 - Typical Stored Charge vs. di_f/dt

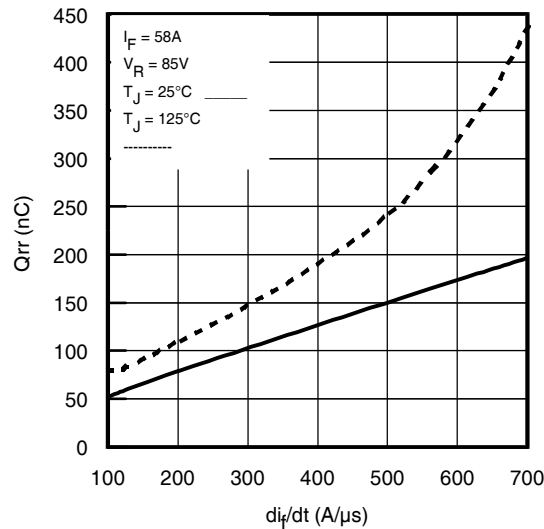


Fig. 20 - Typical Stored Charge vs. di_f/dt

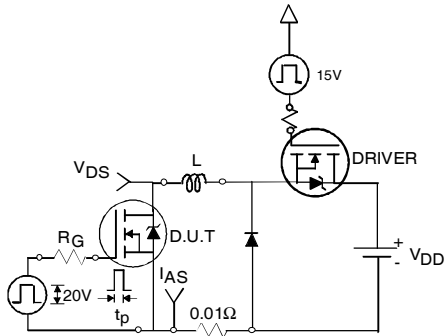


Fig 21a. Unclamped Inductive Test Circuit

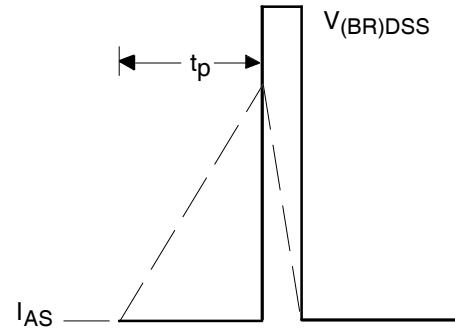


Fig 21b. Unclamped Inductive Waveforms

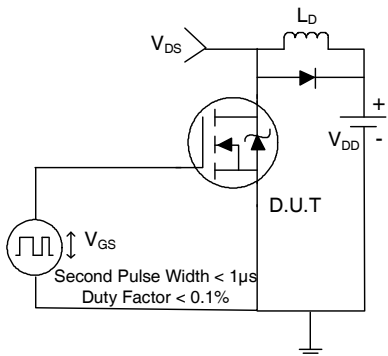


Fig 22a. Switching Time Test Circuit

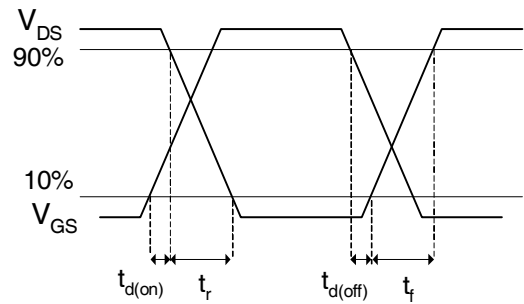


Fig 22b. Switching Time Waveforms

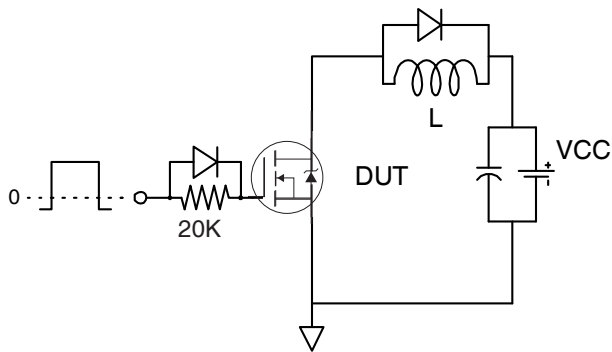


Fig 23a. Gate Charge Test Circuit

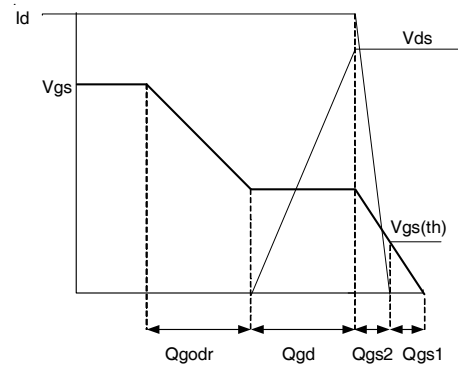
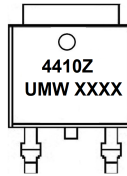


Fig 23b. Gate Charge Waveform

Package Mechanical Data

TO-263

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW IRFS4410Z	TO-263	800	Tape and reel

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[STF5N65M6](#) [IRF40H233XTMA1](#) [STU5N65M6](#) [DMN6022SSD-13](#) [DMN13M9UCA6-7](#) [DMTH10H4M6SPS-13](#) [IPS60R360PFD7SAKMA1](#)
[DMN2990UFB-7B](#) [SSM3K35CT,L3F](#) [IPLK60R1K0PFD7ATMA1](#) [2N7002W-G](#) [MCAC30N06Y-TP](#) [IPWS65R035CFD7AXKSA1](#)
[MCQ7328-TP](#) [SSM3J143TU,LXHF](#) [DMN12M3UCA6-7](#) [PJMF280N65E1_T0_00201](#) [PJMF380N65E1_T0_00201](#)
[PJMF280N60E1_T0_00201](#) [PJMF600N65E1_T0_00201](#) [PJMF900N65E1_T0_00201](#)