700V Half Bridge MOSFET/IGBT Gate Driver

Description

The UMW IRS2104STR is a high voltage, high speed power MOSFET drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 700 V.

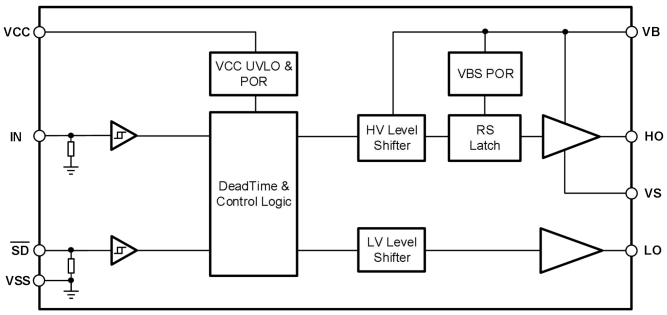
Application

- Motor Control
- Air Conditioners/ WasINg MacINes
- General Purpose Inverters
- Micro/Mini Inverter Drives

Features and Benefits

- Floating channel designed for bootstrap operation
- Fully operational to +700 V
- 3.3V, 5V and 15V input logic compatible
- Tolerant to negative transient voltage dV/dt immune
- Allowable negative Vs capability: -9V
- Gate drive supply range from 10V to 20V
- Shut down input turns off both channels
- Cross-conduction prevention
- Internal 540ns deadtime
- Matched propagation delay for both channels
- Typically output Source/Sink current capability: 300mA/600mA
- Wide operating temperature range -40°C ~125°C

Functional Block Diagram



Function Pin Description

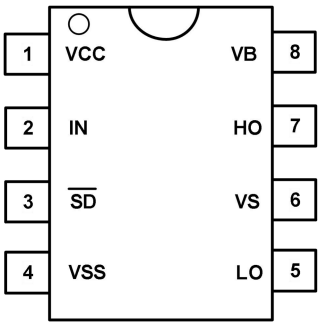


Figure7-1 8-Pin SOIC8 Top view

Table7-1 Lead Definitions

Number	Symbol	Description
1	V_{CC}	Low side and logic fixed supply
2	IN	Logic input for high side and low side gate driver outputs, in phase with HO
3	SD	Logic input for shutdown
4	V_{SS}	Low side return
5	LO	Low side gate drive output
6	V_S	High side floating supply return
7	HO	High side gate drive output
8	V_B	High side floating supply

Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to VSS and an ambient temperature of 25°C.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	-0.3	725	V
V_S	High side floating supply return	V_B – 25	V_B + 0.3	
V_{HO}	High side gate drive output	V_S -0.3	V_B + 0.3	
V_{CC}	Low side and main power supply	-0.3	25	
V_{LO}	Low side gate drive output	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input of IN & $\overline{SD}$	-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns
ESD	HBM Model	1500	—	V
	CDM Model	500	—	V
P_D	Package Power Dissipation @ TA ≤25°C	—	625	mW
Rth_{JA}	Thermal Resistance, Junction to Ambient	--	200	°C/W
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of VS and VSS are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to VSS and the ambient temperature is 25°C.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	VS + 10	VS + 20	V
V_S	High side floating supply return	-9	700	
V_{HO}	High side gate drive output	V_S	V_B	
V_{CC}	Low side and main power supply	10	20	
V_{LO}	Low side gate drive output	0	V_{CC}	
V_{IN}	Logic input of IN & $\overline{SD}$	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note1：Transient negative VS can be used for VSS-50V with a pulse width of 50ns, guaranteed by design..

Note2：When the input pulse width is less than 1us, the input pulse cannot be transmitted normally .

Electrical Characteristics

Valid for temperature range at T_A= 25°C, V_{CC}=V_B= 15V, C_L=1nF, unless otherwise specified

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
t_{ON}	Turn-on propagation delay	—	130	200	ns	V_S=0V
t_{OFF}	Turn-off propagation delay	—	130	200	ns	V_S=700V
t_R	Turn-on rise time	—	75	130	ns	
t_F	Turn-off fall time	—	35	70	ns	
t_{OFF}	Shutdown propagation delay	—	130	200	ns	
DT	Deadtime	400	520	650	ns	
MT	Delay matching	—	—	50	ns	
MDT	Deadtime matching	—	—	60	ns	
V_{CCUV+}	VCC supply UVLO threshold	8	8.9	9.8	V	
V_{CCUV-}		7.4	8.2	9.0	V	
$V_{CCUVHYS}$	hysteresis of V_{CC} UVLO	—	0.7	—	V	
I_{LK}	High-side floating supply leakage current	—	—	50	μA	V_B=V_S=700V
I_{QBS}	Quiescent VB supply current	—	50	100	μA	V_{IN}=0V or 5V
I_{QCC}	Quiescent VCC supply current	—	120	240	μA	V_{IN}=0V or 5V
V_{IH}	Logic “1”(IN&SD) input voltage	2.5	—	—	V	VCC=10Vto 20V
V_{IL}	Logic “0” (IN&SD) input voltage	—	—	0.8	V	VCC=10Vto 20V
V_{OH}	High level output voltage, VBIAS - VO	—	—	0.1	V	$I_{O=}$0A
V_{OL}	Low level output voltage, VO	—	—	0.1	V	$I_{O=}$0A
I_{IN+}	Logic “1” Input bias current	—	5	10	μA	IN=5V, SD=5V
I_{IN-}	Logic “0” Input bias current	—	—	2	μA	IN=0V, SD=0V
I_{O+}	Output high short circuit pulsed current	200	300	—	mA	V_O=0V PW≤10us
I_{O-}	Output low short circuit pulsed current	400	600	—	mA	V_O=15V P

Function Description

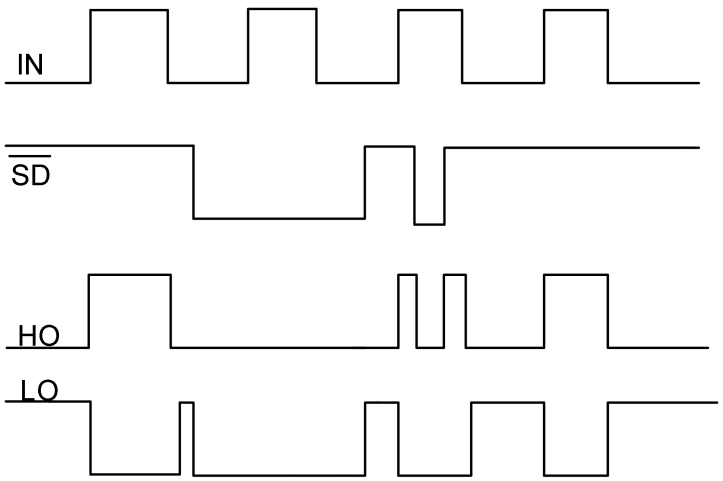


Figure 9-1 IRS2104STR Input and output timing waveform

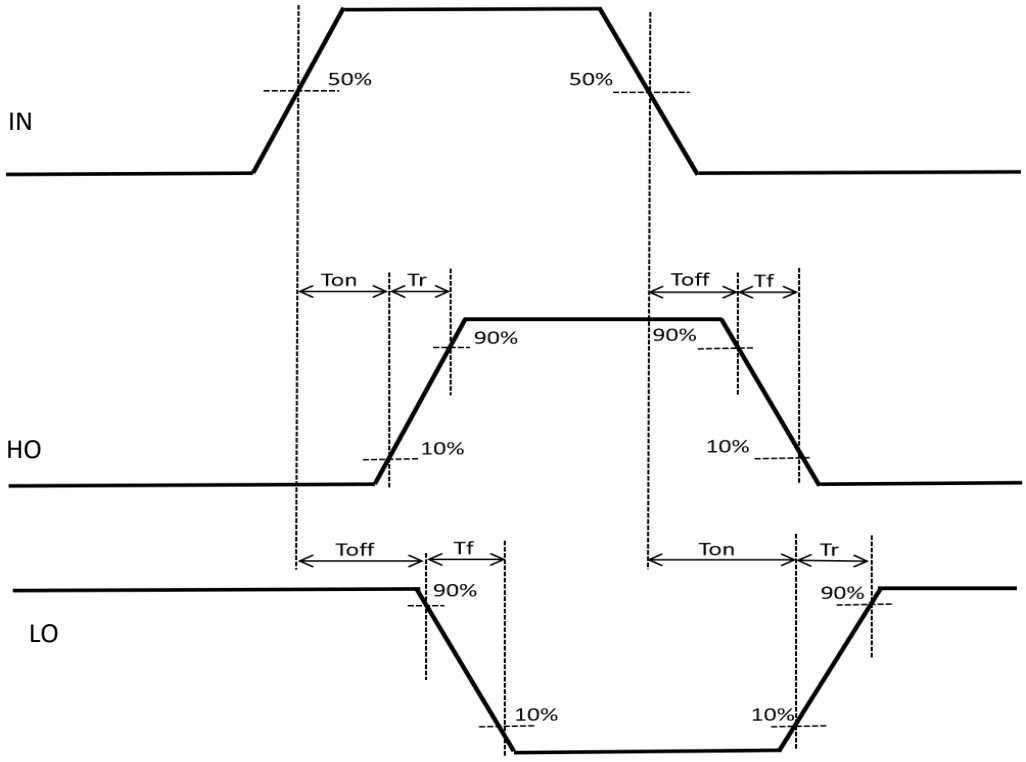


Figure 9-2 Propagation Time Waveform Definition

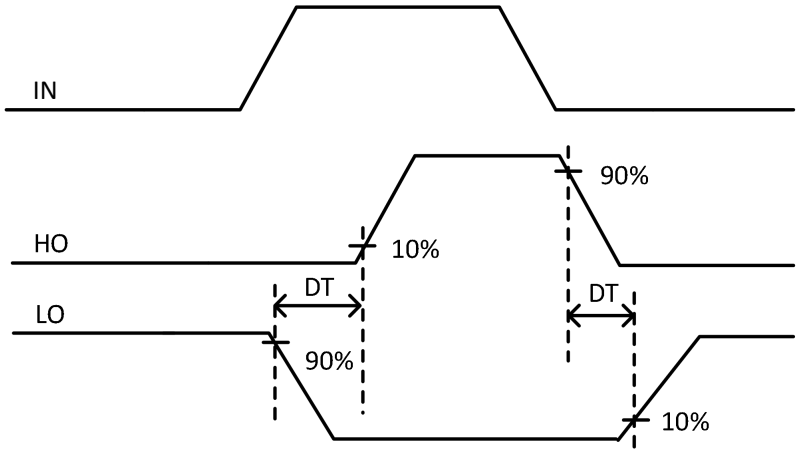


Figure7. Cross Conduction Prevention Delay Time Waveform Definition

Function Block Diagram

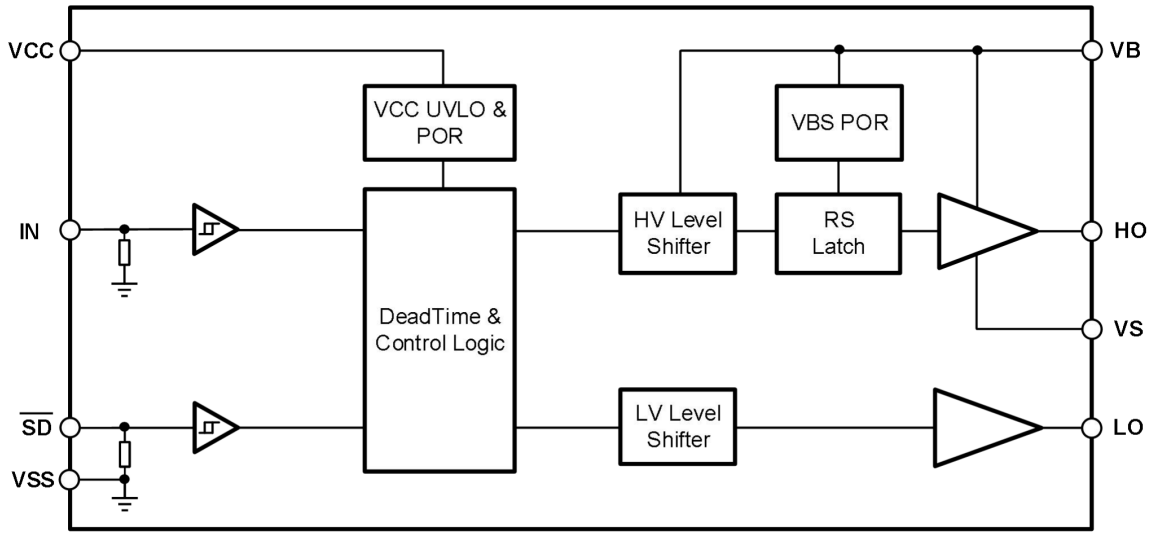


Figure10-1 Function Block Diagram of IRS2104STR

Application message

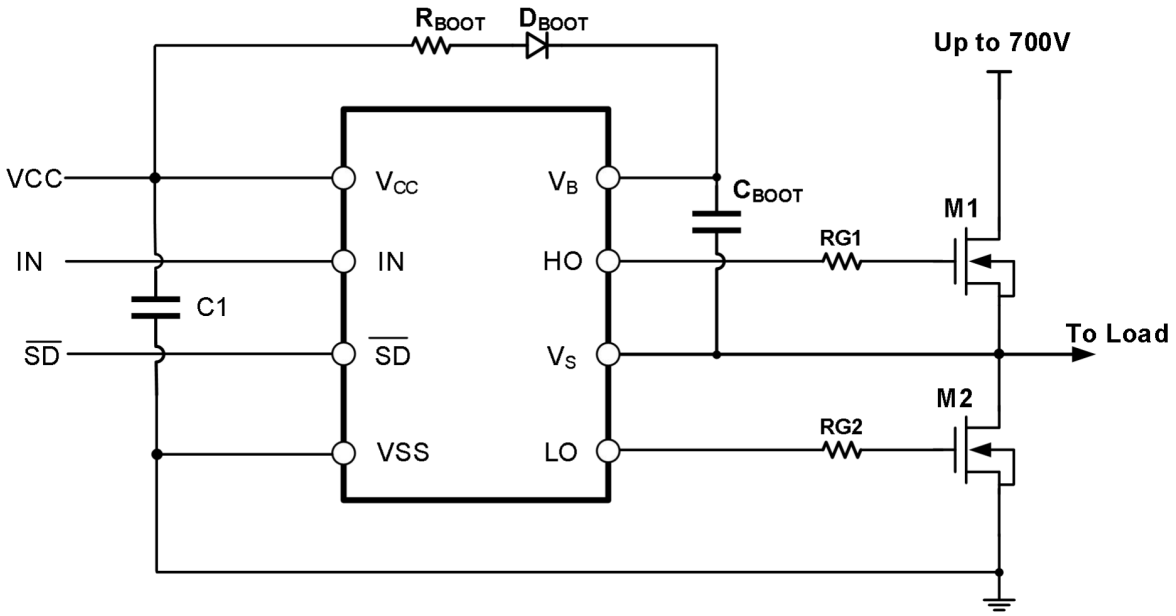
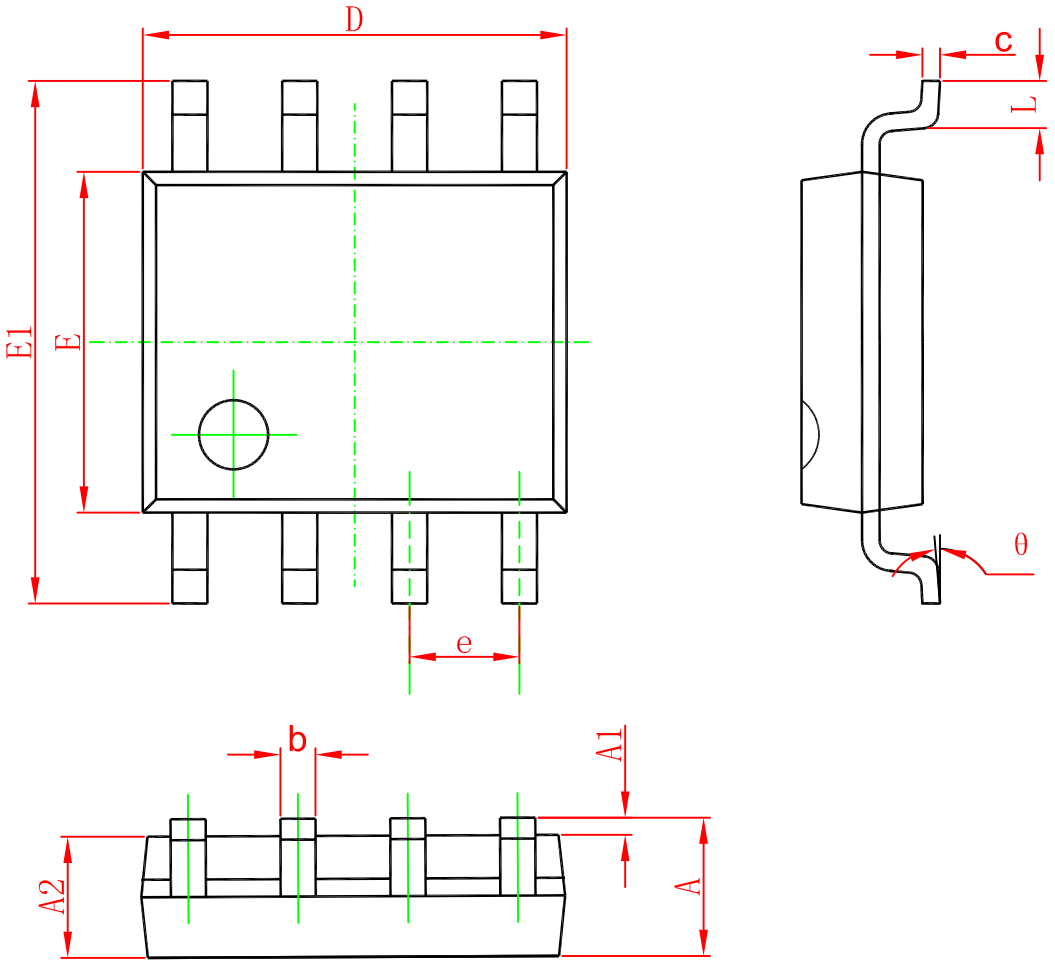


Figure10-2 Typical application circuit of IRS2104STR

PACKAGING INFORMATION

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Marking

Ordering information

Order code	Package	Baseqty	Deliverymode
UMW IRS2104STR	SOP-8	2500	Tape and reel

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