

### Description

The IRS21814STR is a high voltage, high speed power MOSFET drivers with dependent high and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 700 V.

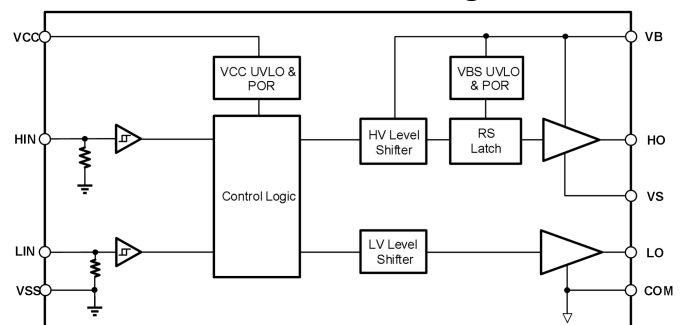
### Features and Benefits

- Floating channel designed for bootstrap operation
- Fully operational to +700 V
- 3.3V, 5V and 15V input logic compatible
- dV/dt noise Immunity  $\pm 50$  V/nsec
- Allowable negative Vs capability: -9V
- Gate drive supply range from 10V to 20V
- Undervoltage lockout for both channels
  - UVLO forward 8.9V
  - UVLO reverse 8.2V
- Turn-on/Turn-off propagation delay -
  - Ton/Toff =130ns/130ns
- Matched propagation delay for both channels
- Typically output Source/Sink current capability: 4A/4A

### Application

- Motor Control
- Air Conditioners/ Washing Machines
- General Purpose Inverters
- Micro/Mini Inverter Drives

### Functional Block Diagram



Function Pin Description

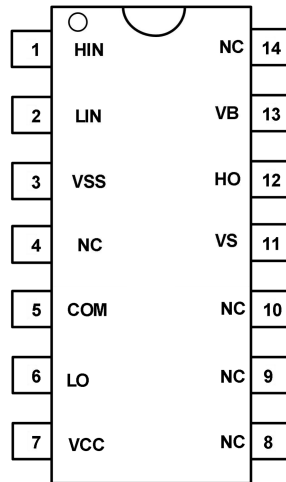


Figure7-1 14-Pin SOIC14 Top view

Table7-1 Lead Definitions

Number	Symbol	Description
1	HIN	Logic input for high side gate driver output (HO), in phase
2	LIN	Logic input for low side gate driver output (LO), in phase
3	VSS	Logic ground
4	NC	No connect
5	COM	Low side return
6	LO	Low side gate drive output
7	VCC	Low side and logic fixed supply
8	NC	No connect
9	NC	No connect
11	VS	High side floating supply return
12	HO	High side gate drive output
13	VB	High side floating supply
14	NC	No connect

### Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to COM and an ambient temperature of 25°C.

Symbol	Definition	MIN.	MAX.	Units
V <sub>B</sub>	High side floating supply	-0.3	725	V
V <sub>S</sub>	High side floating supply return	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3	
V <sub>HO</sub>	High side gate drive output	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3	
V <sub>CC</sub>	Low side and main power supply	-0.3	25	
V <sub>LO</sub>	Low side gate drive output	-0.3	V <sub>CC</sub> + 0.3	
V <sub>IN</sub>	Logic input (HIN, LIN)	V <sub>SS</sub> -0.3	V <sub>SS</sub> +5	
V <sub>SS</sub>	Logic ground	V <sub>CC</sub> -25	V <sub>CC</sub> +0.3	
dV <sub>S</sub> /dt	dV/dt noise Immunity		50	V/ns
ESD	HBM Model	1.5		kV
	Machine Model	500		V
P <sub>D</sub>	Package Power Dissipation @ TA ≤25°C		0.625	W
R <sub>thJA</sub>	Thermal Resistance, Junction to Ambient		200	°C /W
T <sub>J</sub>	Junction Temperature		150	°C
T <sub>S</sub>	Storage Temperature	-55	150	
T <sub>L</sub>	Lead Temperature (Soldering, 10 seconds)		300	

### Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of VS and COM are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to COM and the ambient temperature is 25°C.

Symbol	Definition	MIN.	MAX.	Units
V <sub>B</sub>	High side floating supply	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
V <sub>S</sub>	High side floating supply return	-9	700	
V <sub>HO</sub>	High side gate drive output	V <sub>S</sub>	V <sub>B</sub>	
V <sub>CC</sub>	Low side and main power supply	10	20	
V <sub>LO</sub>	Low side gate drive output	0	V <sub>CC</sub>	
V <sub>IN</sub>	Logic input of HIN & LIN	0	V <sub>CC</sub>	
V <sub>SS</sub>	Logic ground	-5	5	
T <sub>A</sub>	Ambient temperature	-40	125	°C

**Electrical Characteristics**

 Valid for temperature range at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = V_B = 15\text{V}$ ,  $C_L = 1\text{nF}$ , unless otherwise specified

Symbol	Definition	MIN	TYP	MAX	Units	Test Condition	
$t_{ON}$	Turn-on propagation delay		130	220	ns	$V_S = 0$	
$t_{OFF}$	Turn-off propagation delay		130	220		$V_S = 0\text{V}$ or $700\text{V}$	
$t_{sd}$	Shut-down propagation delay		130	220			
$t_R$	Turn-on rise time		40	60		$V_S = 0\text{V}$	
$t_F$	Turn-off fall time		20	35			
MT	Matched propagation time delay			50			
$V_{CCUV+}$	VCC supply UVLO threshold	8	8.9	9.8	V		
$V_{CCUV-}$		7.4	8.2	9.0			
$V_{CCUVHYS}$	hysteresis of $V_{CC}$ UVLO	—	0.7	—			
$V_{BSUV+}$	VBS supply UVLO threshold	8	8.9	9.8			
$V_{BSUV-}$		7.4	8.2	9.0			
$V_{BSUVHYS}$	hysteresis of $V_{BS}$ UVLO	—	0.7	—			
$I_{LK}$	High-side floating supply leakage current	—	—	50	$\mu\text{A}$	$V_B = V_S = 700\text{V}$	
$I_{QBS}$	Quiescent VB supply current	—	50	100		$V_{IN} = 0\text{V}$ or $5\text{V}$	
$I_{QCC}$	Quiescent VCC supply current	—	150	240			
$V_{IH}$	Logic "1" input voltage	2.5	—	—	V	$V_{CC} = 10\sim 20\text{V}$	
$V_{IL}$	Logic "0" input voltage	—	—	0.8			
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	—	—	1.4			$I_O = 0\text{A}$
$V_{OL}$	Low level output voltage, $V_O$	—	—	0.1			$I_O = 20\text{mA}$
$I_{IN+}$	Logic "1" Input bias current	—	25	60	$\mu\text{A}$	$V_O = 0\text{V}$ , $L_{IN} = 5\text{V}$ ,	
$I_{IN-}$	Logic "0" Input bias current	—	—	2		$L_{IN} = 0\text{V}$ ,	
$I_{O+}$	Output high short circuit pulsed current	3.0	4.0	—	A	$V_O = 0\text{V}$ $PW \leq 10\mu\text{s}$	
$I_{O-}$	Output low short circuit pulsed current	3.0	4.0	—		$V_O = 15\text{V}$ P	

Function Description

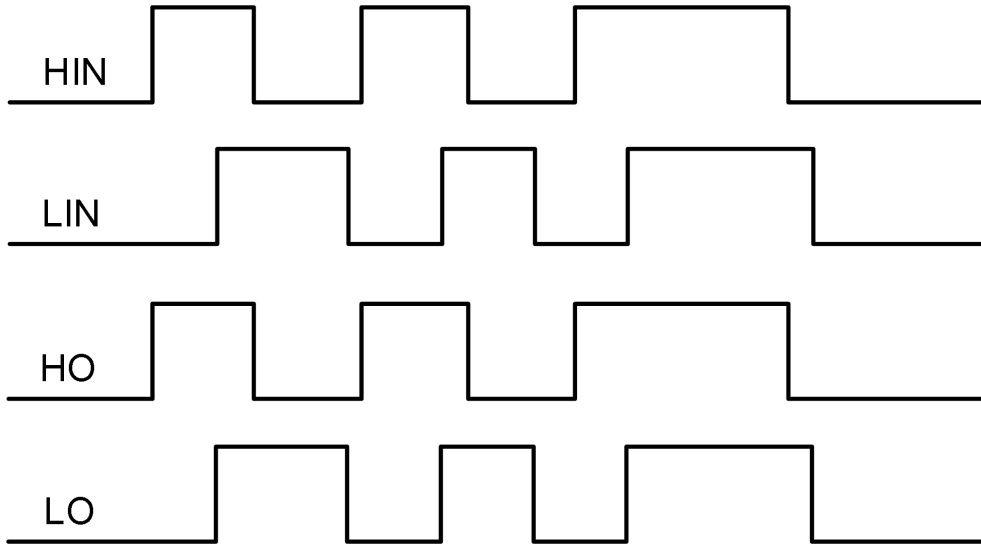


Figure 1. IRS21814STR Input and output timing waveform

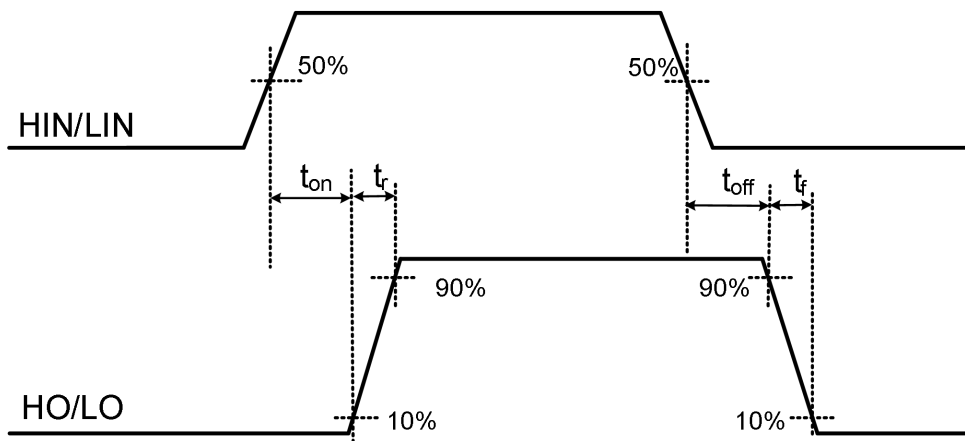


Figure 2. Propagation Time Waveform Definition

Waveform of Parameter

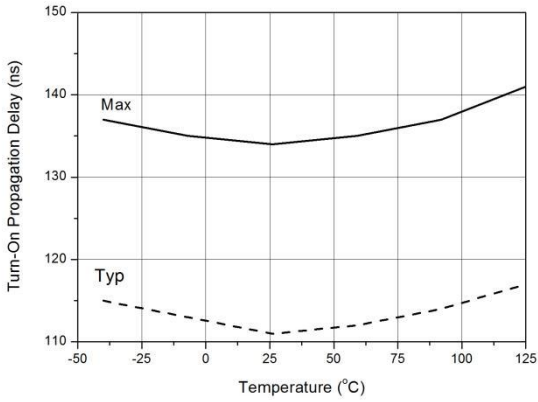


Figure 3A. Turn-On Propagation Delay vs. Temperature

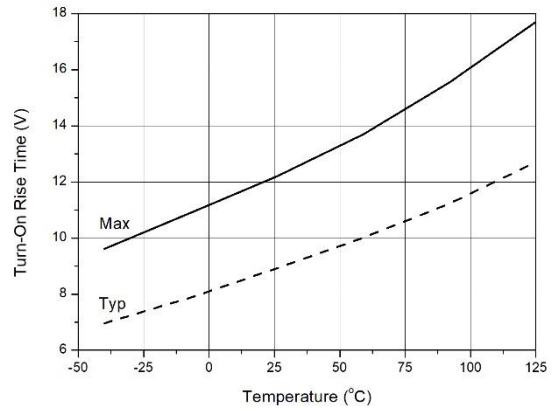


Figure 5A. Turn-On Rise Time vs. Temperature

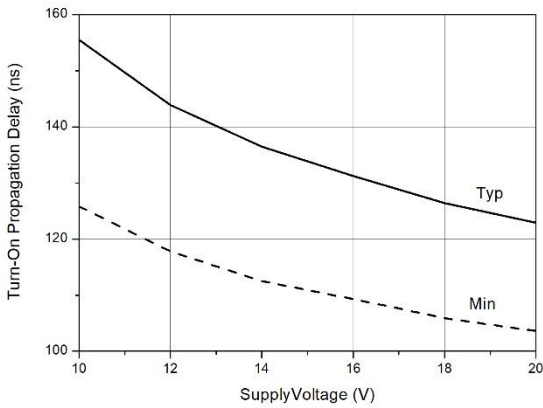


Figure 3B. Turn-on Propagation Delay vs. Supply Voltage

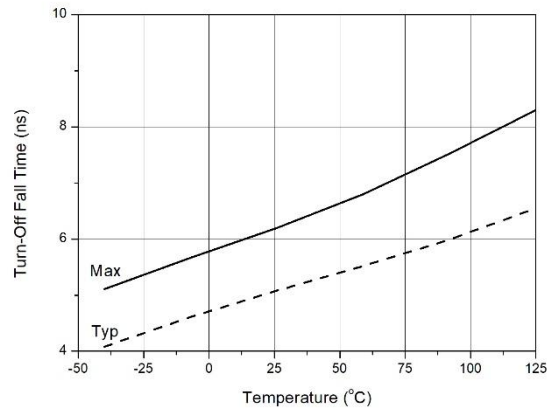


Figure 6A. Turn-Off Fall Time vs. Temperature

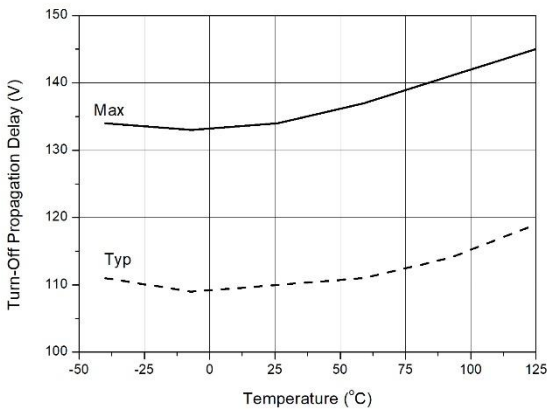


Figure 4A. Turn-Off Propagation Delay vs. Temperature

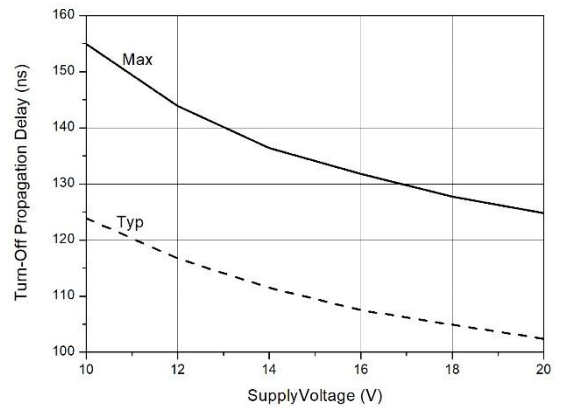


Figure 4B. Turn-off Propagation Delay vs. Supply Voltage

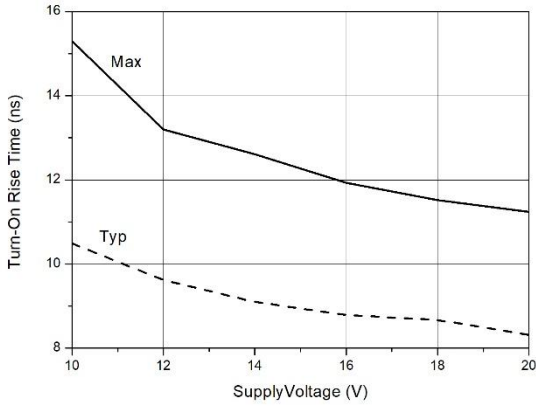


Figure 5B. Turn-On Rise Time vs. Supply Voltage

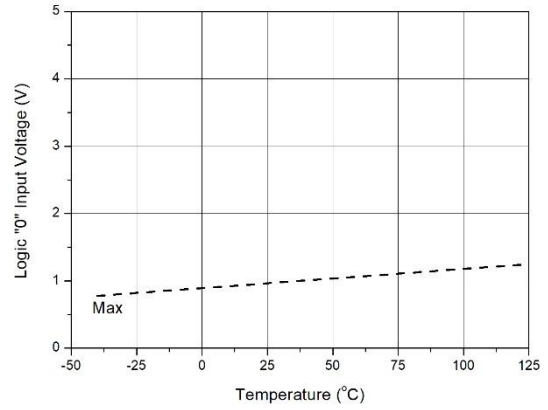


Figure 8A. Logic "0" Input Voltage vs. Temperature

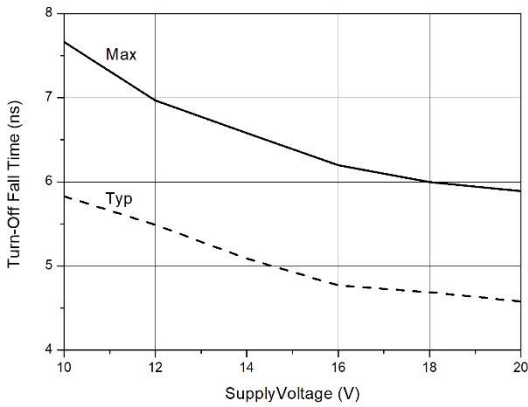


Figure 6B. Turn-Off Fall Time vs. Supply Voltage

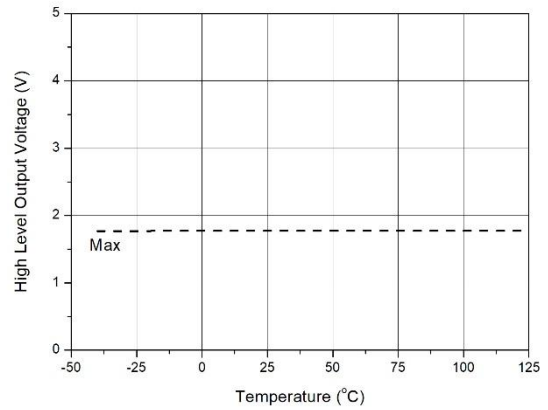


Figure 9A. High Level Output Voltage vs. Temperature (Io = 0mA)

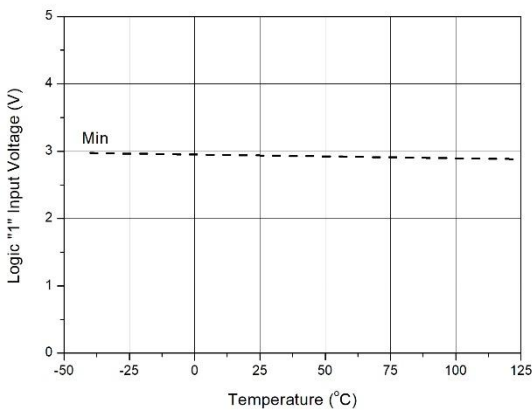


Figure 7A. Logic "1" Input Voltage vs. Temperature

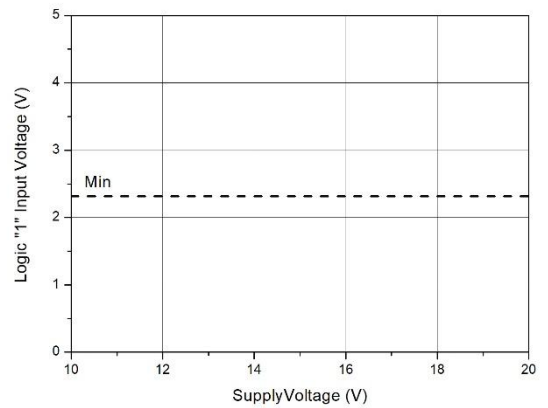


Figure 7B. Logic "1" Input Voltage vs. Supply Voltage

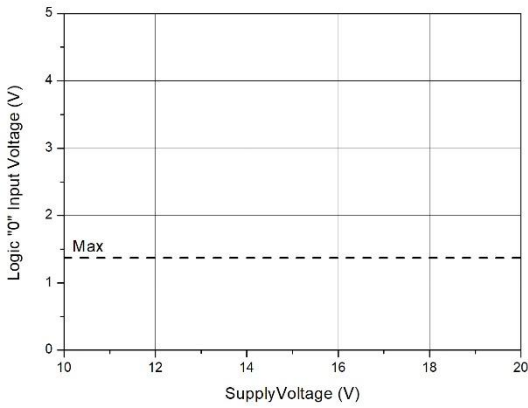


Figure 8B. Logic "0" Input Voltage vs. Supply Voltage

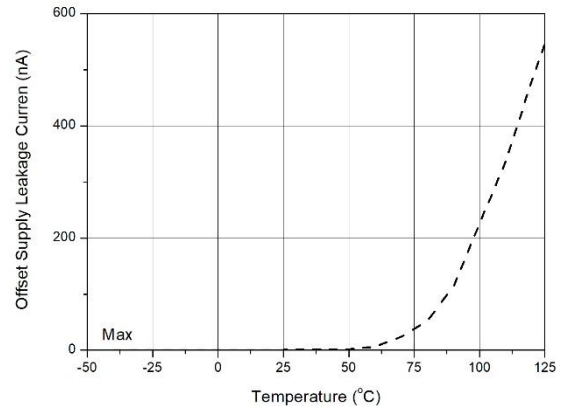


Figure 11A. Offset Supply Leakage Current vs. Temperature

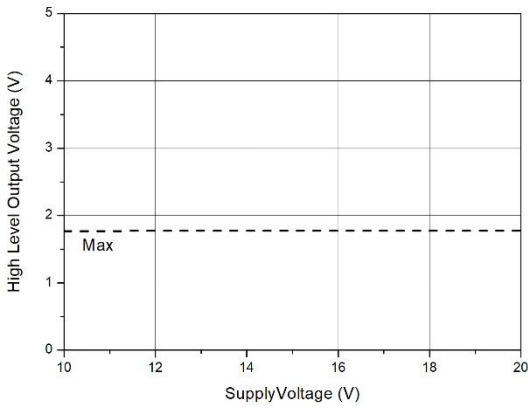


Figure 9B. High Level Output Voltage vs. Supply Voltage (Io = 0mA)

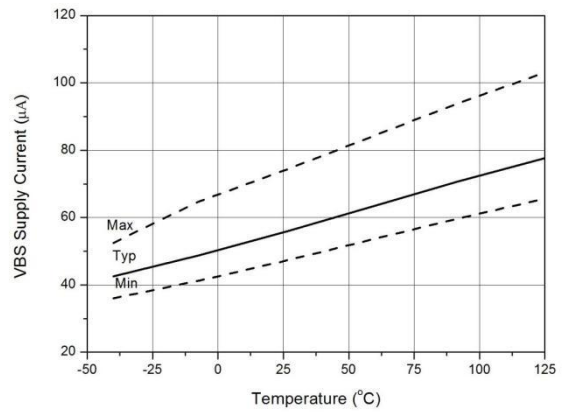


Figure 12A. VBS Supply Current vs. Temperature

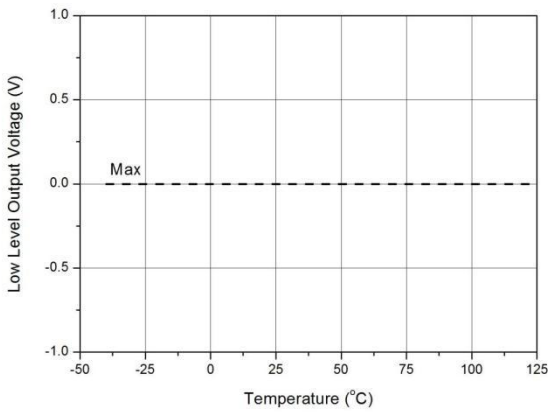


Figure 10A. Low Level Output vs. Temperature

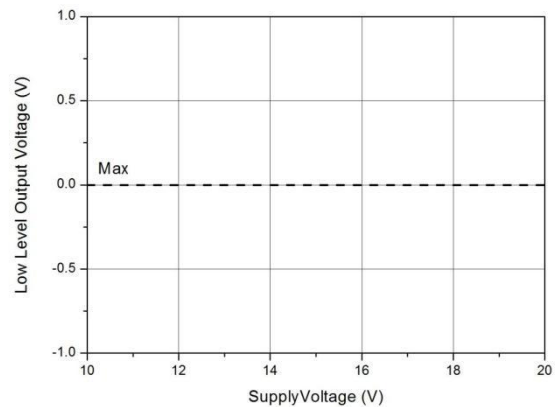


Figure 10B. Low Level Output vs. Supply Voltage



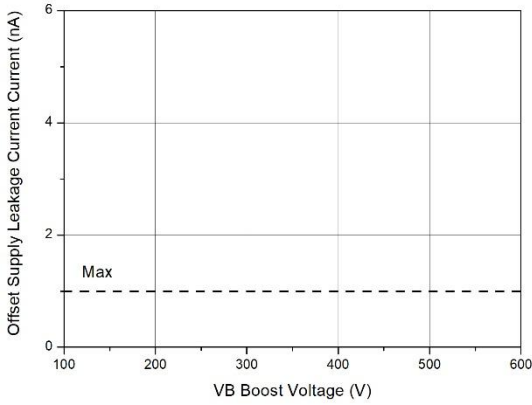


Figure 11B. Offset Supply Leakage Current vs. VB Boost Voltage

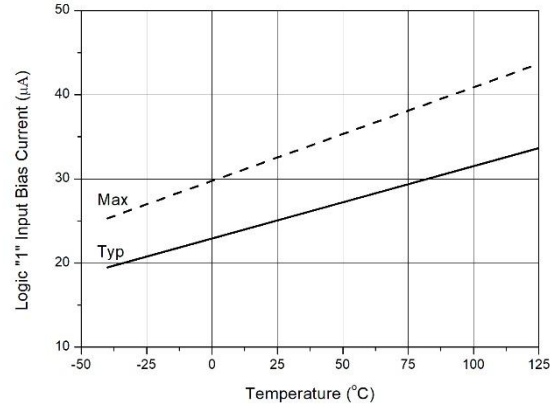


Figure 14A. Logic "1" Input Bias Current vs. Temperature

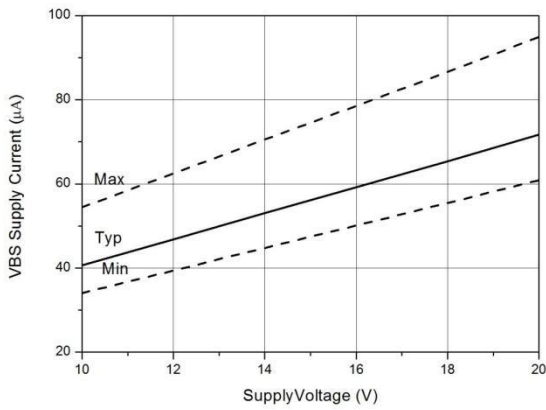


Figure 12B. VBS Supply Current vs. VBS Floating Supply Voltage

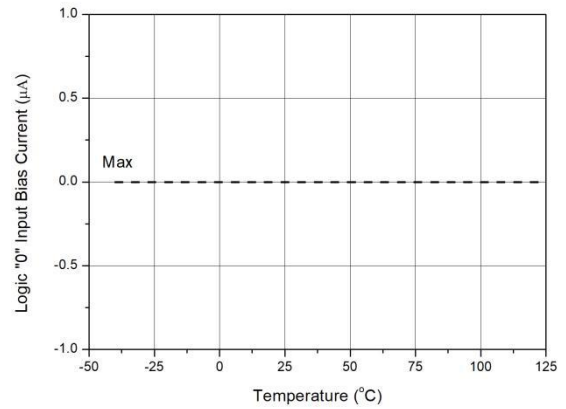


Figure 15A. Logic "0" Input Bias Current vs. Temperature

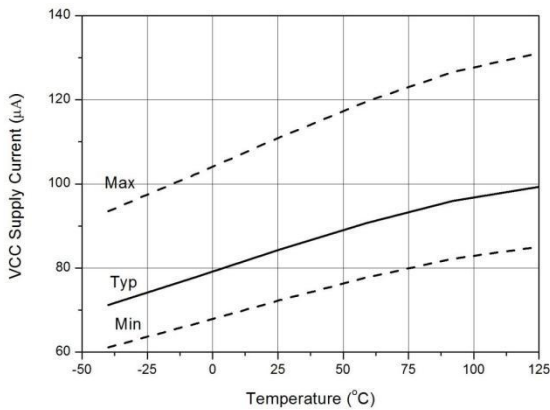


Figure 13A. VCC Supply Current vs. Temperature

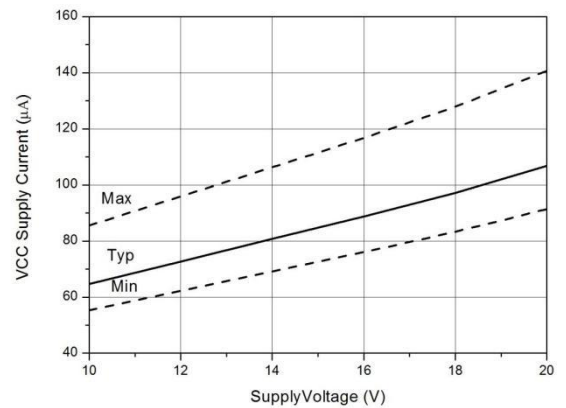


Figure 13B. VCC Supply Current vs. Supply Voltage

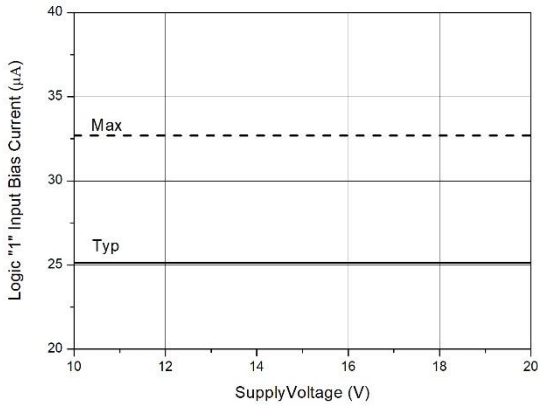


Figure 14B. Logic "1" Input Bias Current vs. Supply Voltage

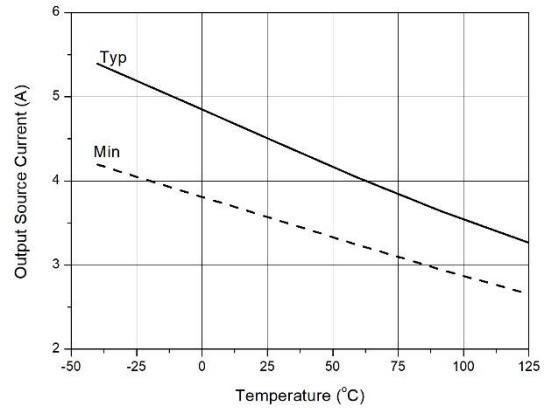


Figure 18A. Output Source Current vs. Temperature

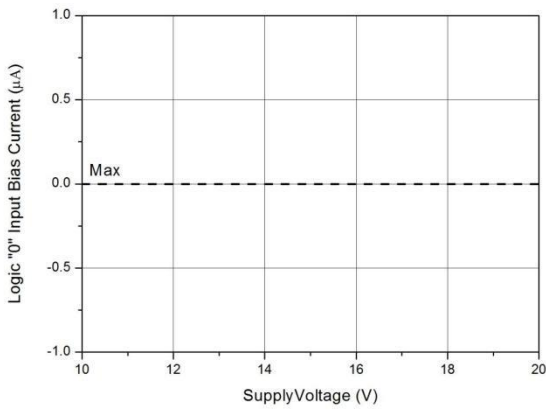


Figure 15B. Logic "0" Input Bias Current vs. Supply Voltage

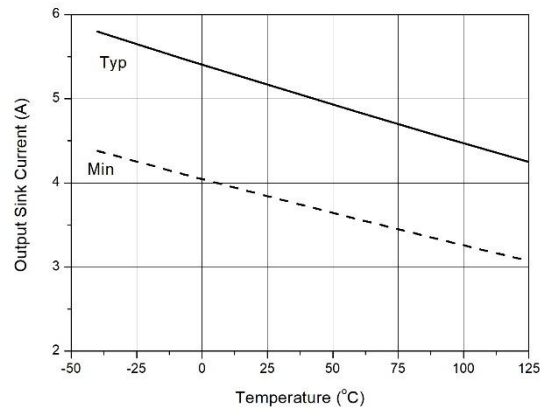


Figure 19A. Output Sink Current vs. Temperature

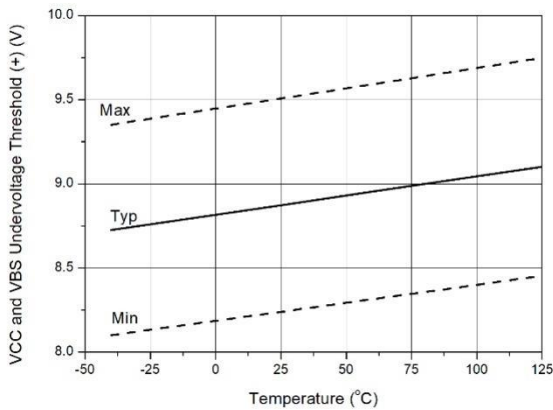


Figure 16. VCC and VBS Undervoltage Threshold (+) vs. Temperature

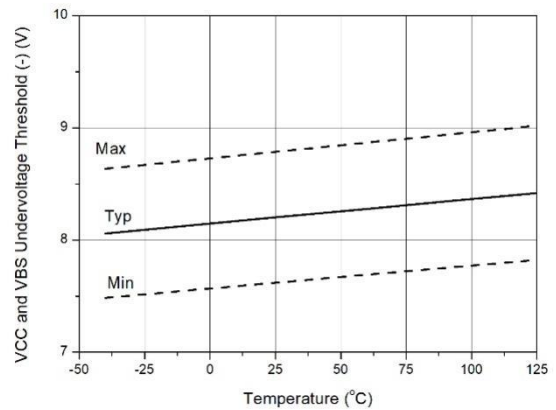


Figure 17. VCC and VBS Undervoltage Threshold (-) vs. Temperature

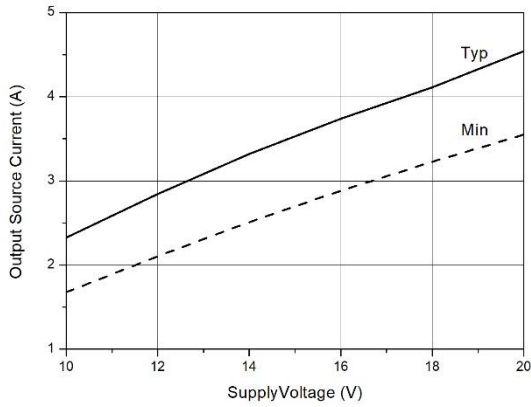


Figure 18B. Output Source Current vs. Supply Voltage

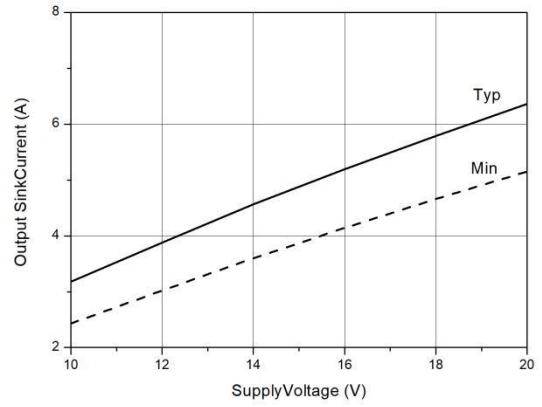


Figure 19B. Output Sink Current vs. Supply Voltage

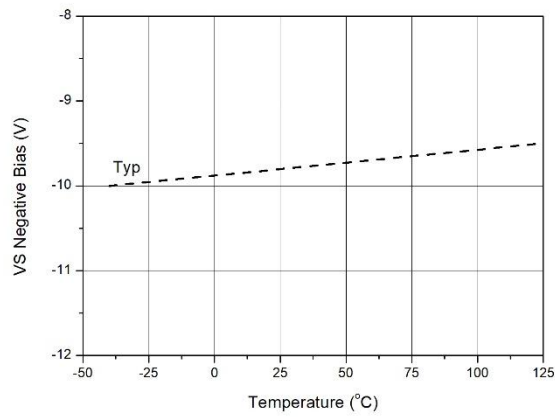


Figure 20. VS Negative Bias vs. Temperature

Function Block Diagram

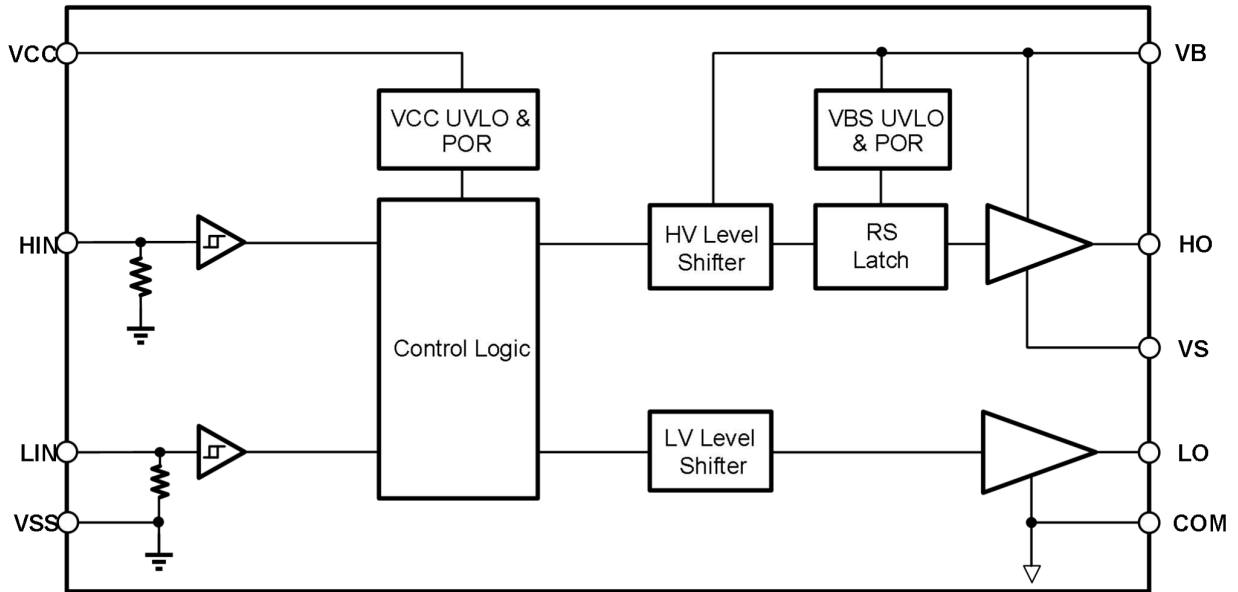


Figure 21. Function Block Diagram of IRS21814STR

Application message

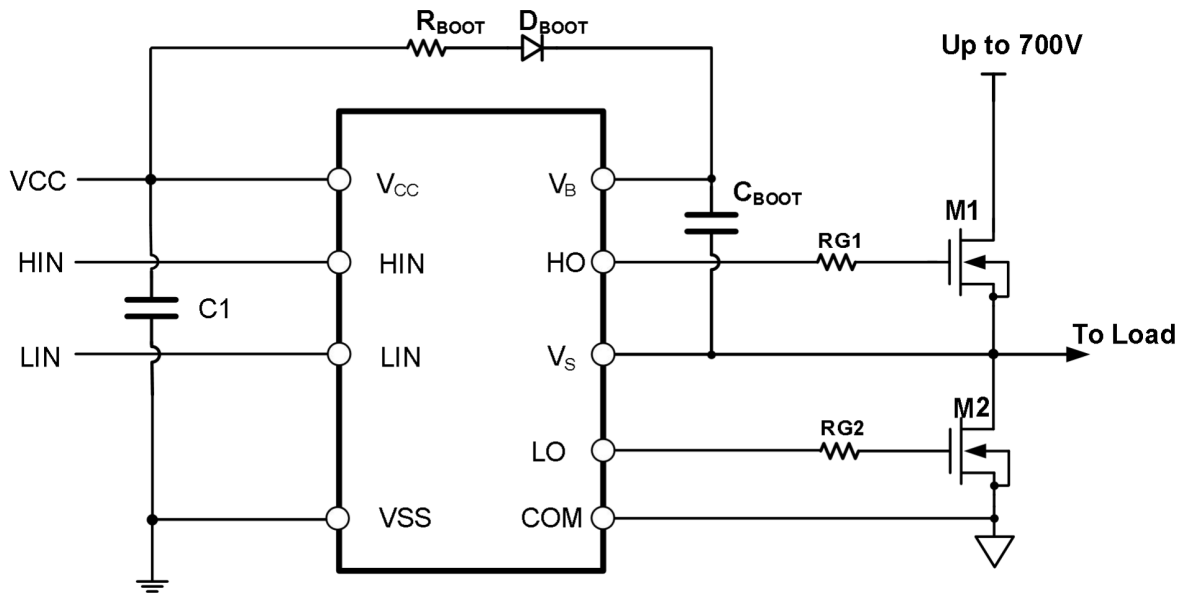
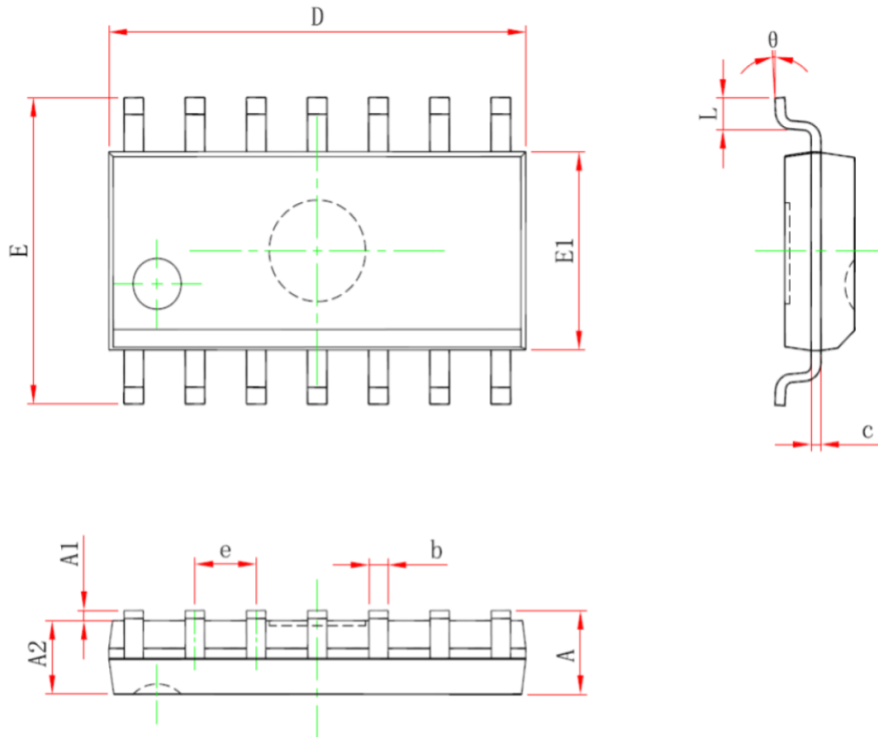


Figure 22. Typical application circuit of IRS21814STR

SOP-14



**Marking**



**Ordering information**

Order code	Package	Baseqty	Deliverymode
UMW IRS21814STR	SOP-14	2500	Tape and reel

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