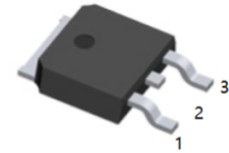


Features

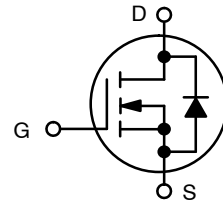
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses

Applications

- VCore Applications
- DC-DC Converters
- High/Low Side Switching
- $V_{DS}(V) = 25V$
- $I_D = 65A$ ($V_{GS} = 10V$)
- $R_{DS(ON)} < 7.5m\Omega$ ($V_{GS} = 10V$)
- $R_{DS(ON)} < 11.1m\Omega$ ($V_{GS} = 4.5V$)



1.G 2.D 3.S
TO-252(DPAK) top view



MAXIMUM RATINGS ($T_J = 25^\circ C$ unless otherwise stated)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	25	V
Gate-to-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	$T_A = 25^\circ C$	13	A
		$T_A = 85^\circ C$	10	
Power Dissipation $R_{\theta JA}$ (Note 1)	Steady State	$T_A = 25^\circ C$	2.0	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)		$T_A = 25^\circ C$	10.4	A
Power Dissipation $R_{\theta JA}$ (Note 2)	Steady State	$T_A = 85^\circ C$	8.0	
		$T_A = 25^\circ C$	1.28	W
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ C$	65	A
		$T_C = 85^\circ C$	50	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ C$	50	W
Pulsed Drain Current		$t_p = 10\mu s$	$T_A = 25^\circ C$	130
Current Limited by Package	Steady State	$T_A = 25^\circ C$	45	A
Operating Junction and Storage Temperature		T_J, T_{STG}	-55 to +175	$^\circ C$
Source Current (Body Diode)		I_S	42	A
Drain to Source dV/dt		dV/dt	6	V/ns
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ C, V_{DD} = 50 V, V_{GS} = 10 V, I_L = 13 A_{pk}, L = 1.0 mH, R_G = 25 \Omega$)		EAS	84.5	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ C$

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	3	°C/W
Junction-to-TAB (Drain)	$R_{\theta JC-TAB}$	3.5	
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	75	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	117	

1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	25			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			21		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.45		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			5.2		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 30\text{ A}$	6.1	7.5	m Ω
		$V_{GS} = 4.5\text{ V}$	$I_D = 30\text{ A}$	8.9	11.1	
Forward Transconductance	g_{FS}	$V_{DS} = 1.5\text{ V}, I_D = 15\text{ A}$		48		S
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 12\text{ V}$		1308		pF
Output Capacitance	C_{OSS}			342		
Reverse Transfer Capacitance	C_{RSS}			169		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		11	16.5	nC
Threshold Gate Charge	$Q_{G(TH)}$			1.2		
Gate-to-Source Charge	Q_{GS}			3.9		
Gate-to-Drain Charge	Q_{GD}			4.7		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		21.8		nC
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		12.2		ns
Rise Time	t_r			20.1		
Turn-Off Delay Time	$t_{d(OFF)}$			15.2		
Fall Time	t_f			4.3		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
4. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified) (continued)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$			7.1		ns
Rise Time	t_r				17		
Turn-Off Delay Time	$t_{d(OFF)}$				22		
Fall Time	t_f				2.3		
Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 30\text{ A}$	$T_J = 25^\circ\text{C}$		0.9	1.2	V
			$T_J = 125^\circ\text{C}$		0.76		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 30\text{ A}$			12.7		ns
Charge Time	t_a				7.0		
Discharge Time	t_b				5.7		
Reverse Recovery Charge	Q_{RR}				3.5		
Source Inductance	L_S	$T_A = 25^\circ\text{C}$			2.49		nH
Drain Inductance, DPAK	L_D				0.0164		
Drain Inductance, IPAK	L_D				1.88		
Gate Inductance	L_G				3.46		
Gate Resistance	R_G				0.75		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

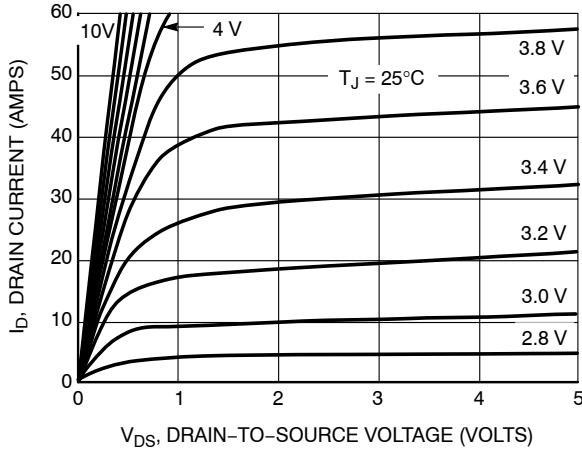


Figure 1. On-Region Characteristics

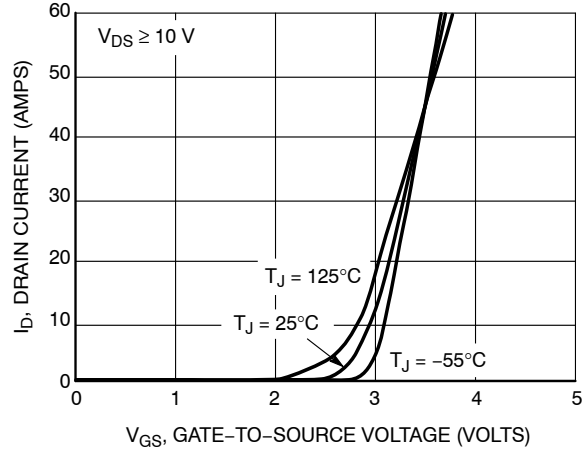


Figure 2. Transfer Characteristics

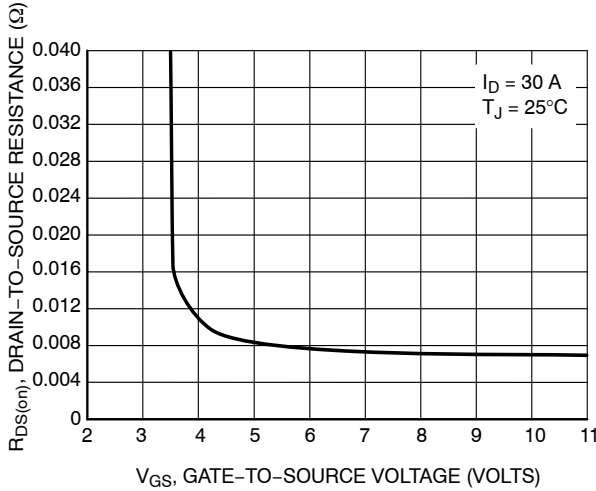


Figure 3. On-Resistance vs. Gate-to-Source Voltage

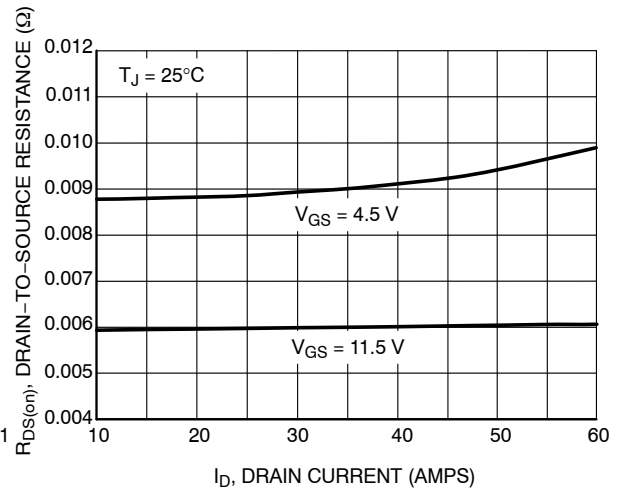


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

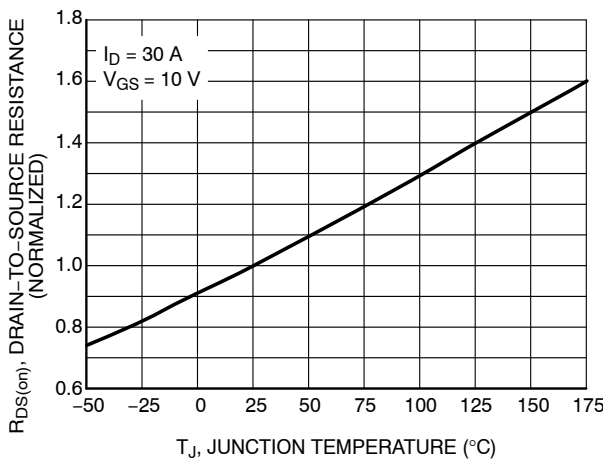


Figure 5. On-Resistance Variation with Temperature

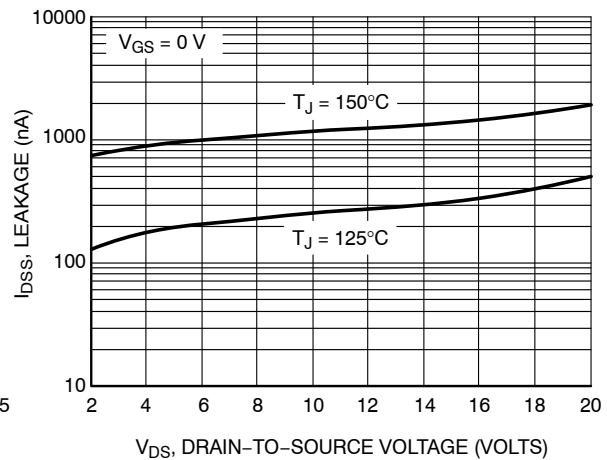


Figure 6. Drain-to-Source Leakage Current vs. Drain Voltage

TYPICAL PERFORMANCE CURVES

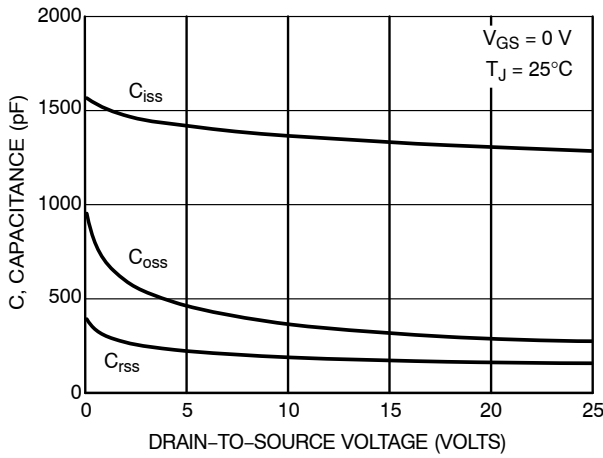


Figure 7. Capacitance Variation

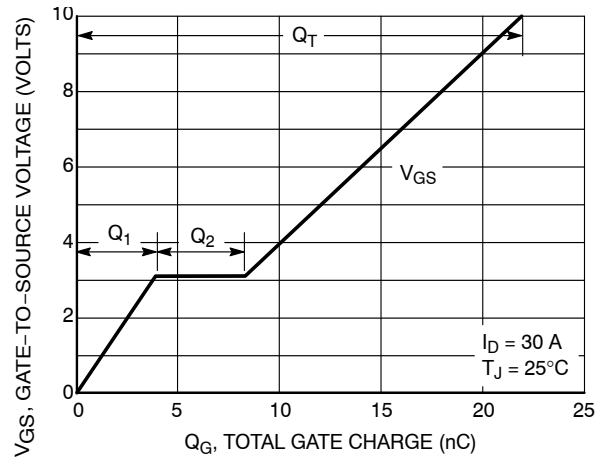


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

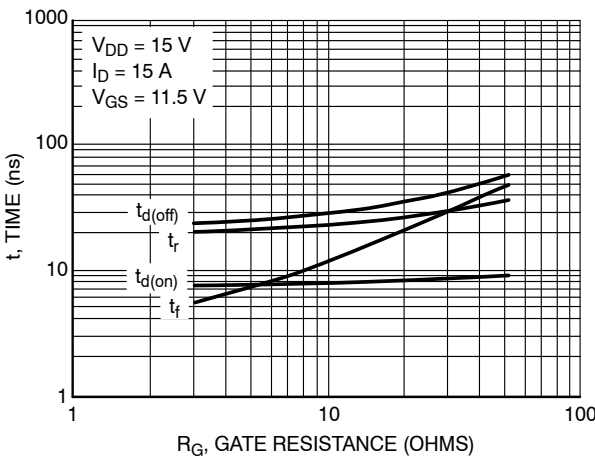


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

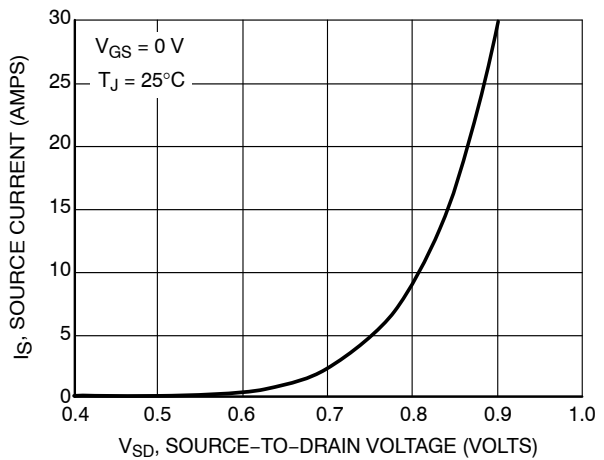


Figure 10. Diode Forward Voltage vs. Current

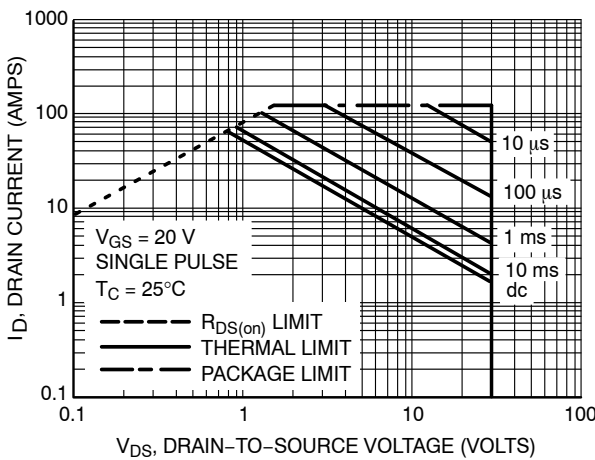


Figure 11. Maximum Rated Forward Biased Safe Operating Area

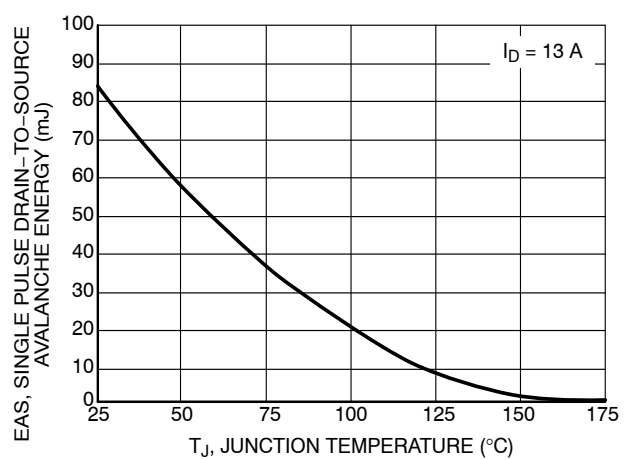


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL PERFORMANCE CURVES

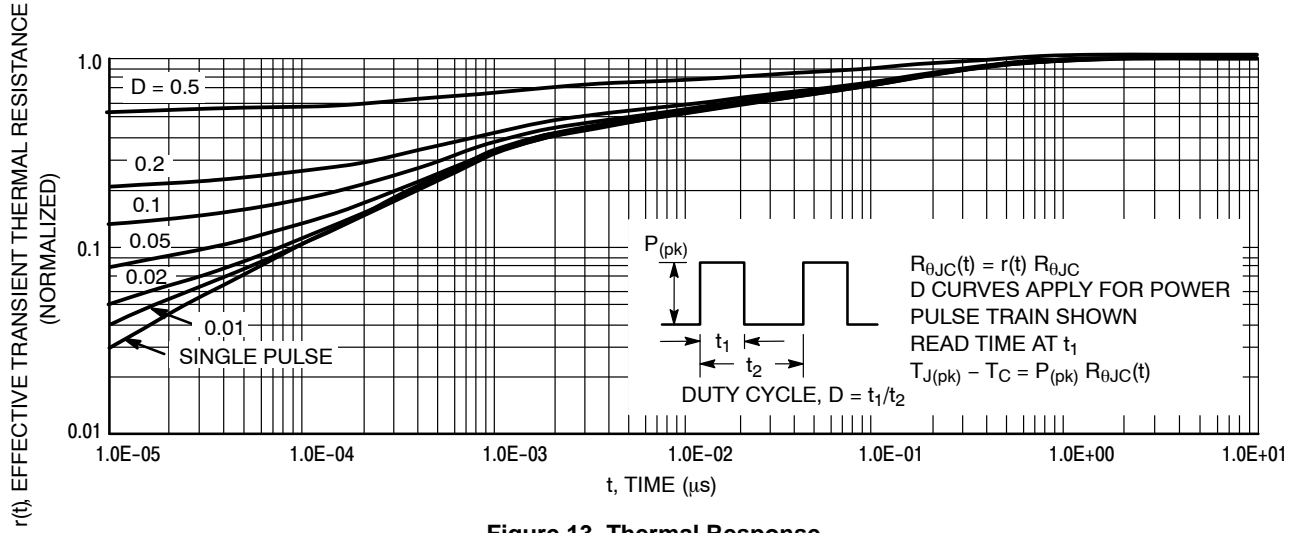
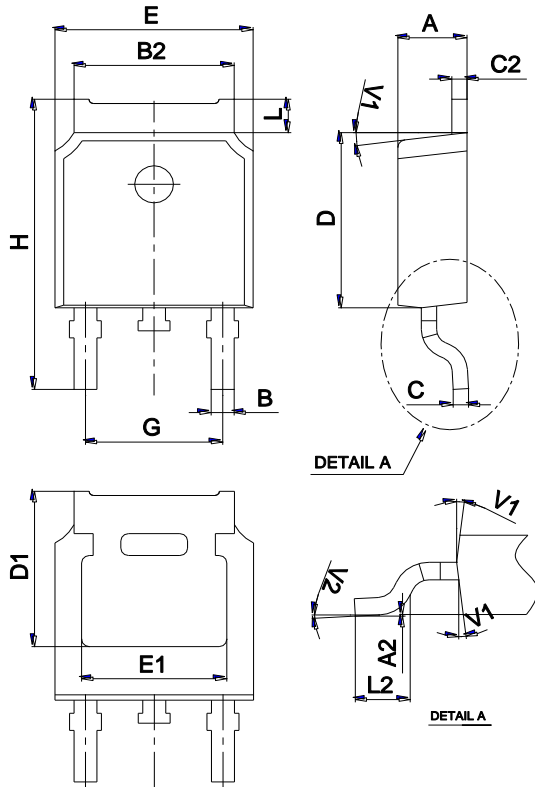


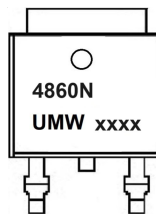
Figure 13. Thermal Response

Package Mechanical Data TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW NTD4860NT4G	TO-252	2500	Tape and reel

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[DMN2990UFB-7B](#) [SSM3K35CT,L3F](#) [IPLK60R1K0PFD7ATMA1](#) [2N7002W-G](#) [MCAC30N06Y-TP](#) [IPWS65R035CFD7AXKSA1](#)
[MCQ7328-TP](#) [SSM3J143TU,LXHF](#) [DMN12M3UCA6-7](#) [PJMF280N65E1_T0_00201](#) [PJMF380N65E1_T0_00201](#)
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