精密、零漂移、零交叉、真正的轨至轨输入/输出运算放大器

说明

OPA4388系列精密运算放大器是超低噪声、快速稳定、零漂移、零交叉 器件，可实现轨至轨输入和输出运行。这些特性及出色 的交流性能与仅为 0.25μV 的失调电压以及 0.005μV/°C 的温漂相结合，使得 OPA4388 成为驱 动 高精密模数转换器 (ADC) 或缓冲高分辨率数模转 换器 (DAC) 输出的理想选择。该设计在驱动模数转换 器 (ADC) 时具有出色的性能，而不会降低线性度。

应用

- 商用网络和服务器 PSU
- 笔记本电脑电源适配器设计
- 称重计
- 实验室和现场仪表
- 电池测试
- 电子温度计
- 温度变送器

特性

- 超低失调电压：±0.25μV
- 零漂移：±0.005μV/°C
- 零交叉：140dB CMRR 真正 RRIO
- 低噪声：7.0nV √Hz （1kHz 时）
- 无 1/f 噪声：140nV_{PP}（0.1Hz 至 10Hz）
- 快速稳定：2μs（1V，0.01%）
- 增益带宽：10MHz
- 单电源：2.5V 至 5.5V
- 双电源：±1.25V 至 ±2.75V
- 真正的轨至轨输入和输出
- EMI/RFI 滤波输入

Pin Configuration and Functions

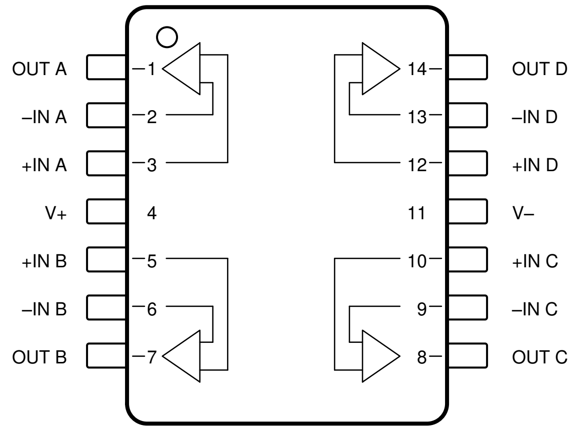


图 5-4. OPA4388 SOP-14 (D) and TSSOP-14 (PW) Packages, Top View

Pin Functions:OPA4388

NAME	OPA4388 (SOP-14) (TSSOP-14)	I/O	DESCRIPTION
- IN A	2	I	Inverting input, channel A
- IN B	6	I	Inverting input, channel B
- IN C	9	I	Inverting input, channel C
- IN D	13	I	Inverting input, channel D
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
+IN C	10	I	Noninverting input, channel C
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V -	11	—	Negative (lowest) power supply
V+	4	—	Positive (highest) power supply

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage	V_S = (V+) – (V–)	Single-supply		6	V
		Dual-supply		±3	
Signal input pins	Voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Current			±10	mA
Output short circuit(2)			Continuous	Continuous	
Temperature	Operating, T_A		–55	150	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Short-circuit to ground, one amplifier per package.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	Single-supply	2.5		5.5	V
	Dual-supply	±1.25		±2.75	
Specified temperature		–40		125	°C

Thermal Information: OPA4388

THERMAL METRIC(1)		OPA4388 (SOP) 14 PINS	OPA4388 (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86.4	109.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.3	27.4	°C/W
~~$R_{\theta JB}$~~	~~Junction-to-board thermal resistance~~	~~41.0~~	~~56.1~~	°C/W
~~Ψ_{JT}~~	~~Junction-to-top characterization parameter~~	~~11.3~~	~~1.5~~	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	40.7	54.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

Electrical Characteristics: VS = ±1.25 V to ±2.75 V (VS = 2.5 to 5.5 V)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	V_S = 5.5 V	OPA4388		±2.25	±8	μV
		T_A = –40°C to +125°C, V_S = 5.5 V	OPA4388			±10.5	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C, V_S = 5.5 V	OPA4388		±0.005	±0.05	μV/°C
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C	OPA4388		±1.25	±3.5	μV/V

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_B	Input bias current	R_{IN} = 100 kΩ, OPA4388			±30	±500	pA
			T_A = 0°C to +85°C			±600	
			T_A = –40°C to +125°C			±800	
I_{OS}	Input offset current	R_{IN} = 100 kΩ, OPA4388				±1000	
			T_A = 0°C to +85°C			±1100	
			T_A = –40°C to +125°C			±1100	
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz			0.14		μV_{PP}
		f = 10 Hz			7		
e_N	Input voltage noise density	f = 100 Hz			7		nV/√Hz
		f = 1 kHz			7		
		f = 10 kHz			7		
I_N	Input current noise density	f = 1 kHz			100		fA/√Hz
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
		(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	V_S = ±1.25 V OPA4388	102	110		
CMRR	Common-mode rejection ratio		V_S = ±2.75 V	124	140		dB
		(V–) < V_{CM} < (V+) + 0.1 V, T_A = –40°C to +125°C	V_S = ±1.25 V OPA4388	102	107		
		(V–) – 0.05 V < V_{CM} < (V+) + 0.1 V, T_A = –40°C to +125°C	V_S = ±2.75 V	124	140		
z_{id}	Differential input impedance				100 || 2		MΩ || pF
z_{ic}	Common-mode input impedance				60 || 4.5		TΩ || pF

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
A_{OL}	Open-loop voltage gain	(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ		126	148		dB
		(V–) + 0.15 V < V_O < (V+) – 0.15 V, R_{LOAD} = 10 kΩ, V_S = 5.5 V, T_A = –40°C to +125°C	OPA4388	120	126		
		(V–) + 0.25 V < V_O < (V+) – 0.25 V, R_{LOAD} = 2 kΩ		126	148		
		(V–) + 0.30 V < V_O < (V+) – 0.30 V, R_{LOAD} = 2 kΩ, V_S = 5.5 V, T_A = –40°C to +125°C	OPA4388	120	126		
GBW	Unity-gain bandwidth				10		MHz
SR	Slew rate	G = 1, 4-V step			5		V/µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 1 V_{RMS}			0.0005%		
t_S	Settling time	To 0.1%	V_S = ±2.5 V, G = 1, 1-V step		0.75		µs
		To 0.01%	V_S = ±2.5 V, G = 1, 1-V step		2		µs
t_{OR}	Overload recovery time	V_{IN} × G = V_S			10		µs
V_O	Voltage output swing from rail	Positive rail	No load		1	15	mV
			R_{LOAD} = 10 kΩ		5	20	
			R_{LOAD} = 2 kΩ		20	50	
		Negative rail	No load		5	15	
			R_{LOAD} = 10 kΩ		10	20	
			R_{LOAD} = 2 kΩ		40	60	
		T_A = –40°C to +125°C, both rails, R_{LOAD} = 10 kΩ			10	25	
I_{SC}	Short-circuit current	V_S = 5.5 V			±60		mA
		V_S = 2.5 V			±30		mA
C_{LOAD}	Capacitive load drive	See 图 6-26					
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A, see 图 6-25			100		Ω
I_Q	Quiescent current per amplifier	V_S = ±1.25 V (V_S = 2.5 V)	I_O = 0 A		1.7	2.4	mA
			T_A = –40°C to +125°C, I_O = 0 A		1.7	2.4	
		V_S = ±2.75 V (V_S = 5.5 V)	I_O = 0 A		1.9	2.6	
			T_A = –40°C to +125°C, I_O = 0 A		1.9	2.6	

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

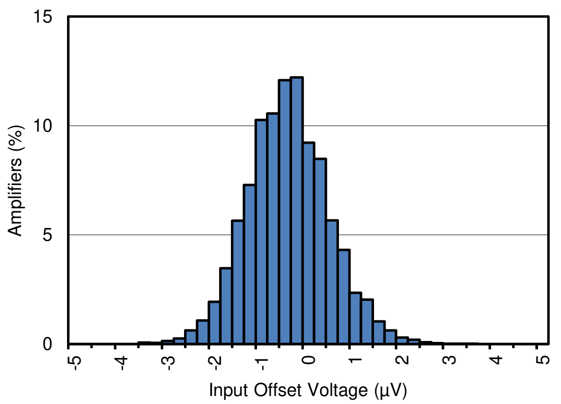


图 6-1. Offset Voltage Production Distribution

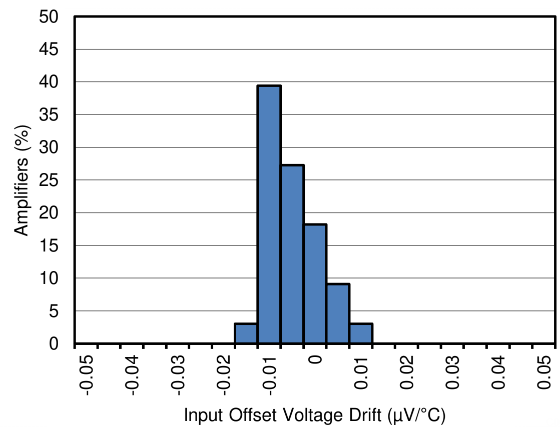


图 6-2. Offset Voltage Drift Distribution From −40°C to +125°C

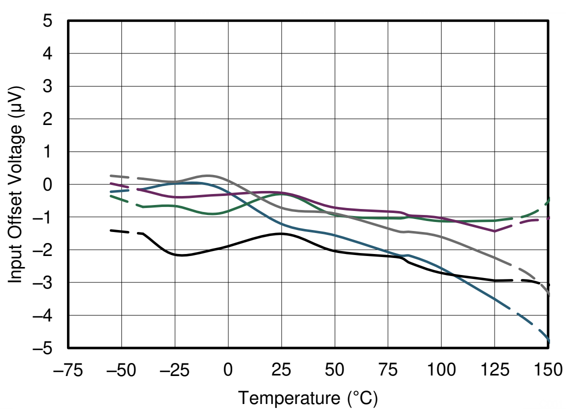


图 6-3. Offset Voltage vs Temperature

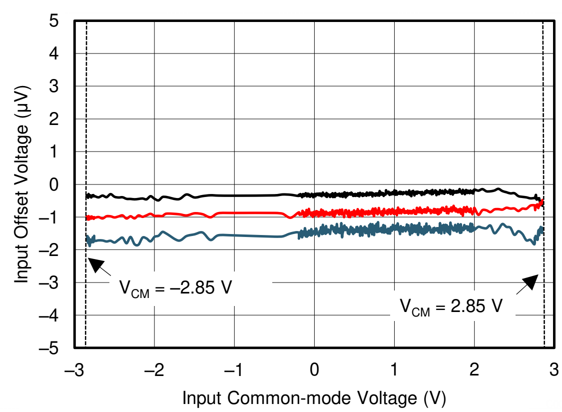


图 6-4. Offset Voltage vs Common-Mode Voltage

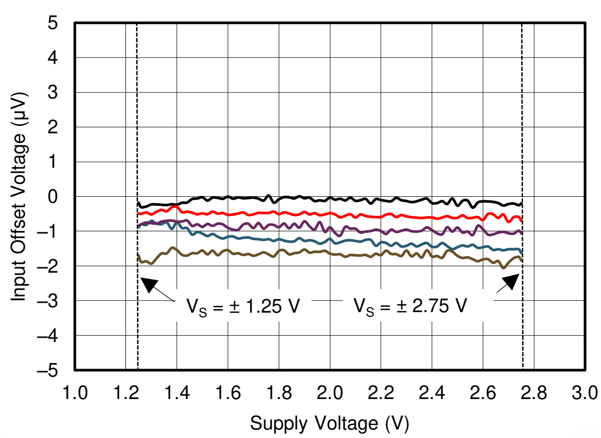


图 6-5. Offset Voltage vs Supply Voltage

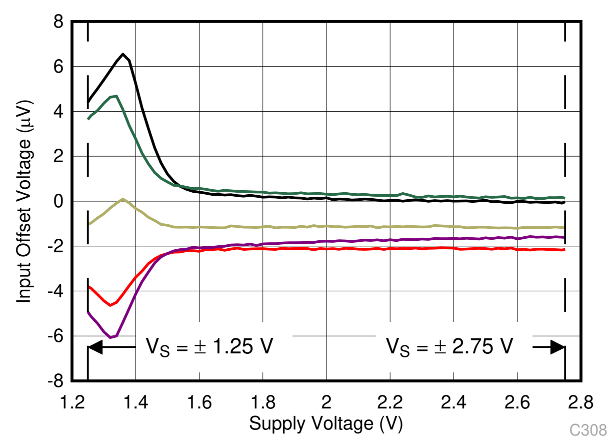


图 6-6. Offset Voltage vs Supply Voltage: OPA4388

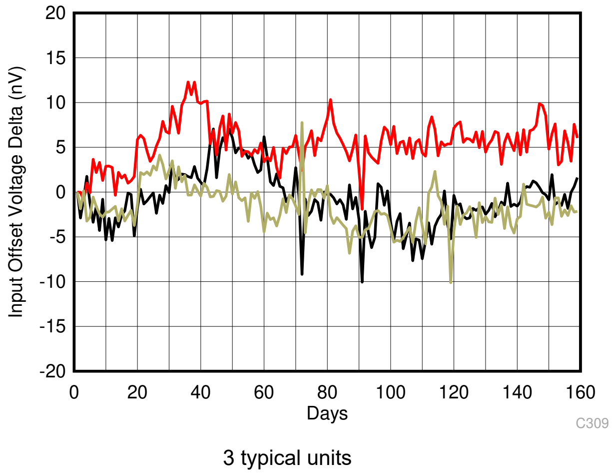


图 6-7. Offset Voltage Long Term Drift

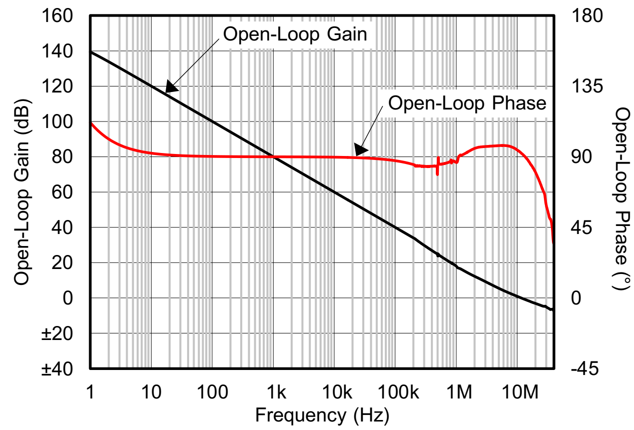


图 6-8. Open-Loop Gain and Phase vs Frequency

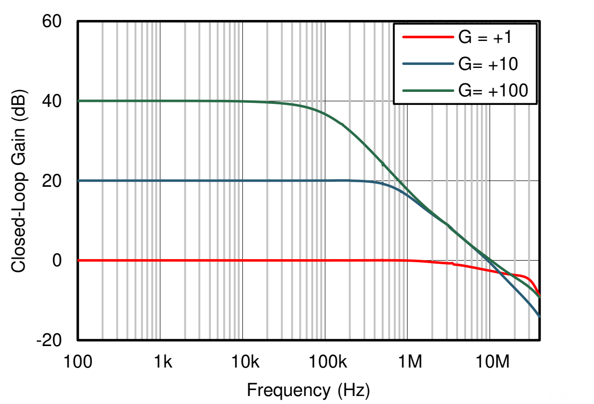


图 6-9. Closed-Loop Gain and Phase vs Frequency

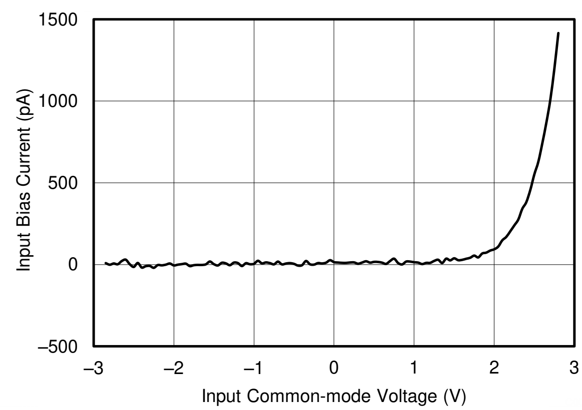


图 6-10. Input Bias Current vs Common-Mode Voltage

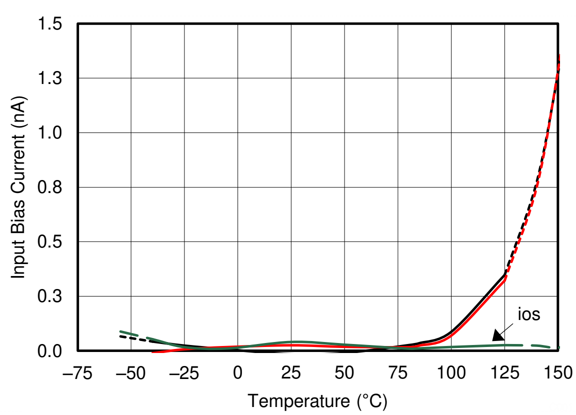


图 6-11. Input Bias Current vs Temperature

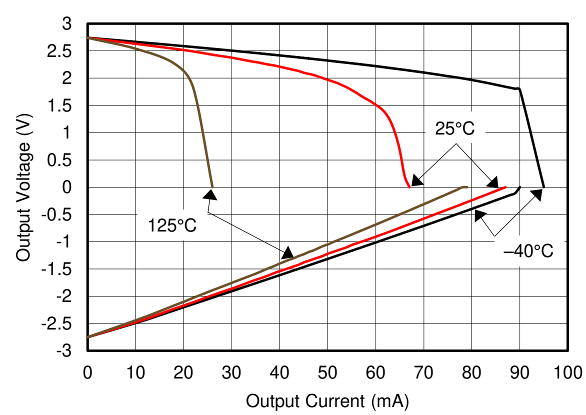


图 6-12. Output Voltage Swing vs Output Current (Maximum Supply)

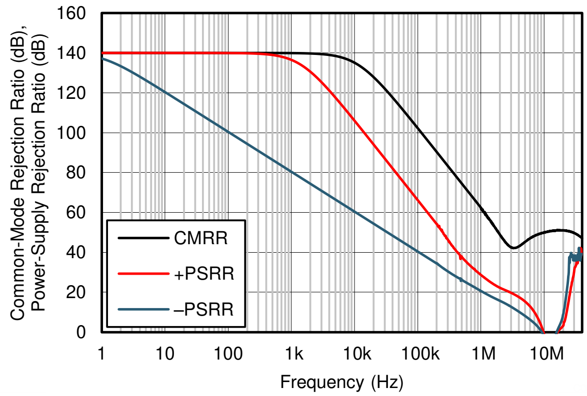


图 6-13. CMRR and PSRR vs Frequency

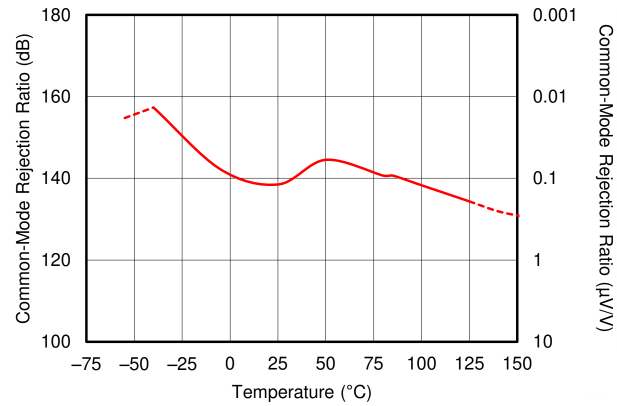


图 6-14. CMRR vs Temperature

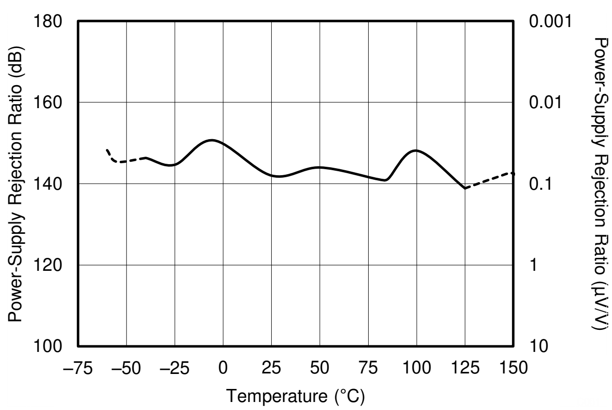


图 6-15. PSRR vs Temperature

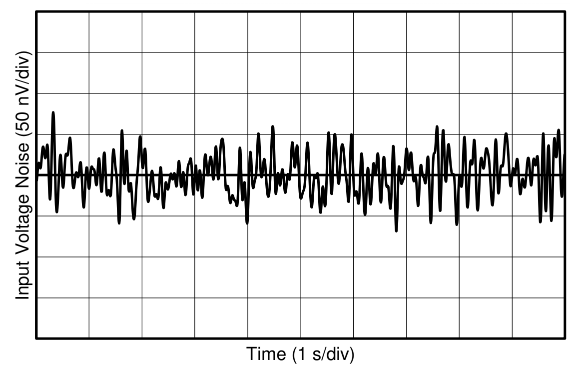


图 6-16. 0.1-Hz to 10-Hz Noise

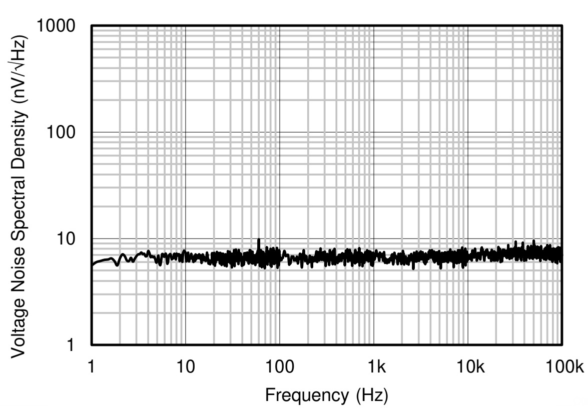


图 6-17. Input Voltage Noise Spectral Density vs Frequency

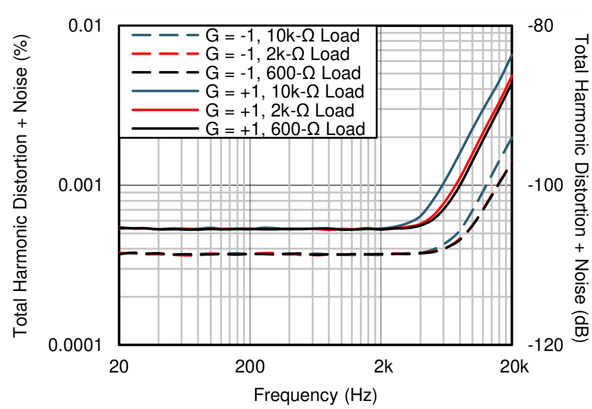


图 6-18. THD+N Ratio vs Frequency

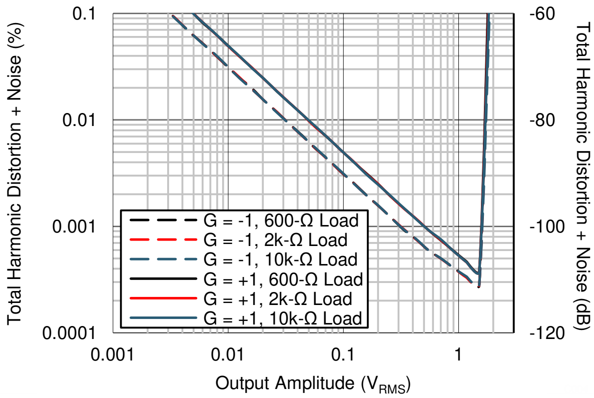


图 6-19. THD+N vs Output Amplitude

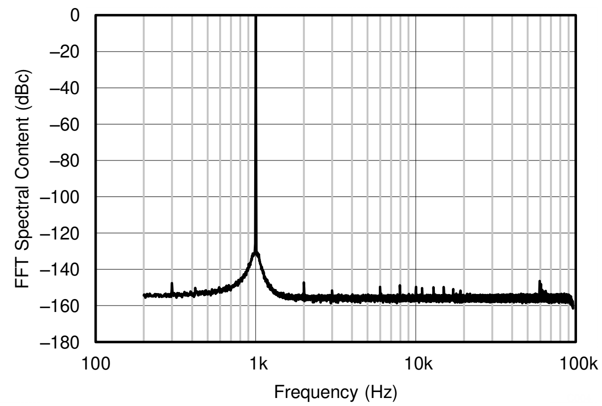


图 6-20. Spectral Content (With 10-kΩ Load)

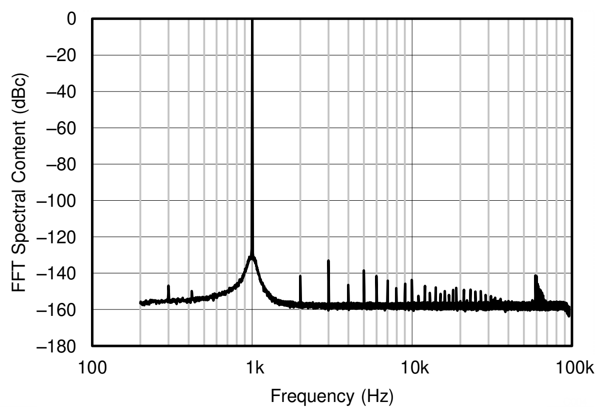


图 6-21. Spectral Content (With 2-kΩ Load)

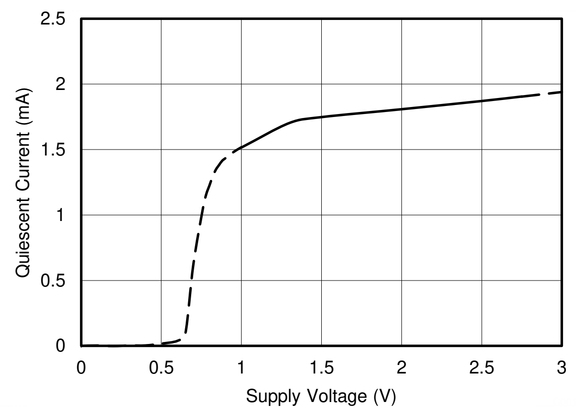


图 6-22. Quiescent Current vs Supply Voltage

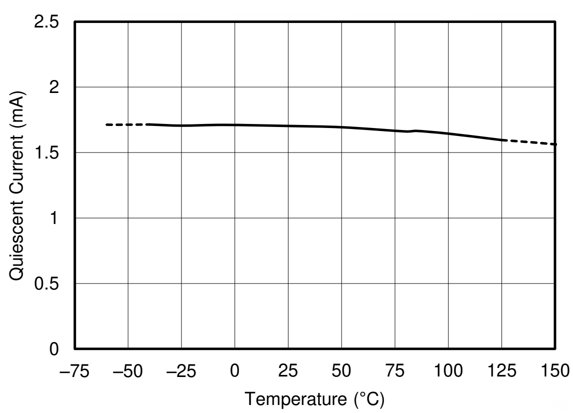


图 6-23. Quiescent Current vs Temperature

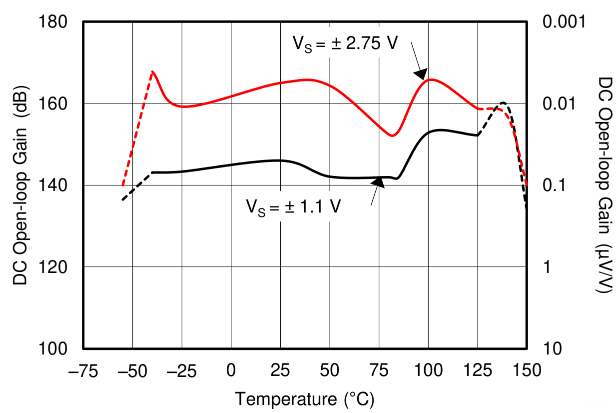


图 6-24. Open-Loop Gain vs Temperature

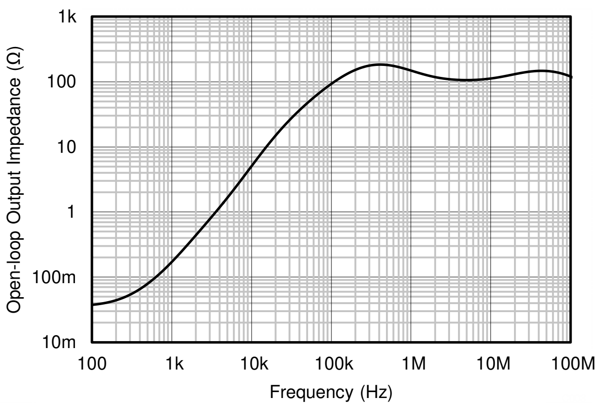


图 6-25. Open-Loop Output Impedance vs Frequency

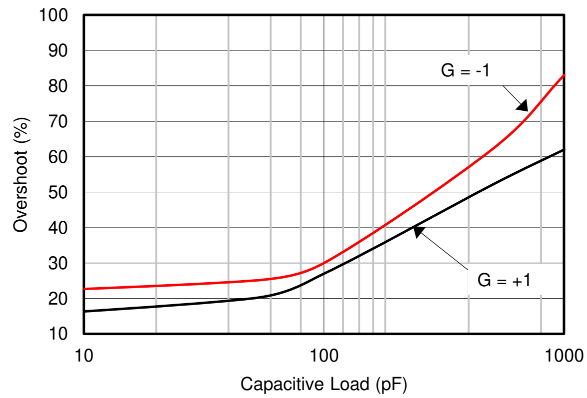


图 6-26. Small-Signal Overshoot vs Capacitive Load (10-mV Step)

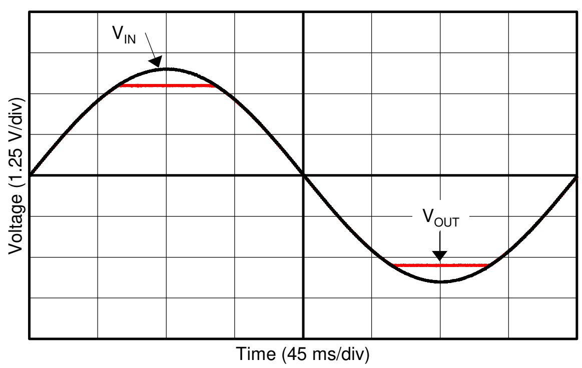


图 6-27. No Phase Reversal

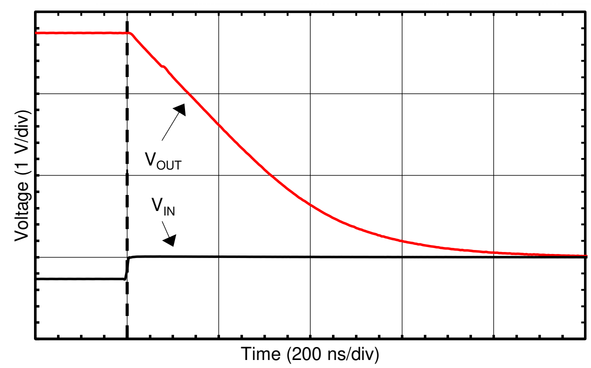


图 6-28. Positive Overload Recovery

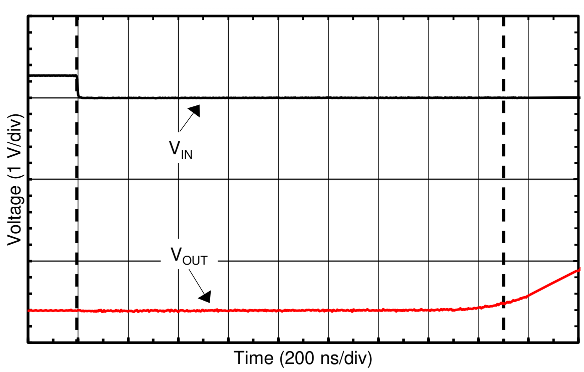
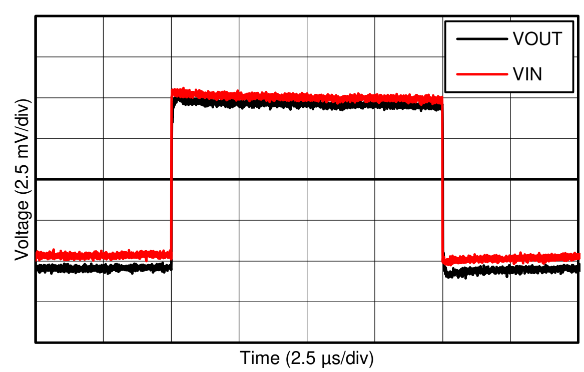
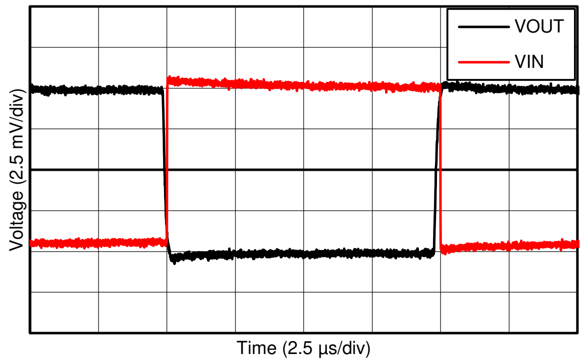


图 6-29. Negative Overload Recovery



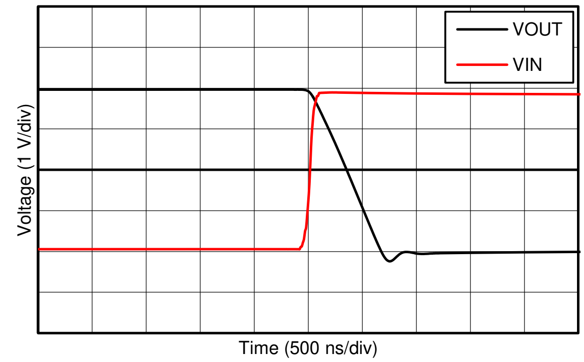
G = +1

图 6-30. Small-Signal Step Response (10-mV Step)



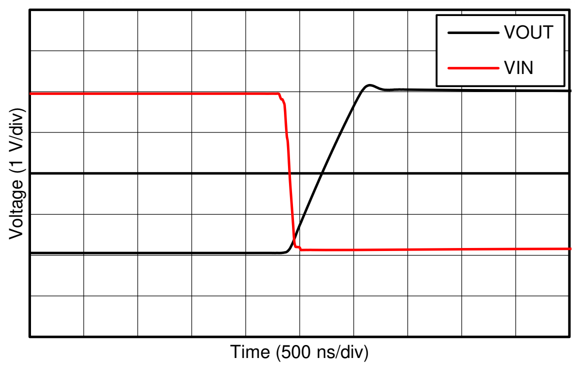
G = −1

图 6-31. Small-Signal Step Response (10-mV Step)



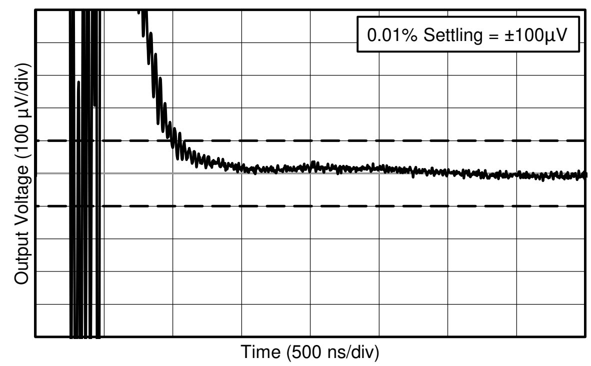
Falling output

图 6-32. Large-Signal Step Response (4-V Step)



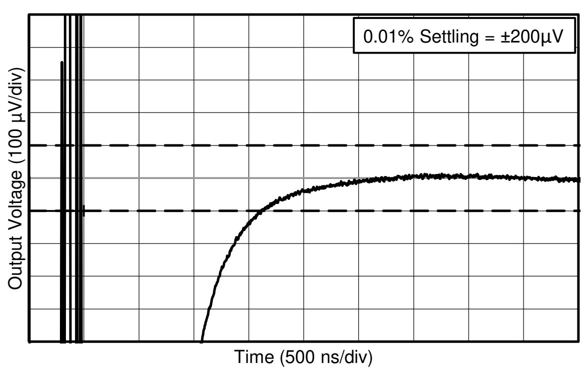
Rising output

图 6-33. Large-Signal Step Response (4-V Step)



0.01% settling = ±100 µV

图 6-34. Settling Time (1-V Positive Step)



0.01% settling = ±200 µV

图 6-35. Settling Time (1-V Negative Step)

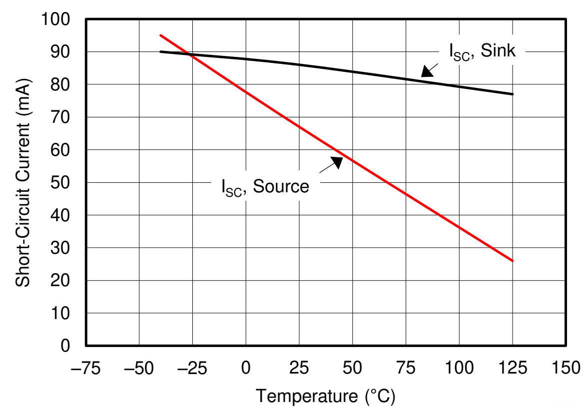


图 6-36. Short-Circuit Current vs Temperature

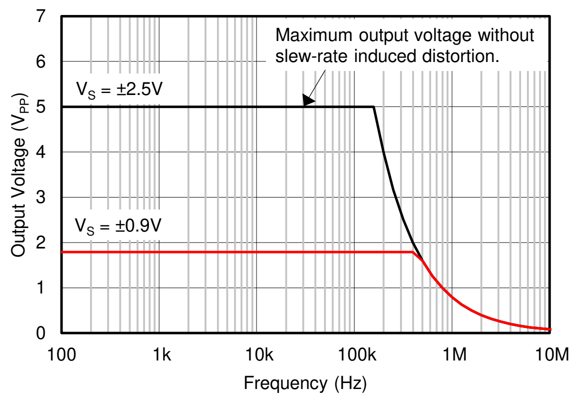


图 6-37. Maximum Output Voltage vs Frequency

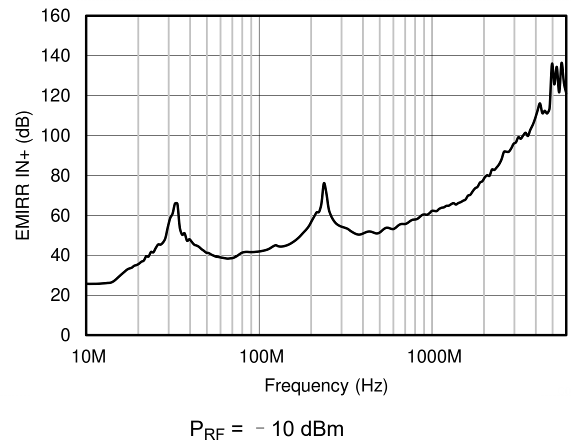
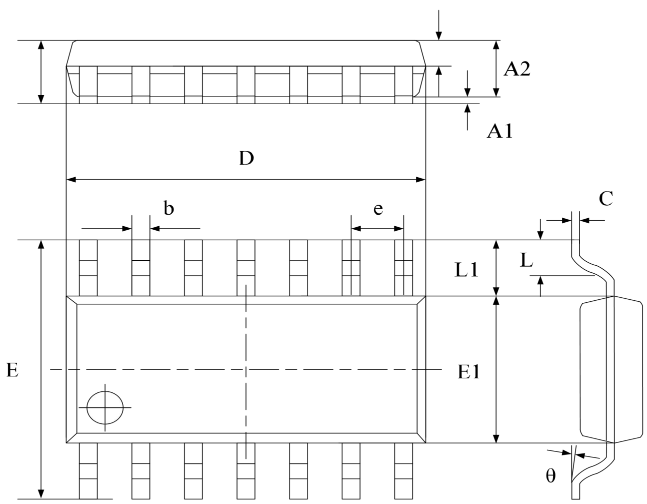


图 6-38. EMIRR vs Frequency

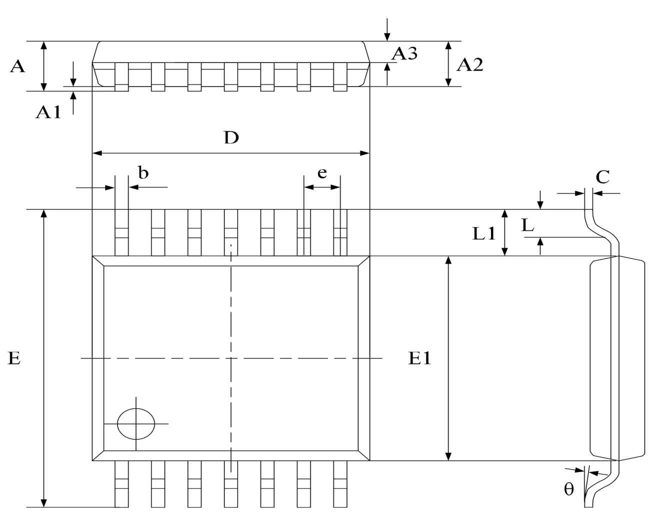
Package Dimension

SOP-14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.450	1.850	0.059	0.076
A1	0.100	0.300	0.004	0.012
A2	1.350	1.550	0.055	0.063
A3	0.550	0.750	0.022	0.031
b	0.406typ.		0.017typ.	
C	0.203typ.		0.008typ.	
D	8.630	8.830	0.352	0.360
E	5.840	6.240	0.238	0.255
E1	3.850	4.050	0.157	0.165
e	1.270 typ.		0.050 typ.	
L1	1.040 ref.		0.041 ref.	
L	0.350	0.750	0.014	0.031
θ	2°	8°	2°	8°

TSSOP-14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.200	-	0.0472
A1	0.050	0.150	0.002	0.006
A2	0.900	1.050	0.037	0.043
A3	0.390	0.490	0.016	0.020
b	0.200	0.290	0.008	0.012
C	0.130	0.180	0.005	0.007
D	4.860	5.060	0.198	0.207
E	6.200	6.600	0.253	0.269
E1	4.300	4.500	0.176	0.184
e	0.650 typ.		0.0256 typ.	
L1	1.000 ref.		0.0393 ref.	
L	0.450	0.750	0.018	0.031
θ	0°	8°	0°	8°

Marking

Ordering information

Order code	Package	Baseqty	Deliverymode
UMW OPA4388ID	SOP-14	2500	Tape and reel
UMW OPA4388IDR	SOP-14	2500	Tape and reel
UMW OPA4388IPWR	TSSOP-14	4000	Tape and reel