

DESCRIPTION

The SLP74LV1T08 is a single, level translating 2-input AND gate. The input is designed with a lower threshold circuit to match 1.8 V input logic at $V_{CC} = 3.3V$ and can be used in 1.8V to 3.3V level up translation. In addition, the 5V tolerant input pins enable level down translation (3.3V to 2.5V output at $V_{CC} = 2.5V$).

The output level is referenced to the supply voltage and supports 1.8V, 2.5V, 3.3V and 5.0V CMOS levels. The wide V_{CC} range of 1.6V to 5.5V allows generation of desired output levels to connect to controllers or processors.

FEATURES

- Single supply voltage translator at 1.8V, 2.5V, 3.3V and 5.0V
- Logic output is referenced to V_{CC}
- Input accept voltages up to 5V
- Up translation
 - 1.2V to 1.8V at $V_{CC} = 1.8V$
 - 1.8V 1.5V to 2.5V at $V_{CC} = 2.5V$
 - 1.8V to 3.3V at $V_{CC} = 3.3V$
 - 3.3V to 5.0V at $V_{CC} = 5.0V$
- Down translation
 - 3.3V to 1.8V at $V_{CC} = 1.8V$
 - 3.3V to 2.5V at $V_{CC} = 2.5V$
 - 5.0V to 3.3V at $V_{CC} = 3.3V$
- ESD protection:
 - HBM Exceeds 2000V
 - CDM Exceeds 1000V
- Latch-up performance exceeds 250mA
- Specified from $-40^{\circ}C$ to $+85^{\circ}C$ and from $-40^{\circ}C$ to $+125^{\circ}C$

BLOCK DIAGRAM

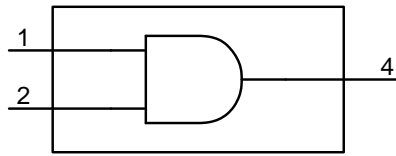


Fig.1 Function diagram

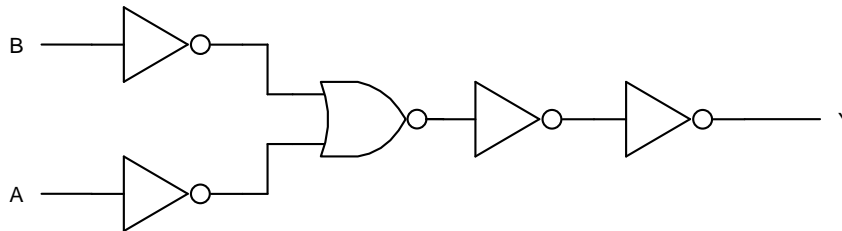


Fig.2 Logic diagram

PIN CONFIGURATION

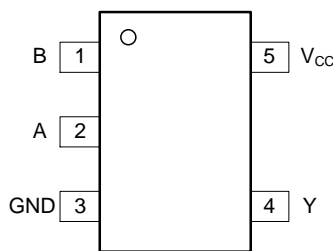


Fig.3 Pin configuration

PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1	B	I	Data input
2	A	I	Data input
3	GND	/	Ground
4	Y	O	Data output
5	V _{CC}	/	Supply voltage

FUNCTIONAL DESCRIPTION^[1]

Input A	Input B	Output Y
L	L	L
L	H	L
H	L	L
H	H	H

[1] H = HIGH voltage level;

L = LOW voltage level.

LIMITING VALUES

Characteristics	Symbol	Conditions	Min.	Max.	Unit
Supply voltage	V_{CC}		-0.5	+7.0	V
Input voltage	V_I		-0.5	+7.0	V
Input clamping current	I_{IK}	$V_I < 0V^{[1]}$	-20		mA
Output clamping current	I_{OK}	$V_O < 0V$ or $V_O > V_{CC}^{[1]}$	-20	+20	mA
Output voltage	V_O	Active mode	-0.5	$V_{CC}+0.5$	V
		Power-down mode	-0.5	+4.6	V
Output current	I_O	$V_O = 0V$ to V_{CC}	-25	+25	mA
Supply current	I_{CC}			+50	mA
Ground current	I_{GND}		-50		mA
Storage temperature	T_{stg}		-65	+150	°C
Thermal resistance, junction to ambient	R_{thJA}			239	°C/W
Latch up	LU	$T_A = 25^\circ C, 125^\circ C$	250		mA
ESD human-body model	ESD-HBM	$T_A = 25^\circ C$	2000		V
ESD charged-device model	ESD-CDM	$T_A = 25^\circ C$	1000		V

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITION (UNLESS OTHERWISE SPECIFIED $T_A = 25^\circ C$)

Voltages are referenced to GND (ground = 0V)

Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}		1.6		5.5	V
Input voltage	V_I		0		5.5	V
Output voltage	V_O		0		V_{CC}	V
Ambient temperature	T_A		-40	+25	+125	°C
Input transition rise and fall rate	$\Delta t/\Delta V$	$V_{CC} = 1.8V$ to $5.5V$			20	ns/V

STATIC CHARACTERISTICS

Voltages are referenced to GND (ground = 0V)

Characteristics	Symbol	Test condition	25°C		-40°C to 85°C		-40°C to +125°C		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
HIGH-level input voltage	V_{IH}	$V_{CC} = 1.65V$ to 1.8V	0.94		1.0		1.0		V
		$V_{CC} = 2.0V$	0.99		1.03		1.03		V
		$V_{CC} = 2.25V$ to 2.5V	1.135		1.18		1.18		V
		$V_{CC} = 2.75V$	1.21		1.23		1.23		V
		$V_{CC} = 3.0V$ to 3.3V	1.35		1.37		1.37		V
		$V_{CC} = 3.6V$	1.47		1.48		1.48		V
		$V_{CC} = 4.5V$ to 5.5V	2.02		2.03		2.03		V
		$V_{CC} = 5.5V$	2.10		2.11		2.11		V
LOW-level input voltage	V_{IL}	$V_{CC} = 1.65V$ to 2.0V		0.58		0.55		0.55	V
		$V_{CC} = 2.25V$ to 2.75V		0.75		0.71		0.71	V
		$V_{CC} = 3.0V$ to 3.6V		0.80		0.80		0.80	V
		$V_{CC} = 4.5V$ to 5.5V		0.80		0.80		0.80	V
HIGH-level output voltage	V_{OH}	$V_I = V_{IH}$ or V_{IL}							
		$I_O = -20\mu A$; $V_{CC} = 1.65V$ to 5.5V	$V_{CC}-0.1$		$V_{CC}-0.1$		$V_{CC}-0.1$		V
		$I_O = -2mA$; $V_{CC} = 1.65V$	1.28		1.21		1.21		V
		$I_O = -2mA$; $V_{CC} = 1.8V$	1.5		1.45		1.45		V
		$I_O = -2.3mA$; $V_{CC} = 2.3V$	2.0		2.0		2.0		V
		$I_O = -3mA$; $V_{CC} = 2.3V$	2.0		1.93		1.93		V
		$I_O = -3mA$; $V_{CC} = 2.5V$	2.25		2.15		2.15		V
		$I_O = -3mA$; $V_{CC} = 3.0V$	2.78		2.7		2.7		V
		$I_O = -5.5mA$; $V_{CC} = 3.0V$	2.6		2.49		2.49		V
		$I_O = -5.5mA$; $V_{CC} = 3.3V$	2.9		2.8		2.8		V
		$I_O = -4mA$; $V_{CC} = 4.5V$	4.2		4.1		4.1		V
		$I_O = -8mA$; $V_{CC} = 4.5V$	4.1		3.95		3.95		V
$I_O = -8mA$; $V_{CC} = 5.0V$	4.6		4.5		4.5		V		
LOW-level output voltage	V_{OL}	$V_I = V_{IH}$ or V_{IL}							
		$I_O = 20\mu A$; $V_{CC} = 1.65V$ to 5.5V		0.1		0.1		0.1	V
		$I_O = 2mA$; $V_{CC} = 1.65V$		0.2		0.25		0.25	V
		$I_O = 2.3mA$; $V_{CC} = 2.3V$		0.1		0.15		0.15	V
		$I_O = 3mA$; $V_{CC} = 2.3V$		0.15		0.2		0.2	V
		$I_O = 3mA$; $V_{CC} = 3.0V$		0.1		0.15		0.15	V
		$I_O = 5.5mA$; $V_{CC} = 3.0V$		0.2		0.25		0.25	V
$I_O = 4mA$; $V_{CC} = 4.5V$		0.15		0.2		0.2	V		

Characteristics	Symbol	Test condition	25°C		-40°C to 85°C		-40°C to +125°C		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
		$I_o = 8\text{mA}; V_{CC} = 4.5\text{V}$		0.3		0.35		0.35	V
Input leakage current	I_i	$V_i = 5.5\text{V or GND}; V_{CC} = 0\text{V to } 5.5\text{V}$		± 0.1		± 1.0		± 1.0	μA
Supply current	I_{CC}	$V_i = V_{CC} \text{ or GND}; I_o = 0\text{A}; V_{CC} = 1.65\text{V to } 5.5\text{V}$		1.0		10		10	μA
Additional supply current	ΔI_{CC}	Per input pin; $V_{CC} = 1.8\text{V}$ $V_i = 0.3\text{V or } 1.1\text{V};$ $I_o = 0\text{A};$ other pins at V_{CC} or GND		10		10		10	μA
		Per input pin; $V_{CC} = 5.5\text{V}$ $V_i = 0.3\text{V or } 3.4\text{V};$ $I_o = 0\text{A};$ other pins at V_{CC} or GND		1.35		1.5		1.5	mA

DYNAMIC CHARACTERISTICS

GND = 0V. For test circuit, see WAVEFORMS.

Characteristics	Symbol	Test condition	-40°C to +125°C					Unit
			Min.	Typ. 25°C	Max. 25°C	Max. 85°C	Max. 125°C	
Propagation delay	t_{pd}	A, B to Y; ^[1]						
		$V_{CC} = 1.8\text{V}; C_L = 15\text{pF}$		9.3	14.0	16.2	16.7	ns
		$V_{CC} = 1.8\text{V}; C_L = 30\text{pF}$		10.2	15.3	17.9	18.4	ns
		$V_{CC} = 2.5\text{V}; C_L = 15\text{pF}$		5.9	8.6	10.1	10.6	ns
		$V_{CC} = 2.5\text{V}; C_L = 30\text{pF}$		6.6	9.6	11.1	11.6	ns
		$V_{CC} = 3.3\text{V}; C_L = 15\text{pF}$		4.4	6.2	7.2	7.5	ns
		$V_{CC} = 3.3\text{V}; C_L = 30\text{pF}$		5.2	7.3	8.6	8.9	ns
		$V_{CC} = 5.0\text{V}; C_L = 15\text{pF}$		3.4	4.4	4.9	5.1	ns
		$V_{CC} = 5.0\text{V}; C_L = 30\text{pF}$		3.6	4.7	5.2	5.4	ns
Input capacitance	C_i			3.6	10	10	10	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

WAVEFORMS

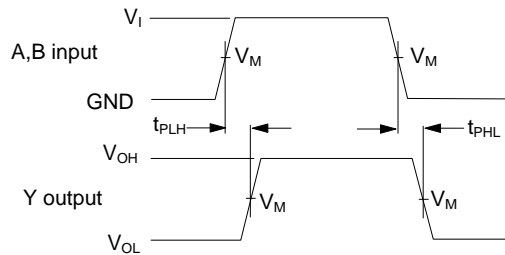


Fig.4 The input (A, B) to output (Y) propagation delays

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Measurement points: $V_M=0.5 \cdot V_{CC}$;

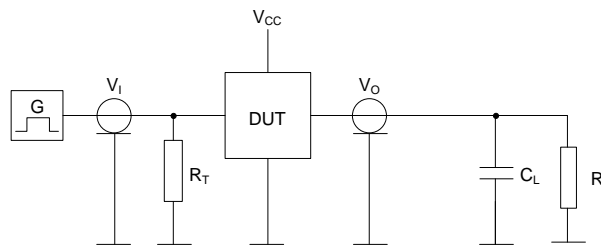
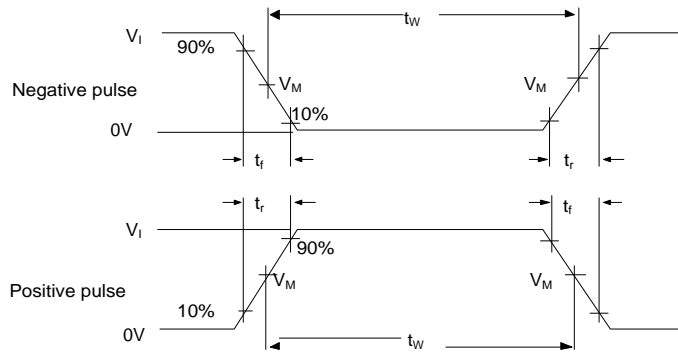


Fig.5 Definitions test circuit

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

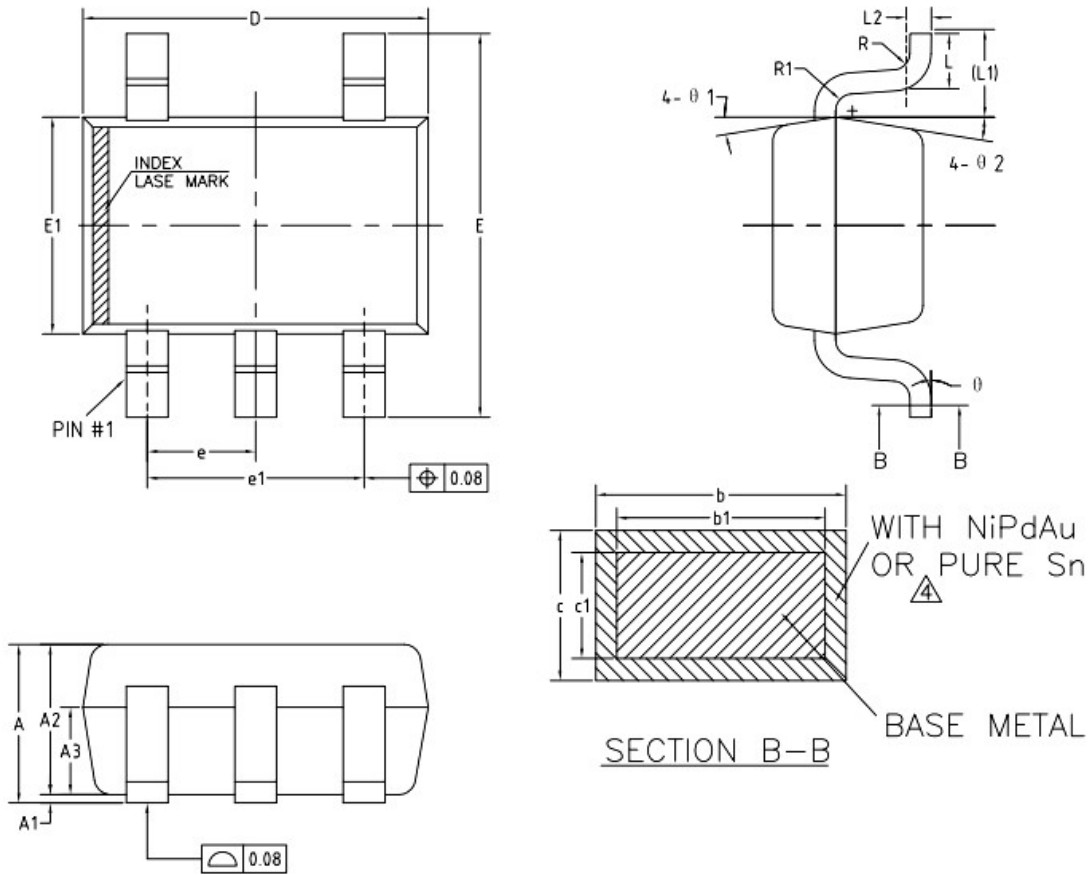
R_L = Load resistor

Test data

Supply voltage	Input			Load	
	V_I	t_r, t_f	f_{max}	C_L	R_L
1.8V	V_{CC}	$\leq 3.0ns$	15MHz	15pF, 30pF	1M Ω
2.5V	V_{CC}	$\leq 3.0ns$	25MHz	15pF, 30pF	1M Ω
3.3V	3V	$\leq 3.0ns$	50MHz	15pF, 30pF	1M Ω
5.0V	3V	$\leq 3.0ns$	50MHz	15pF, 30pF	1M Ω

Package Dimension

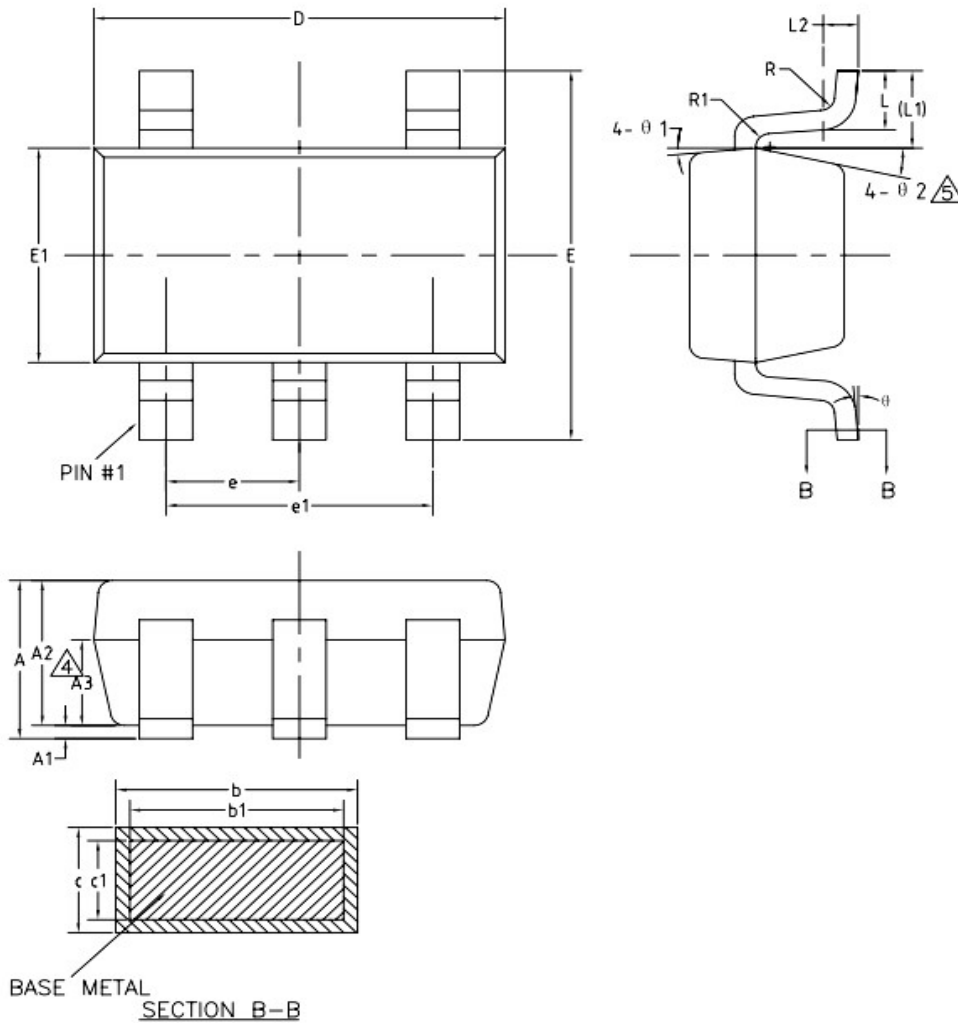
SC70-5



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX	
A	0.85	—	1.05	
A1	0	—	0.10	
A2	0.80	0.90	1.00	
A3	0.47	0.52	0.57	
b	NiPdAu	0.22	—	0.29
	PURE Sn	0.23	—	0.33
b1	0.22	0.25	0.28	
c	NiPdAu	0.115	—	0.15
	PURE Sn	0.12	—	0.18
c1	0.115	0.13	0.14	
D	2.02	2.07	2.12	
E	2.20	2.30	2.40	
E1	1.25	1.30	1.35	
e	0.60	0.65	0.70	
e1	1.20	1.30	1.40	
L	0.28	0.33	0.38	
L1	0.50REF			
L2	0.15BSC			
R	0.10	—	—	
R1	0.10	—	0.25	
theta	0°	—	8°	
theta 1	6°	9°	12°	
theta 2	6°	9°	12°	

SOT23-5



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.25
Δ A1	0	—	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.36	—	0.50
b1	0.36	0.38	0.45
c	0.14	—	0.20
c1	0.14	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	0.90	0.95	1.00
Δ e1	1.80	1.90	2.00
L	0.35	0.45	0.60
L1	0.59REF		
L2	0.25BSC		
R	0.10	—	—
R1	0.10	—	0.25
θ	0°	—	8°
θ 1	3°	5°	7°
Δ θ 2	6°	—	14°

information

Order code	Marking code	Package	Baseqty	Deliverymode
UMW SN74LV1T08DBVR	NEE3	SOT23-5	3000	Tape and reel
UMW SN74LV1T08DCKR	WE3	SC70-5	3000	Tape and reel

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