

Product introduction

SN74LVC1G08 is a 2-input AND gate integrated circuit, which can realize the mathematical logic operation of $Y = A \cdot B$ and $Y = \overline{A + B}$. Advanced CMOS process design is adopted, which has the working characteristics of low power consumption and high output driving capability. The chip can work normally when the power supply voltage VCC is between 1.65V and 5.5V V. And 74LVC1G08 has a variety of small package shapes, It can be widely used in high-end precision instruments, miniaturized low-power handheld devices, artificial intelligence and other fields.

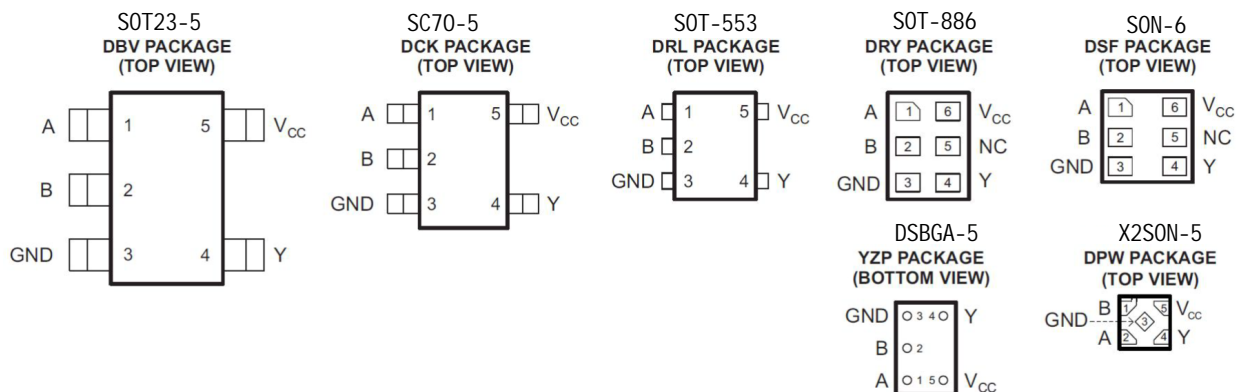
Product features

- Low input current: 0.1uA typical
- Low static power consumption: 0.1uA typical
- High output drive: VCC=4.5V, more than 32MA
- Wide working voltage range: 1.65V to 5.5V
- Package form: DBV/DCK/DRL/YZP/ DRY/DSF/ DPW

product usage

- Portable audio interface
- digital television
- Wireless headphones, smart watches, etc.
- Blu-ray player and home theater
- Solid state drive
- Smart wearable devices

Package form and pin function definition



NAME	PIN			DESCRIPTION
	DBV, DCK, DRL, YZP	DRY, DSF	DPW	
A	1	1	2	Input
B	2	2	1	Input
GND	3	3	3	Ground
Y	4	4	4	Output
V _{CC}	5	6	5	Power pin
NC		5		Not connected

Note: NC null pin, no connecting wire inside.

■ Limit parameter

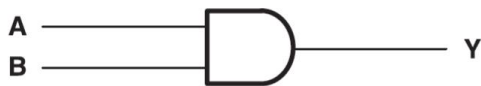
parameter	symbol	limit value	unit
operating voltage	V _{CC}	6.5	V
input	V _{IN}	-0.5~6.5	V
Output voltage (1)	V _{OUT}	-0.5~6.5	V
Single pin output current	I _{OUT}	25	mA
Or Vcc current.	I _{CC}	50	mA
Storage temperature	T _S	-65-150	°C
Pin welding temperature	T _W	260, 10s	°C
Working temperature	T _A	-40-105	°C

Note: 1. Under the condition of V_{CC} = 0V power-off, the output can withstand the limit voltage,

2. Limit parameter refers to the limit value that cannot be exceeded under any condition. In case of exceeding this limit value, physical properties such as product degradation may be caused Damage;

At the same time, the chip can not be guaranteed to work normally under the near limit parameters.

■ Principle logic diagram



■ truth table

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

■ working conditions

project	symbol	test condition	minimum value	typical value	maximum	unit
operating voltage	V _{CC}	-	1.65	-	5.5	V
Input high level voltage	V _{IH}	V _{CC} =1.65V~1.95V	0.65* V _{CC}	-	-	V
		V _{CC} =2.3V~2.7V	1.7V	-	-	
		V _{CC} =3V~5.5V	0.7* V _{CC}	-	-	
Low-Level Input Voltage	V _{IL}	V _{CC} =1.65V~1.95V	-	-	0.35* V _{CC}	V
		V _{CC} =2.3V~2.7V	-	-	0.7	
		V _{CC} =3V~5.5V	-	-	0.3* V _{CC}	
input voltage	V _I	-	0	-	5.5	V
Output voltage	V _O	-	0	-	V _{CC}	V
High level output current	I _{OH}	V _{CC} =1.65V	-	-	-4	mA
		V _{CC} =2.3V	-	-	-8	
		V _{CC} =3V	-	-	-16	
		V _{CC} =4.5V	-	-	-32	
Low level output current	I _{OL}	V _{CC} =1.65V	-	-	4	mA
		V _{CC} =2.3V	-	-	8	
		V _{CC} =3V	-	-	16	
		V _{CC} =4.5V	-	-	32	

Electrical characteristics

Electrical characteristics of DC: $T_A=25^{\circ}\text{C}$

project	symbol	test condition	V_{CC}	typical value	maximum	unit
High level load voltage	V_{OH}	$I_{OH}=-100\mu\text{A}$	1.65V~5.5V	1.64	-	V
		$I_{OH}=-4\text{ mA}$	1.65V	1.47	-	
		$I_{OH}=-8\text{ mA}$	2.3V	2.15	-	
		$I_{OH}=-16\text{ mA}$	3V	2.73	-	
		$I_{OH}=-32\text{ mA}$	4.5V	4.0	-	
Low level load voltage	V_{OL}	$I_{OH}=100\mu\text{A}$	1.65V~5.5V	0.01	-	V
		$I_{OH}=4\text{ mA}$	1.65V	0.11	-	
		$I_{OH}=8\text{ mA}$	2.3V	0.11	-	
		$I_{OH}=16\text{ mA}$	3V	0.2	-	
		$I_{OH}=32\text{ mA}$	4.5V	0.35	-	
incoming current	I_I	VI =5.5V or GND	0~5.5V	A	± 5	uA
				B	± 5	
Turn-off current	I_{OFF}	$V_I=5.5\text{V}$	0	0.01	± 10	uA
		$V_O=5.5\text{V}$	0	0.01	± 10	
operational current	I_{CC}	$V_I=5.5\text{V}, I_O=0$	1.65V~5.5V	0.01	10	uA
		$V_I=\text{GND}, I_O=0$		0.01	10	
Working current variation value	ΔI_{CC}	A= $V_{CC}-0.6\text{V}$ B=VCC or GND	3V~5.5V	25	-	uA
		B= $V_{CC}-0.6\text{V}$ A= VCC or GND		25	-	

Ac electrical characteristics: $T_A=25^{\circ}\text{C}$ V(298)=5.0V, $t_r \leq 20\text{ns}$. See test method.

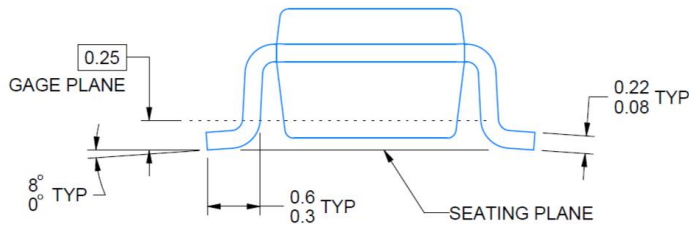
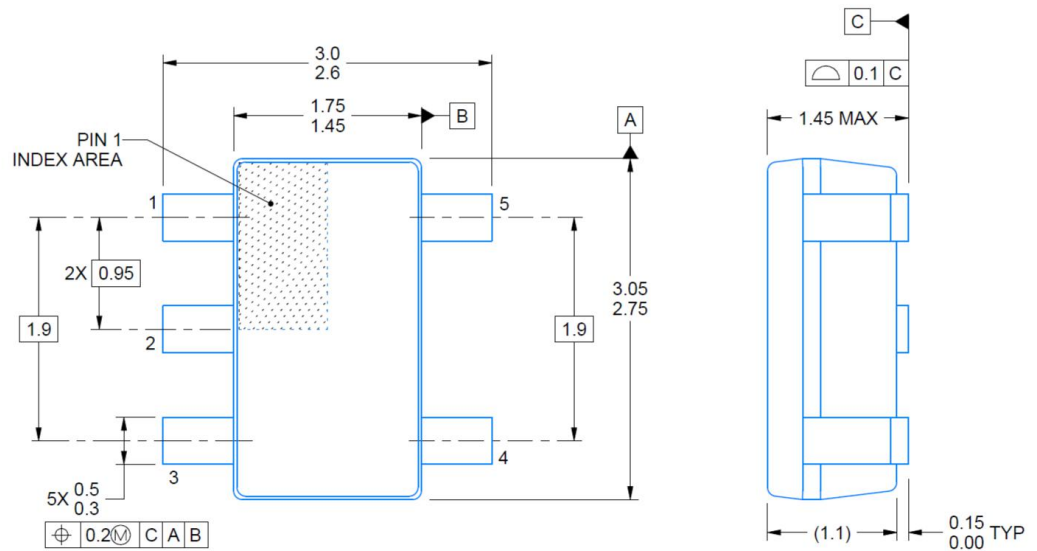
project	symbol	test condition	minimum value	typical value	maximum	unit
Maximum transmission delay time a, B to Y	t_{PHL}	$C_L=15\text{pF}$	-	10	-	ns
	t_{PLH}	$C_L=15\text{pF}$	-	10	-	ns

Note: 1. CL capacitor is external chip capacitor (0603), which is connected close to the output pin, and the capacitor ground is close to the chip GND; 2. Input: port input level, $f=500\text{kHz}, D=50\%$; $t_r=t_f \leq 20\text{ns}$;
3. Output: Y-terminal output test.

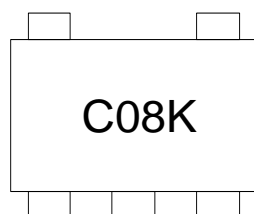
■ Encapsulated information

Unit: mm/inch

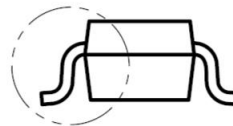
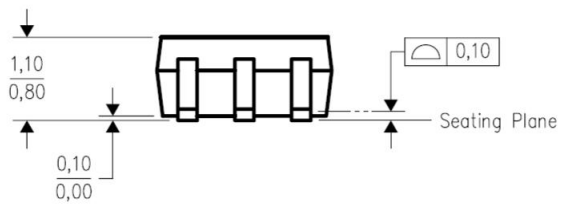
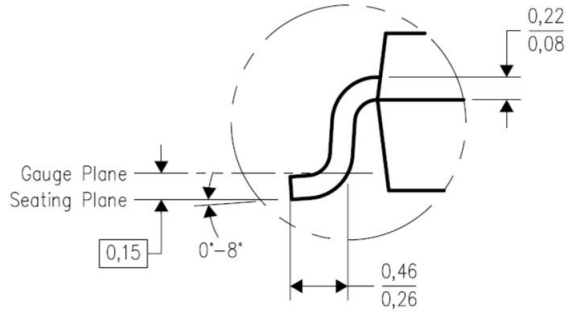
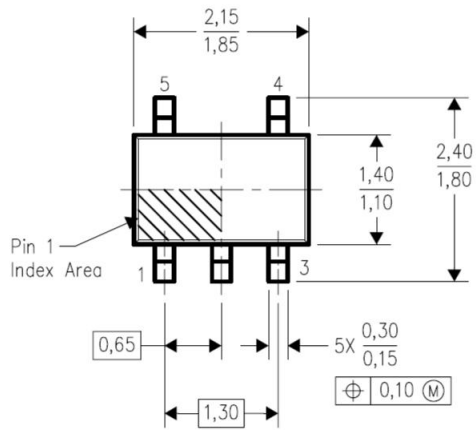
DBV (SOT23-5)



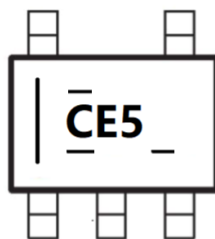
■ Marking



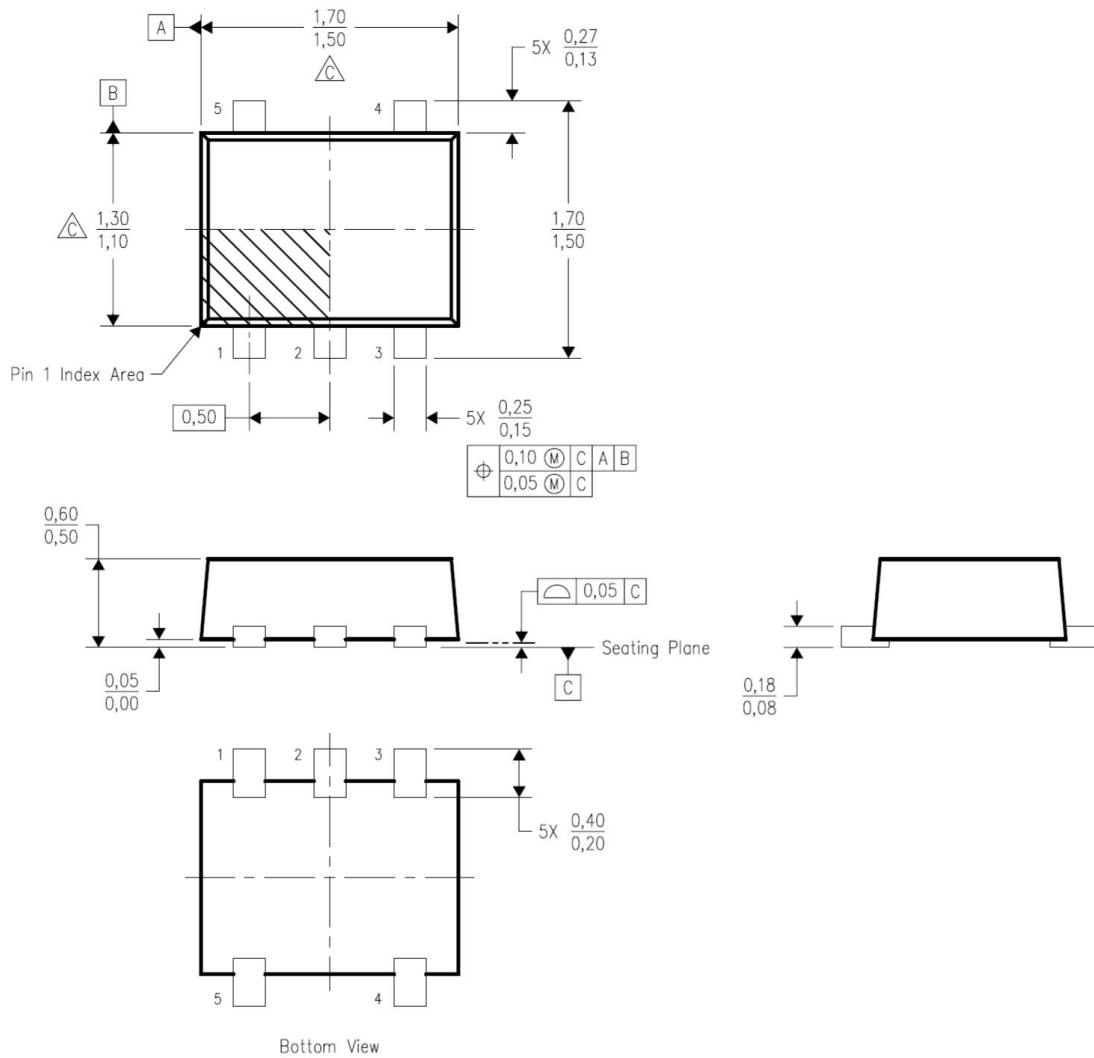
DCK (SC70-5)



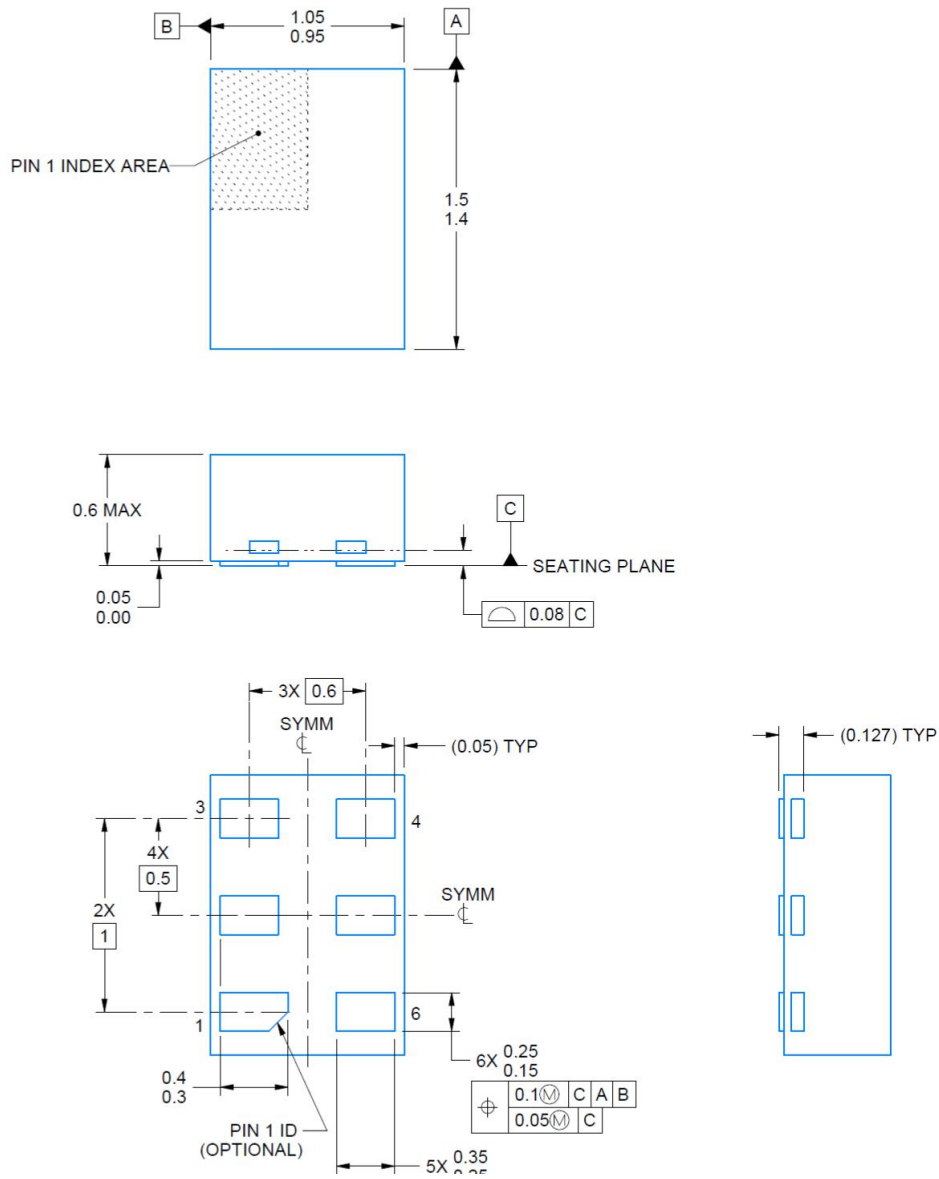
■ Marking



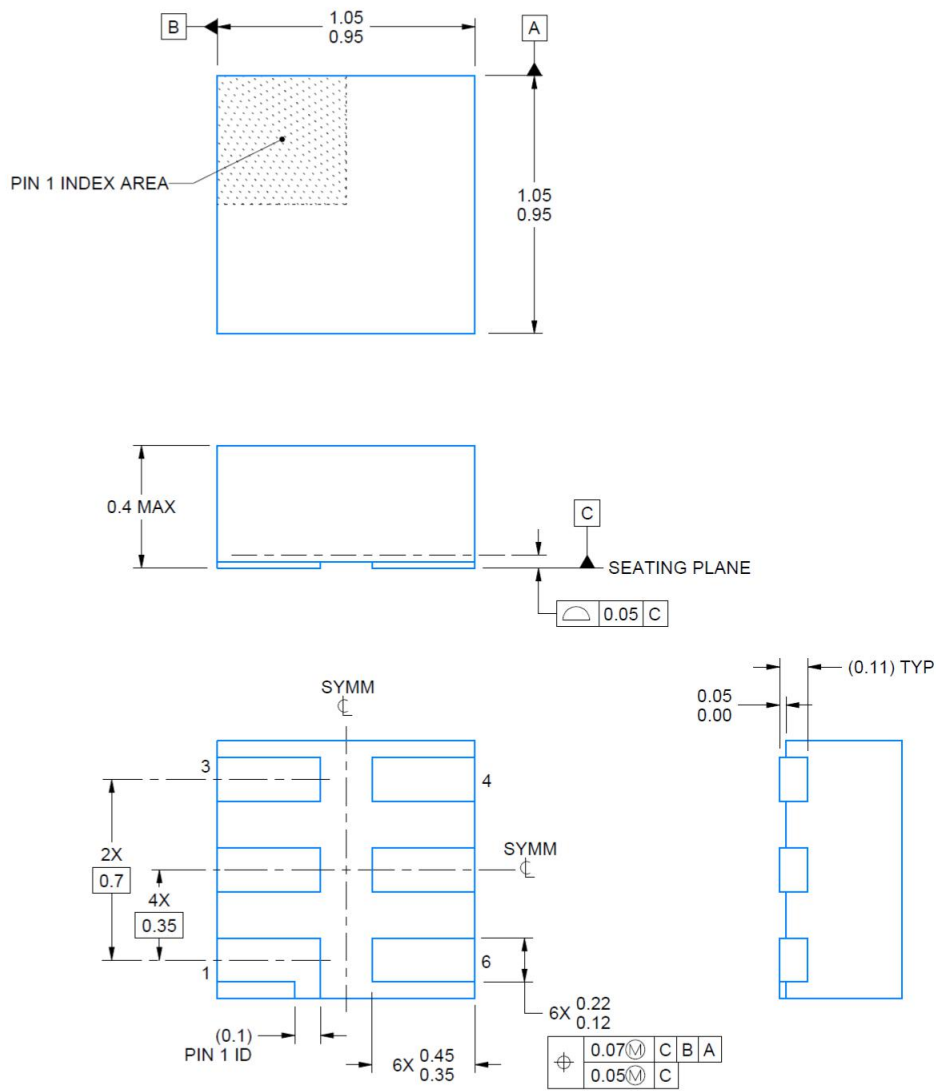
DRL (SOT-553)



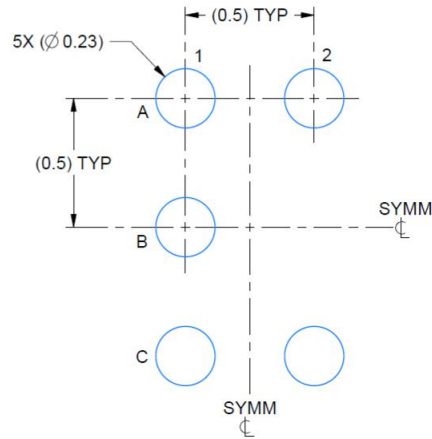
DRY (SOT-886)



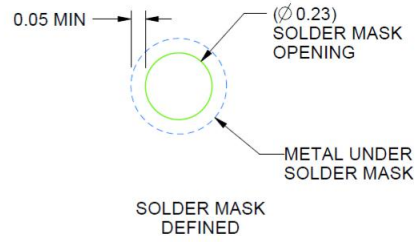
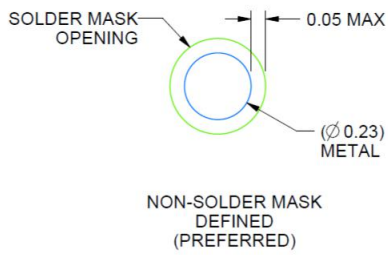
DSF (SON-6)



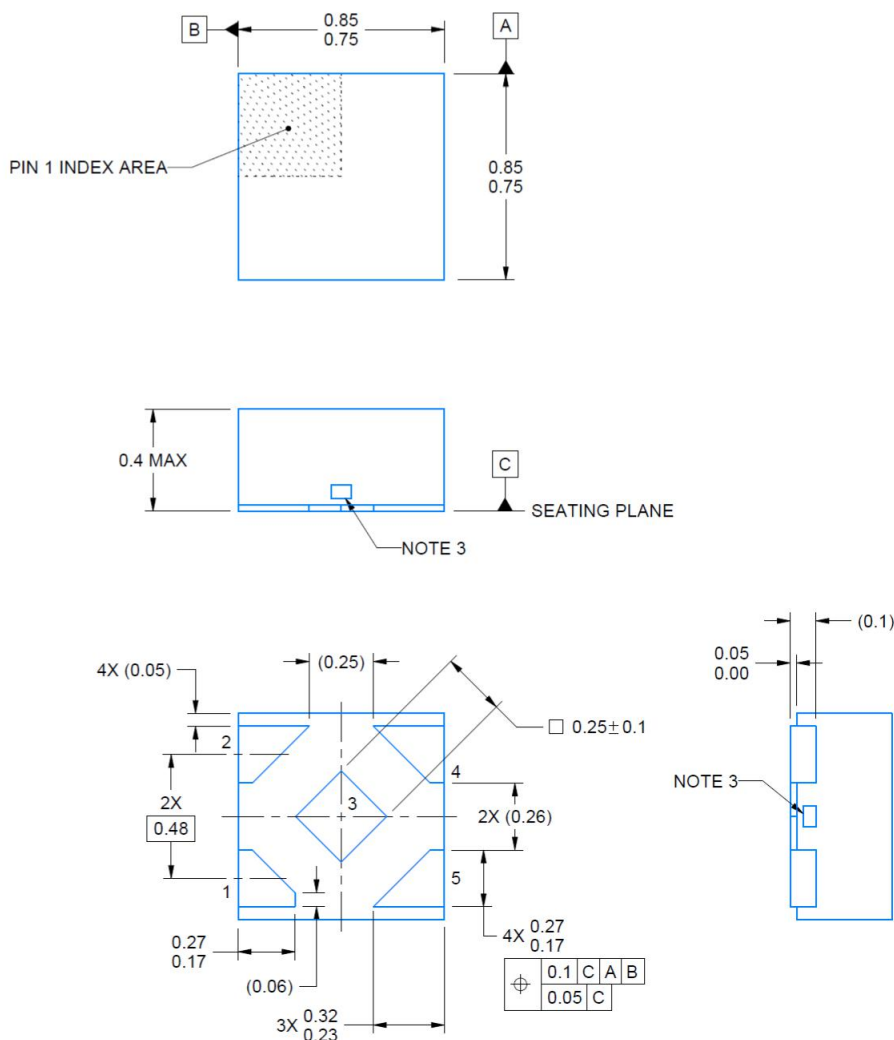
YZP (DSBGA-5)



LAND PATTERN EXAMPLE
SCALE:40X



DPW (X2SON-5)



Ordering information

Order code	Package	Baseqty	Deliverymode
SN74LVC1G08DBVR	SOT23-5	3000	Tape and reel
SN74LVC1G08DCKR	SC70-5	3000	Tape and reel
SN74LVC1G08DSFR	SON-6	5000	Tape and reel
SN74LVC1G08DRYR	SOT-886	5000	Tape and reel
SN74LVC1G08YZPR	DSBGA-5	3000	Tape and reel
SN74LVC1G08DPWR	X2SON-5	3000	Tape and reel
SN74LVC1G08DRLR	SOT-553	4000	Tape and reel

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