

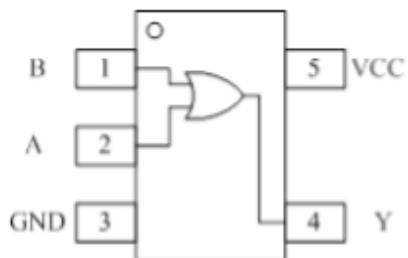
General Description

The SN74LVC1G32 is a single 2-input OR Gate in three tiny footprint packages. The device performs much as LCX multi-gate products in speed and drive.

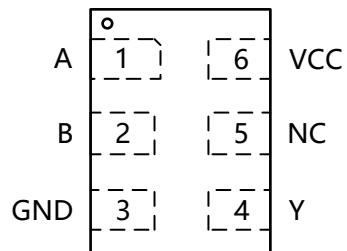
Features

- Tiny SC70-5 /SOT23-5/DFN Packages
- 2.4ns t_{PD} at 5V (typ)
- Source/Sink 24mA at 3.0V
- Over-Voltage Tolerant Inputs
- Designed for 1.65V to 5.5V V_{CC} Operation
- These Devices are Pb-Free and are RoHS Compliant

Pin Configuration



SC70-5/SOT23-5



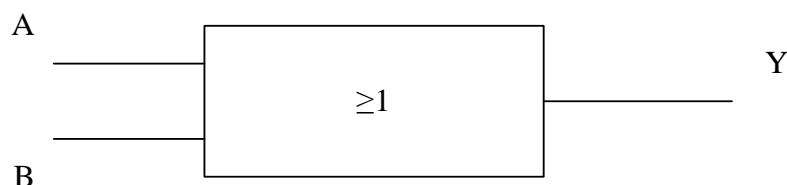
DFN6

Figure1: Top View

Pin Function

(SC70 -5/ SOT23-5 /DFN6)

PIN	FUNCTION
1	IN B
2	INA
3	GND
4	Y
5	VCC

Block Diagram**Figure2.**Logic symbol**Functional Description****Function Table**

Input		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	-0.5 to 7.0	V
V_I	DC Input Voltage	$-0.5 \leq V_I \leq +7.0$	V
V_O	DC Output Voltage Output in Higher or Low State	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current $V_I < GND$	-50	mA
I_{OK}	DC Output Diode Current $V_O < GND, V_O > V_{CC}$	-50	mA
I_O	DC Output Sink Current	-50	mA
I_{CC}	DC Supply Current per Supply Pin	± 100	mA
I_{GND}	DC Ground Current per Supply Pin	± 100	mA
T_{STG}	Storage Temperature Range	-65 to 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T_J	Junction Temperature Under Bias	150	°C
θ_{JA}	Thermal Resistance SC70-5	435	
	SOT23-5	300	°C/W
		423	
P_D	Power Dissipation in Still Air at 85°C	200	mW
MSL	Moisture Sensitivity	Level 1	
ESD	ESD Classification Human Body Model (Note 2)	2000	
	Machine Model (Note 3)	200	V
	Charged Device Model (Note 4)	N/A	
$I_{Latchup}$	Latchup Performance Above V_{CC} and Below GND at 125°C (Note 5)	± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. IO absolute maximum rating must be observed.
2. Tested to EIA/JESD22-A114-A, rated to EIA/JESD22-A114-B.
3. Tested to EIA/JESD22-A115-A, rated to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA/JESD78

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage Operating	1.65	5.5	V
	Date Retention	1.5	5.5	
V_{IN}	DC Input Voltage	0	5.5	V
V_{OUT}	DC Output Voltage (High or Low State)	0	5.5	V
T_A	Operating Temperature Range	-40	85	°C
t_r, t_f	Input Rise and Fall Time $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	0	20	
	$V_{CC} = 3.0\text{ V} \pm 0.3\text{ V}$	0	10	ns/V
	$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$	0	5	

Electrical Characteristics**DC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Condition	V _{cc} (V)	TA = 25 °C			-40 °C ≤ TA ≤ 85 °C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		1.65to1.95 2.3 to 5.5	0.75Vcc 0.7Vcc			0.75Vcc 0.7Vcc		V
V _{IL}	Low-Level Input Voltage		1.65to1.95 2.3 to 5.5			0.25Vcc 0.3Vcc		0.25Vcc 0.3Vcc	V
V _{OH}	High-Level Output Voltage V _{IN} = V _{IL}	I _{OH} = -100uA	1.65to5.5	Vcc-0.1	Vcc		Vcc-0.1		V
		I _{OH} = -3mA	1.65	1.29	1.52		1.29		
		I _{OH} = -8mA	2.3	1.9	2.1		1.9		
		I _{OH} = -12mA	2.7	2.2	2.4		2.2		
		I _{OH} = -16mA	3.0	2.4	2.7		2.4		
		I _{OH} = -24mA	3.0	2.3	2.5		2.3		
		I _{OH} = -32mA	4.5	3.8	4.0		3.8		
V _{OL}	Low-Level Output Voltage V _{IN} = V _{IH}	I _{OH} = 100uA	1.65to5.5		0.0	0.1		0.1	V
		I _{OL} = 3mA	1.65		0.08	0.24		0.24	
		I _{OL} = 8mA	2.3		0.20	0.3		0.3	
		I _{OL} = 12mA	2.7		0.22	0.4		0.4	
		I _{OL} = 16mA	3.0		0.28	0.4		0.4	
		I _{OL} = 24mA	3.0		0.38	0.55		0.55	
		I _{OL} = 32mA	4.5		0.42	0.55		0.55	
I _{IN}	Input Leakage Current	V _{IN} = 5.5V or GND	0 to 5.5		±0.1			±1.0	uA
I _{OFF}	Power Off Leakage Current	V _{IN} = 5.5V or V _{OUT} = 5.5V	0			1		10	uA
I _{CC}	Quiescent Supply Current	V _{IN} = 5.5V or GND	5.5					10	uA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

$t_r=t_f = 3\text{ns}$;

Symbol	Parameter	Condition	$V_{CC}(\text{V})$	$TA = 25^\circ\text{C}$			$-40^\circ\text{C} \leq TA \leq 85^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
t_{PD}	Propagation Delay (Figure 3 and 4)	$R_L = 1\text{M}\Omega, C_L = 15\text{ pF}$	1.65	2.0	10.1	12.9	2.0	13.9	ns
		$R_L = 1\text{M}\Omega, C_L = 15\text{ pF}$	1.8	2.0	9.1	11.6	2.0	12.4	
		$R_L = 1\text{M}\Omega, C_L = 15\text{ pF}$	2.5	0.2	6.0	7.7	0.8	8.2	
		$R_L = 1\text{M}\Omega, C_L = 15\text{ pF}$	3.3	0.8	5.0	6.5	0.5	7.0	
		$R_L = 500\Omega, C_L = 50\text{ pF}$		1.2	5.6	7.1	1.5	7.6	
		$R_L = 1\text{M}\Omega, C_L = 15\text{ pF}$	5.0	0.5	4.4	5.6	0.5	6.1	
		$R_L = 500\Omega, C_L = 50\text{ pF}$		0.8	4.8	6.1	0.8	6.6	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	$V_{CC} = 5.5\text{ V}, V_I = 0\text{ V}$ or V_{CC}	>2.5	pF
C_{PD}	Power Dissipation Capacitance (Note 6)	$10\text{MHz}, V_{CC} = 3.3\text{ V}, V_I = 0\text{ V}$ or V_{CC} $10\text{MHz}, V_{CC} = 5.5\text{ V}, V_I = 0\text{ V}$ or V_{CC}	21 21	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$I_{CC(OPR)} = C_{PD} * V_{CC} * f_{in} + I_{CC} * C_{PD}$ is used to determine the no-load dynamic power consumption;

$P_D = C_{PD} * V_{CC}^2 * f_{in} + I_{CC} * V_{CC} * f_{Fig.}$

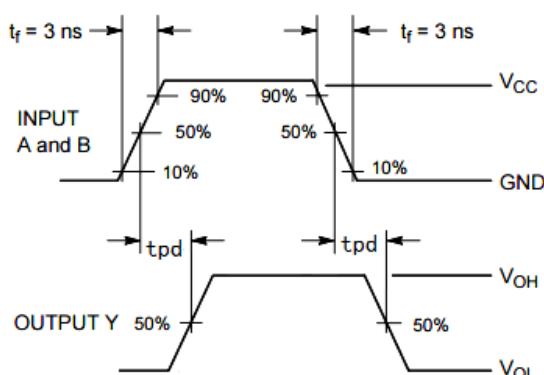


Figure 3. Switching Waveform

PROPAGATION DELAYS

$t_R = t_F = 3\text{ns}$, 10% to 90%;

$f = 1\text{ MHz}; t_W = 500\text{ ns}$

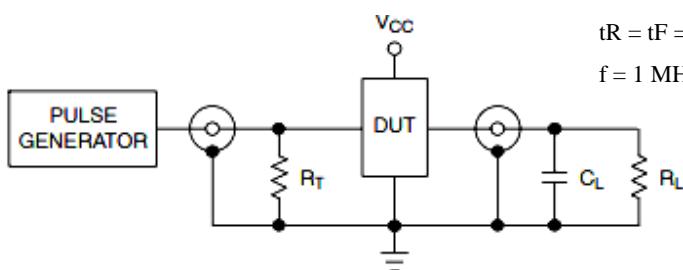
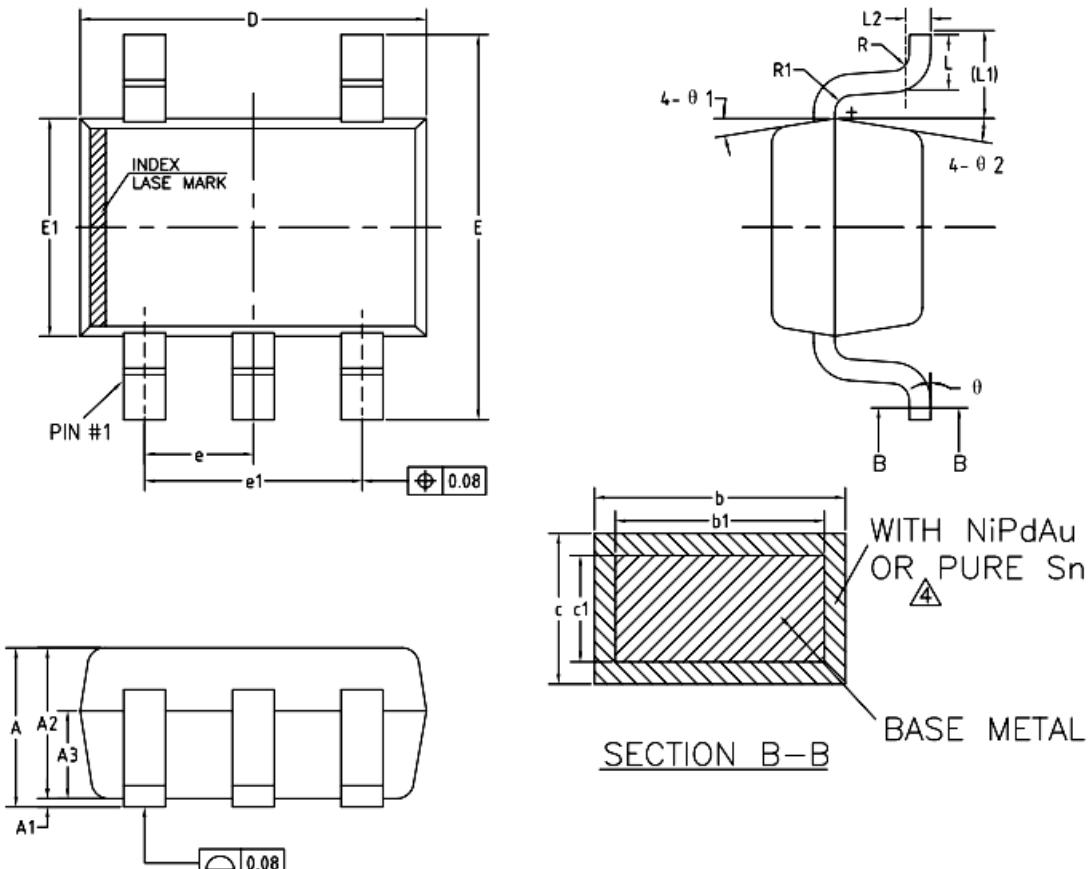


Figure 4. Test Circuit

Package Dimension

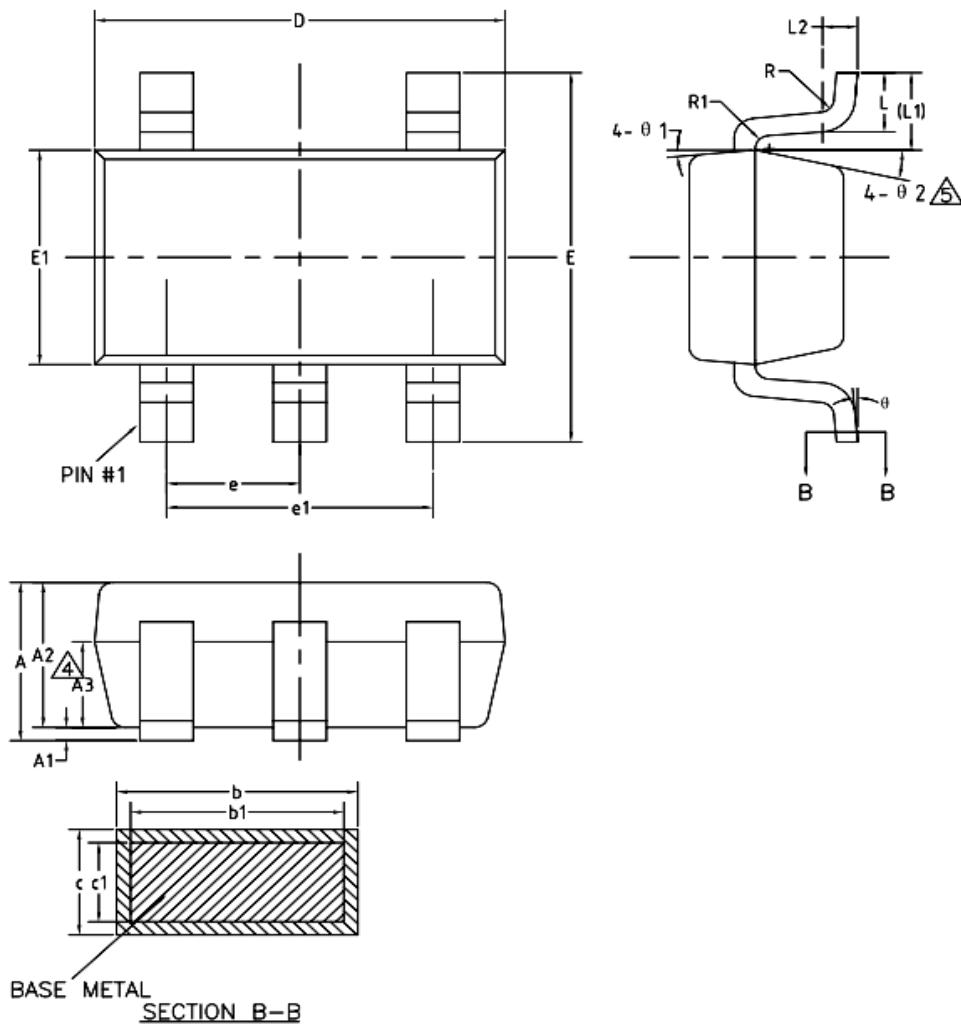
SC70-5



COMMON DIMENSIONS
 (UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX	
A	0.85	—	1.05	
A1	0	—	0.10	
A2	0.80	0.90	1.00	
A3	0.47	0.52	0.57	
b	NiPdAu PURE Sn	0.22 0.23	— —	0.29 0.33
b1	0.22	0.25	0.28	
c	NiPdAu PURE Sn	0.115 0.12	— —	0.15 0.18
c1	0.115	0.13	0.14	
D	2.02	2.07	2.12	
E	2.20	2.30	2.40	
E1	1.25	1.30	1.35	
e	0.60	0.65	0.70	
e1	1.20	1.30	1.40	
L	0.28	0.33	0.38	
L1	0.50REF			
L2	0.15BSC			
R	0.10	—	—	
R1	0.10	—	0.25	
θ	0°	—	8°	
θ 1	6°	9°	12°	
θ 2	6°	9°	12°	

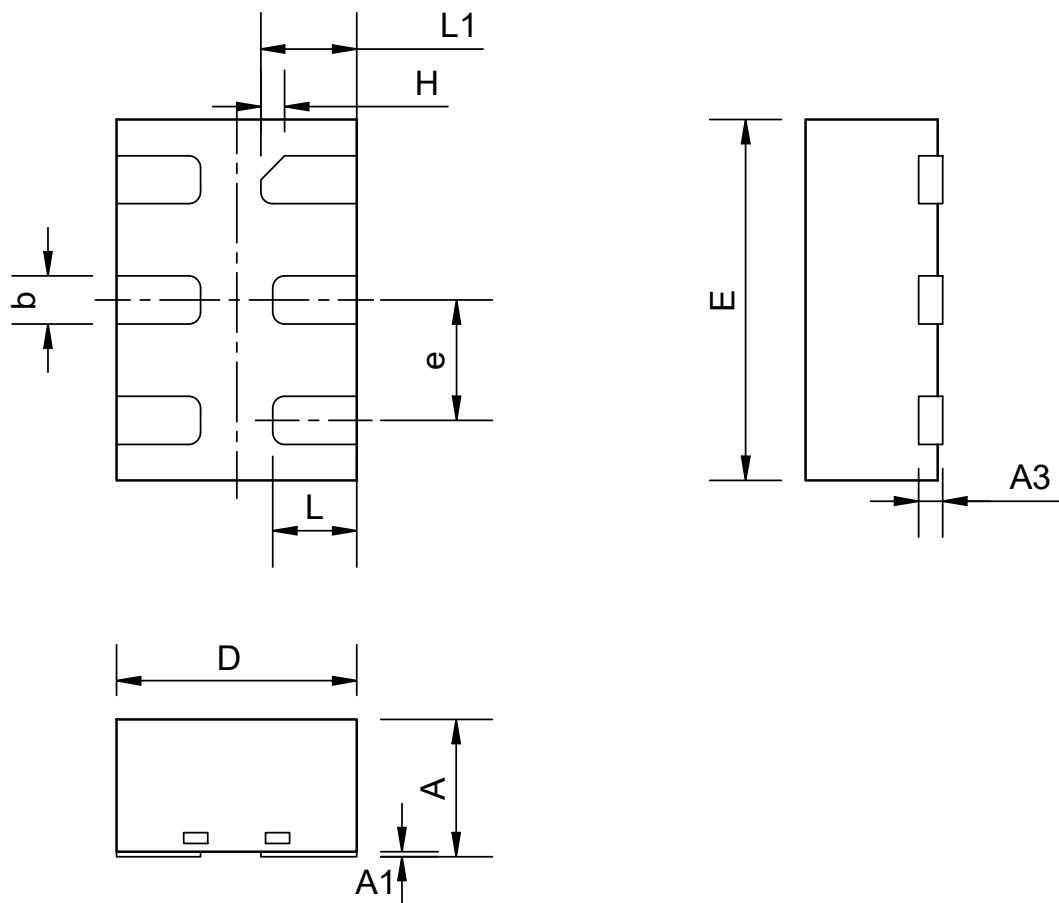
SOT23-5



COMMON DIMENSIONS
 (UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	—	—	1.25
A1	0	—	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.36	—	0.50
b1	0.36	0.38	0.45
c	0.14	—	0.20
c1	0.14	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
L	0.35	0.45	0.60
L1	0.59REF		
L2	0.25BSC		
R	0.10	—	—
R1	0.10	—	0.25
θ	0°	—	8°
θ1	3°	5°	7°
θ2	6°	—	14°

DFN6(1.0×1.5)



COMMON DIMENSIONS

(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.50	--	0.60
A1	0	0.02	0.05
A3	0.10REF		
b	0.15	0.20	0.25
D	0.90	1.00	1.10
E	1.40	1.50	1.60
e	0.40	0.50	0.60
H	0.10REF		
L	0.30	0.35	0.40
L1	0.35	0.40	0.45

Ordering information

Order code	Marking code	Package	Baseqty	Delivery mode
UMW SN74LVC1G32DBVR	C32R	SOT23-5	3000	Tape and reel
UMW SN74LVC1G32DCKR	CG5	SC70-5	3000	Tape and reel
UMW SN74LVC1G32DRYR	CG	DFN6	5000	Tape and reel

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[NLVVHC1GT00DFT2G](#) [NLV74HC02ADTR2G](#) [NLX1G332CMUTCG](#) [NLVHCT132ADTR2G](#) [NL17SG86P5T5G](#) [NL17SZ05P5T5G](#)
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