

### Description

The TSV63x and TSV63xA series of dual and quad operational amplifiers offers low voltage operation and rail-to-rail input and output.

This family features an excellent speed/power consumption ratio, offering an 880 kHz gain-bandwidth product while consuming only 60  $\mu$ A at 5 V supply voltage.

These features make the TSV63x and TSV63xA family ideal for sensor interfaces, battery-supplied and portable applications, and active filtering.

### Applications

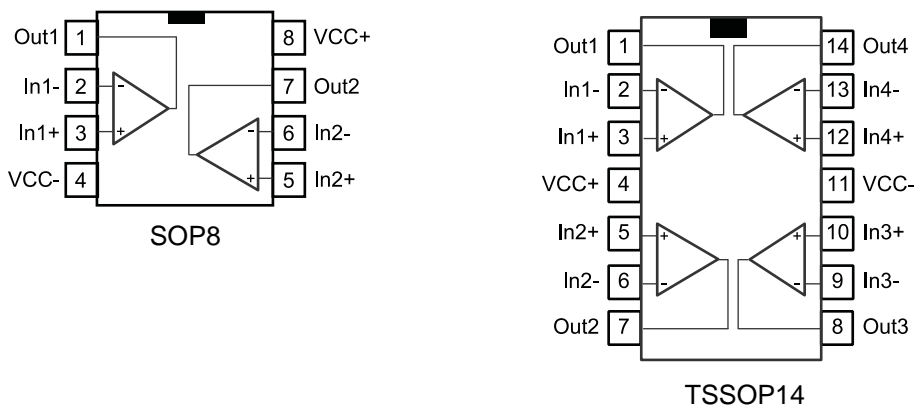
- Battery-powered applications
- Portable devices
- Signal conditioning
- Active filtering
- Medical instrumentation

### Features

- Rail-to-rail input and output
- Low power consumption: 60  $\mu$ A typ at 5 V
- Low supply voltage: 1.5 V - 5.5 V
- Gain bandwidth product: 880 kHz typ
- Unity gain stable on 100 pF capacitor
- Low power shutdown mode: 5 nA typ
- Low offset voltage: 800  $\mu$ V max (A version)
- Low input bias current: 1 pA typ
- EMI hardened op amps
- Automotive qualification

### Package pin connections

Figure 1: Pin connections for each package (top view)



### Absolute maximum ratings and operating conditions

Table 2: Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit	
$V_{CC}$	Supply voltage	6	V	
$V_{id}$	Differential input voltage	$\pm V_{CC}$		
$V_{in}$	Input voltage	$(V_{CC-}) - 0.2$ to $(V_{CC+}) + 0.2$		
$I_{in}$	Input current	10	mA	
$\overline{SHDN}$ SHDN	Shutdown voltage	$(V_{CC-}) - 0.2$ to $(V_{CC+}) + 0.2$	V	
$T_{stg}$	Storage temperature	-65 to 150	$^{\circ}$ C	
$R_{thja}$	Thermal resistance junction to ambient	SOP8	125	$^{\circ}$ C/W
		TSSOP14	100	
$T_j$	Maximum junction temperature	150	$^{\circ}$ C	
ESD	HBM: human body model	4000	V	
	MM: machine model	300		
	CDM: charged device model	1500		
	Latch-up immunity	200	mA	

**Notes:**

- (1) All voltage values, except the differential voltage are with respect to the network ground terminal.
- (2) Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
- (3)  $V_{CC} - V_{IN}$  must not exceed 6 V,  $V_{IN}$  must not exceed 6 V.
- (4) Input current must be limited by a resistor in series with the inputs
- (5)  $R_{th}$  are typical values
- (6) Short-circuits can cause excessive heating and destructive dissipation
- (7) Human body model: 100 pF discharged through a 1.5 k $\Omega$  resistor between two pins of the device, done for all couples of pin combinations with other pins floating.
- (8) Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5  $\Omega$ ), done for all couples of pin combinations with other pins floating
- (9) Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to the ground.

**Table 3: Operating conditions**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply voltage	1.5 to 5.5	V
V <sub>ICM</sub>	Common-mode input voltage range	(V <sub>CC-</sub> ) - 0.1 to (V <sub>CC+</sub> ) + 0.1	
T <sub>oper</sub>	Operating free-air temperature range	-40 to 125	°C

### Electrical characteristics

**Table 4: Electrical characteristics at VCC+ = 1.8 V with VCC- = 0 V, Vicm = VCC/2, Tamb = 25° C, and RL connected to VCC/2 (unless otherwise specified)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
V <sub>io</sub>	Offset voltage	TSV63x			3	mV
		TSV63xA			0.8	
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub> - TSV63x			4.5	
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub> - TSV63xA			2	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2		$\mu$ V/°C
I <sub>io</sub>	Input offset current	(V <sub>out</sub> = V <sub>CC</sub> /2)		1	10	pA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>		1	100	
I <sub>ib</sub>	Input bias current	(V <sub>out</sub> = V <sub>CC</sub> /2)		1	10	pA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>		1	100	
CMR	Common mode rejection ratio 20 log ( $\Delta V_{ic}/\Delta V_{io}$ )	0 V to 1.8 V, V <sub>out</sub> = 0.9 V	53	74		dB
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	51			
A <sub>vd</sub>	Large signal voltage gain	R <sub>L</sub> = 10 k $\Omega$ , V <sub>out</sub> = 0.5 V to 1.3 V	85	95		dB
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	80			
V <sub>OH</sub>	High level output voltage, (V <sub>OH</sub> = V <sub>CC</sub> - V <sub>out</sub> )	R <sub>L</sub> = 10 k $\Omega$		5	35	mV
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			50	
V <sub>OL</sub>	Low level output voltage	R <sub>L</sub> = 10 k $\Omega$		4	35	mV
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			50	
I <sub>out</sub>	I <sub>sink</sub>	V <sub>o</sub> = 1.8 V	6	12		mA
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	4			
	I <sub>source</sub>	V <sub>o</sub> = 0 V	6	10		
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>	4			
I <sub>CC</sub>	Supply current (per channel)	No load, V <sub>out</sub> = V <sub>CC</sub> /2	40	50	60	$\mu$ A
		T <sub>min</sub> < T <sub>op</sub> < T <sub>max</sub>			62	
<b>AC performance</b>						
GBP	Gain bandwidth product	R <sub>L</sub> = 2 k $\Omega$ , C <sub>L</sub> = 100 pF, f = 100 kHz	700	790		kHz
$\phi_m$	Phase margin	R <sub>L</sub> = 2 k $\Omega$ , C <sub>L</sub> = 100 pF		45		Degrees
G <sub>m</sub>	Gain margin	R <sub>L</sub> = 2 k $\Omega$ , C <sub>L</sub> = 100 pF		13		dB
SR	Slew rate	R <sub>L</sub> = 2 k $\Omega$ , C <sub>L</sub> = 100 pF, A <sub>v</sub> = 1	0.2	0.27		V/ $\mu$ s
e <sub>n</sub>	Equivalent input noise voltage	f = 1 kHz		60		nV/ $\sqrt$ Hz
		f = 10 kHz		33		

**Table 5: Shutdown characteristics VCC = 1.8 V**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
$I_{CC}$	Supply current in shutdown mode (all channels)	$\overline{\text{SHDN}} = V_{CC-}$		2.5	50	nA
		$T_{\min} < T_{op} < 85^{\circ} \text{C}$			200	
		$T_{\min} < T_{op} < 125^{\circ} \text{C}$			1.5	$\mu\text{A}$
$t_{on}$	Amplifier turn-on time	$R_L = 2 \text{ k}\Omega$ , $V_{out} = (V_{CC-})$ to $(V_{CC-}) + 0.2 \text{ V}$		200		ns
$t_{off}$	Amplifier turn-off time	$R_L = 2 \text{ k}\Omega$ , $V_{out} = (V_{CC+}) - 0.5 \text{ V}$ to $(V_{CC+}) - 0.7 \text{ V}$		20		
$V_{IH}$	$\overline{\text{SHDN}}$ logic high		1.35			V
$V_{IL}$	$\overline{\text{SHDN}}$ logic low				0.6	
$I_{IH}$	$\overline{\text{SHDN}}$ current high	$\overline{\text{SHDN}} = V_{CC+}$		10		pA
$I_{IL}$	$\overline{\text{SHDN}}$ current low	$\overline{\text{SHDN}} = V_{CC-}$		10		
$I_{OLeak}$	Output leakage in shutdown mode	$\overline{\text{SHDN}} = V_{CC-}$		50		
		$T_{\min} < T_{op} < 125^{\circ} \text{C}$		1		nA

## Dual and quad, rail-to-rail input/output, 60 $\mu$ A, 880 kHz operational amplifiers

**Table 6:  $V_{CC+} = 3.3$  V,  $V_{CC-} = 0$  V,  $V_{icm} = V_{CC}/2$ ,  $T_{amb} = 25^\circ$  C,  $R_L$  connected to  $V_{CC}/2$  (unless otherwise specified)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
$V_{io}$	Offset voltage	TSV63x			3	mV
		TSV63xA			0.8	
		$T_{min} < T_{op} < T_{max}$ - TSV63x			4.5	
		$T_{min} < T_{op} < T_{max}$ - TSV63xA			2	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2		$\mu$ V/ $^\circ$ C
$I_{io}$	Input offset current	$V_{out} = V_{CC}/2$		1	10 <sup>(1)</sup>	pA
		$T_{min} < T_{op} < T_{max}$		1	100	
$I_{ib}$	Input bias current	$V_{out} = V_{CC}/2$		1	10 <sup>(1)</sup>	pA
		$T_{min} < T_{op} < T_{max}$		1	100	
CMR	Common mode rejection ratio $20 \log (\Delta V_{ic}/\Delta V_{io})$	0 V to 3.3 V, $V_{out} = 1.65$ V	57	79		dB
		$T_{min} < T_{op} < T_{max}$	53			
$A_{vd}$	Large signal voltage gain	$R_L = 10$ k $\Omega$ , $V_{out} = 0.5$ V to 2.8 V	88	98		dB
		$T_{min} < T_{op} < T_{max}$	83			
$V_{OH}$	High level output voltage, ( $V_{OH} = V_{CC} - V_{out}$ )	$R_L = 10$ k $\Omega$		5	35	mV
		$T_{min} < T_{op} < T_{max}$			50	
$V_{OL}$	Low level output voltage	$R_L = 10$ k $\Omega$		4	35	mV
		$T_{min} < T_{op} < T_{max}$			50	
$I_{out}$	$I_{sink}$	$V_o = 3.3$ V	23	45		mA
		$T_{min} < T_{op} < T_{max}$	20			
	$I_{source}$	$V_o = 0$ V	23	38		
		$T_{min} < T_{op} < T_{max}$	20			
$I_{CC}$	Supply current, (per channel)	No load, $V_{out} = 1.75$ V	43	55	64	$\mu$ A
		$T_{min} < T_{op} < T_{max}$			66	
<b>AC performance</b>						
GBP	Gain bandwidth product	$R_L = 2$ k $\Omega$ , $C_L = 100$ pF, $f = 100$ kHz	710	860		kHz
$\phi_m$	Phase margin	$R_L = 2$ k $\Omega$ , $C_L = 100$ pF		46		Degrees
$G_m$	Gain margin	$R_L = 2$ k $\Omega$ , $C_L = 100$ pF		13		dB
SR	Slew rate	$R_L = 2$ k $\Omega$ , $C_L = 100$ pF, $A_V = 1$	0.22	0.29		V/ $\mu$ s

## Dual and quad, rail-to-rail input/output, 60 $\mu$ A, 880 kHz operational amplifiers

Table 7: Electrical characteristics at  $V_{CC+} = 5$  V with  $V_{CC-} = 0$  V,  $V_{icm} = V_{CC}/2$ ,  $T_{amb} = 25^\circ$  C, and  $R_L$  connected to  $V_{CC}/2$  (unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>DC performance</b>						
$V_{io}$	Offset voltages	TSV63x			3	mV
		TSV63xA			0.8	
		$T_{min} < T_{op} < T_{max}$ - TSV63x			4.5	
		$T_{min} < T_{op} < T_{max}$ - TSV63xA			2	
$\Delta V_{io}/\Delta T$	Input offset voltage drift			2		$\mu$ V/ $^\circ$ C
$I_{io}$	Input offset current	$(V_{out} = V_{CC}/2)$		1	10 <sup>(1)</sup>	pA
		$T_{min} < T_{op} < T_{max}$		1	100	
$I_{ib}$	Input bias current	$(V_{out} = V_{CC}/2)$		1	10 <sup>(1)</sup>	pA
		$T_{min} < T_{op} < T_{max}$		1	100	
CMR	Common mode rejection ratio 20 log ( $\Delta V_{ic}/\Delta V_{io}$ )	0 V to 5 V, $V_{out} = 2.5$ V	60	80		dB
		$T_{min} < T_{op} < T_{max}$	55			
SVR	Supply voltage rejection ratio 20 log ( $\Delta V_{CC}/\Delta V_{io}$ )	$V_{CC} = 1.8$ to 5 V	75	102		dB
		$T_{min} < T_{op} < T_{max}$	73			
$A_{vd}$	Large signal voltage gain	$R_L = 10$ k $\Omega$ , $V_{out} = 0.5$ V to 4.5 V	89	98		dB
		$T_{min} < T_{op} < T_{max}$	84			
EMIRR	EMI rejection ratio, EMIRR = -20 log ( $V_{RFpeak}/\Delta V_{io}$ )	$V_{RF} = 100$ mV <sub>rms</sub> , $f = 400$ MHz		61		dB
		$V_{RF} = 100$ mV <sub>rms</sub> , $f = 900$ MHz		85		
		$V_{RF} = 100$ mV <sub>rms</sub> , $f = 1800$ MHz		92		
		$V_{RF} = 100$ mV <sub>rms</sub> , $f = 2400$ MHz		83		
$V_{OH}$	High level output voltage, ( $V_{OH} = V_{CC} - V_{out}$ )	$R_L = 10$ k $\Omega$		7	35	mV
		$T_{min} < T_{op} < T_{max}$			50	
$V_{OL}$	Low level output voltage	$R_L = 10$ k $\Omega$		6	35	mV
		$T_{min} < T_{op} < T_{max}$			50	
$I_{out}$	$I_{sink}$	$V_o = 5$ V	40	69		mA
		$T_{min} < T_{op} < T_{max}$	35			
	$I_{source}$	$V_o = 0$ V	40	74		
		$T_{min} < T_{op} < T_{max}$	35			
$I_{CC}$	Supply current, (per channel)	No load, $V_{out} = V_{CC}/2$	50	60	69	$\mu$ A
		$T_{min} < T_{op} < T_{max}$			72	
<b>AC performance</b>						
GBP	Gain bandwidth product	$R_L = 2$ k $\Omega$ , $C_L = 100$ pF, $f = 100$ kHz	730	880		kHz
$F_u$	Unity gain frequency	$R_L = 2$ k $\Omega$ , $C_L = 100$ pF		830		
$\phi_m$	Phase margin	$R_L = 2$ k $\Omega$ , $C_L = 100$ pF		48		Degrees





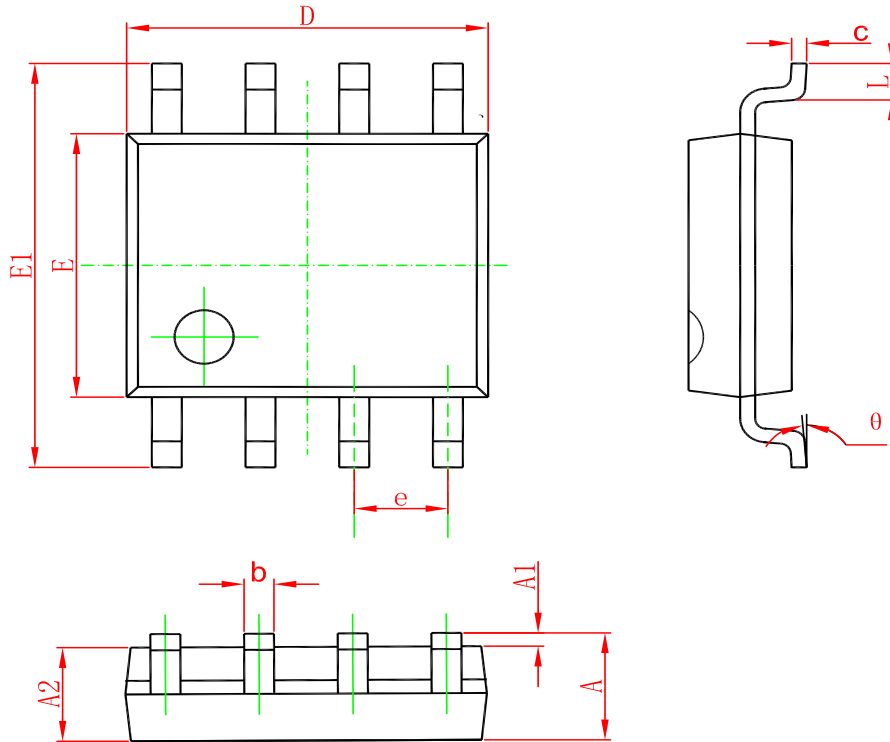


## Electrical characteristics



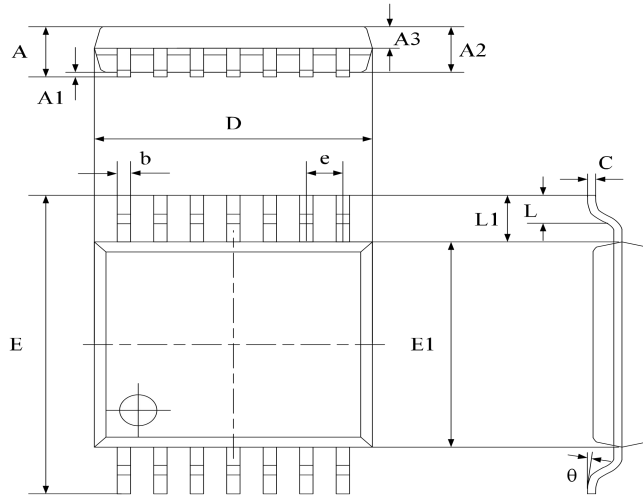
Package Dimension

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
theta	0°	8°	0°	8°

TSSOP-14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	-	1.200	-	0.0472
A1	0.050	0.150	0.002	0.006
A2	0.900	1.050	0.037	0.043
A3	0.390	0.490	0.016	0.020
b	0.200	0.290	0.008	0.012
C	0.130	0.180	0.005	0.007
D	4.860	5.060	0.198	0.207
E	6.200	6.600	0.253	0.269
E1	4.300	4.500	0.176	0.184
e	0.650 typ.		0.0256 typ.	
L1	1.000 ref.		0.0393 ref.	
L	0.450	0.750	0.018	0.031
$\theta$	0°	8°	0°	8°

Ordering information

Order code	Package	Baseqty	Deliverymode	Marking
UMW TSV632IDT	SOP-8	2500	Tape and reel	TSV632
UMW TSV632AIDT	SOP-8	2500	Tape and reel	TSV632A
UMW TSV634IPT	TSSOP-14	4000	Tape and reel	TSV634

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