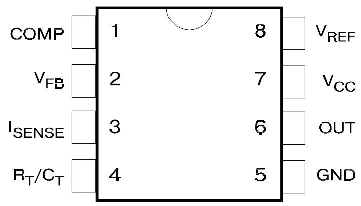
Description

The 2842/43/44/45 are fixed frequency current mode PWM controller. They are specially designed for OFF−Line and DC to DC converter applications with a minimal external components. Internally implemented circuits include a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totempole output ideally suited for driving a power MOSFET. Protection circuitry includes built undervoltage lockout and current limiting. The 2842 and 2844 have UVLO thresholds of 16 V (on) and 10 V (off). The corresponding thresholds for the 2843/45 are 8.4V (on) and 7.6V (off). The 2842 and 2843 can operate within 100% duty cycle. The 2844 and 2845 can operate within 50% duty cycle.
The 284X has Start-Up Current 0.5mA (typ).

Features

- Low Start-Up and Operating Current
- High Current Totem Pole Output
- Undervoltage Lockout With Hysteresis
- Operating Frequency Up To 500KHz

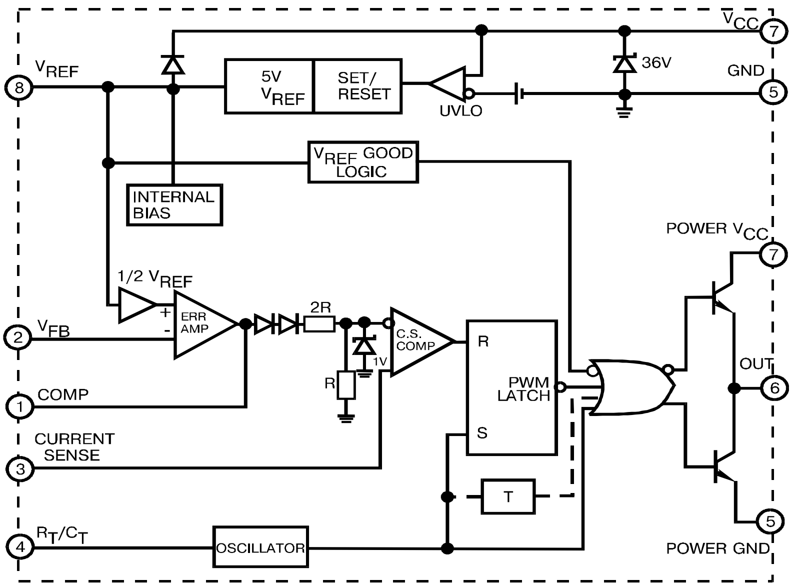
Pin Connection



Top view

Block diagram

(toggle flip flop used only in 2844, 2845)



Absolute Maximum Ratings

Symbol	Parameter	Maximum	Units
V_{CC}	Supply Voltage (low impedance source)	30	V
I_O	Output Current	±1	A
V_I	Input Voltage (Analog Inputs pins 2,3)	−0.3 to 5.5	V
$I_{SINK (E.A)}$	Error Amp Output Sink Current	10	mA
Po	Power Dissipation (T_A=25°C)	1	W
Tstg	Storage Temperature Range	-65 to150	°C
T_L	Lead Temperature (soldering 5 sec.)	260	°C
TA	Operating Ambient Temperature	-25 to +85	°C

Electrical characteristics

(*V_{CC}=15V, R_T=10kΩ, C_T=3.3nF, T_A=0°C to +70°C, unless otherwise specified)

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Units
Reference Section						
Reference Output Voltage	V_{REF}	T_J = 25°C, I_{REF} = 1 mA	4.9	5.0	5.1	V
Line Regulation	ΔV_{REF}	12V ≤ V_{CC} ≤ 25 V		6.0	20	mV
Load Regulation	ΔV_{REF}	1 mA ≤ I_{REF} ≤ 20mA		6.0	25	
Short Circuit Output Current	I_{SC}	T_A = 25°C		-100	-180	mA
Oscillator Section						
Oscillation Frequency	f	T_J = 25°C, 284X	47	50	57	KHz
		284X	47	52	57	
Frequency Change with Voltage	$\Delta f/\Delta V_{CC}$	12V ≤ V_{CC} ≤ 25 V		0.05	1.0	%
Oscillator Amplitude	$V_{(OSC)}$	(peak to peak)		1.6		V
Error Amplifier Section						
Input Bias Current	I_{BIAS}	V_{FB}=3V		-0.1	-2	μA
Input Voltage	$V_{I(E.A)}$	V_{pin1} = 2.5V	2.42	2.5	2.58	V
Open Loop Voltage Gain	A_{VOL}	2V ≤ V_0 ≤ 4V	65	90		dB
Power Supply Rejection Ratio	PSRR	12V ≤ V_{CC} ≤ 25 V	60	70		
Output Sink Current	I_{SINK}	V_{pin2} = 2.7V, V_{pin1} = 1.1V	2	7		mA
Output Source Current	I_{SOURCE}	V_{pin2} = 2.3V, V_{pin1} = 5V	-0.5	-1.0		mA
High Output Voltage	V_{OH}	V_{pin2} = 2.3V, R_L = 15KΩ to GND	5.0	6.0		V
Low Output Voltage	V_{OL}	V_{pin2} = 2.7V, R_L = 15KΩ to PIN 8		0.8	1.1	
Current Sense Section						
Gain	G_V	(Note 1 & 2)	2.85	3.0	3.15	V/V
Maximum Input Signal	$V_{I(MAX)}$	V_{pin1} = 5V (Note1)	0.9	1.0	1.1	V
Supply Voltage Rejection	SVR	12V ≤ V_{CC} ≤ 25 V (Note 1)		70		dB
Input Bias Current	I_{BIAS}	V_{pin3} = 3V		-3.0	-10	μA
Output Section						
Low Output Voltage	V_{OL}	I_{SINK} = 20 mA		0.08	0.4	V
		I_{SINK} = 200 mA		1.4	2.2	
High Output Voltage	V_{OH}	I_{SINK} = 20 mA	13	13.5		
		I_{SINK} = 200 mA	12	13.0		
Rise Time	t_R	T_J = 25°C, C_L = 1nF (Note 3)		45	150	nS
Fall Time	t_F	T_J = 25°C, C_L = 1nF (Note 3)		35	150	
Undervoltage Lockout Section						
Start Theshold	$V_{TH(ST)}$	2842/44	14.5	16.0	17.5	V
		2843/45	7.8	8.4	9.0	
Min. Operating Voltage (After Turn On)	$V_{OPR(min)}$	2842/44	8.5	10	11.5	V
		2843/45	7.0	7.6	8.2	
PWM Section						
Max. Duty Cycle	$D_{(MAX)}$	2842/43	95	97	100	%
		2844/45	47	48	50	
Min. Duty Cycle	$D_{(MAX)}$				0	
Total Standby Current						
Start-Up Current	I_{ST}	284X		0.05		mA
Operating Supply Current	$I_{CC\ (OPR)}$	V_{pin3} = V_{pin2}= 0V		13	17	
Zener Voltage	V_Z	I_{CC}=25 mA	30	38		V

* - Adjust V_{CC} above the start threshold before setting it to 15V.
Note 1: Parameter measured at trip point of latch with V_{pin2}=0.
Note 2: Gain defined as $A=\Delta V_{pin1}/\Delta V_{pin3}$; $0 \le V_{pin3} \le 0.8V$.
Note 3: These parameters, although guaranteed, are not 100% tested in production.

Pin functions

N	Function	Description
1	COMP	This pin is the Error Amplifier output and is made for loop compensation.
2	V_{FB}	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	I_{SENSE}	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R_T/C_T	The oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground.
5	GROUND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sink by this pin.
7	V_{CC}	This pin is the positive supply of the integrated circuit.
8	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.

Application information

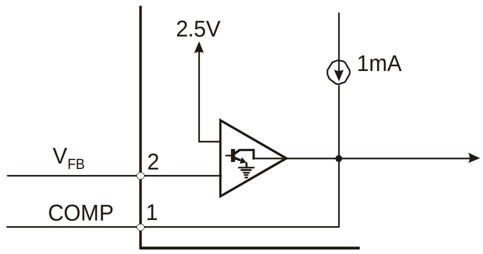


Figure 1. Error Amp Configuration

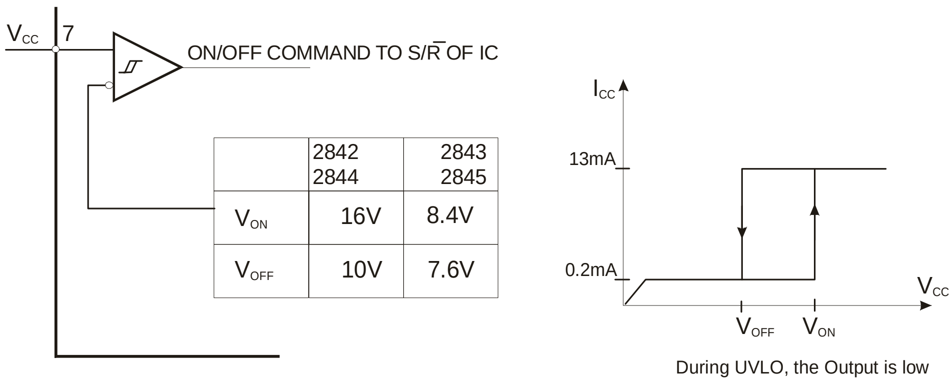
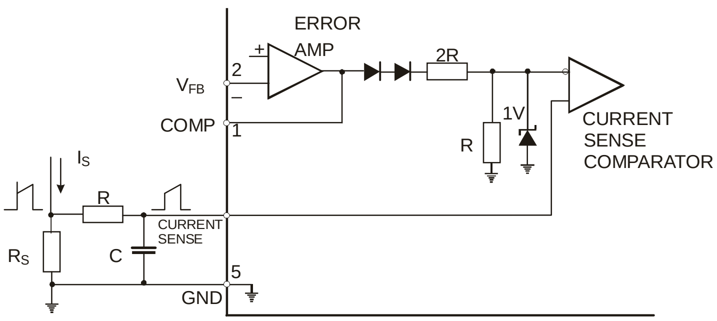


Figure 2. Undervoltage Lockout



Peak current is determined by $I_{S\,max} \approx \frac{1.0V}{R_S}$

Figure 3. Current Sense Circuit

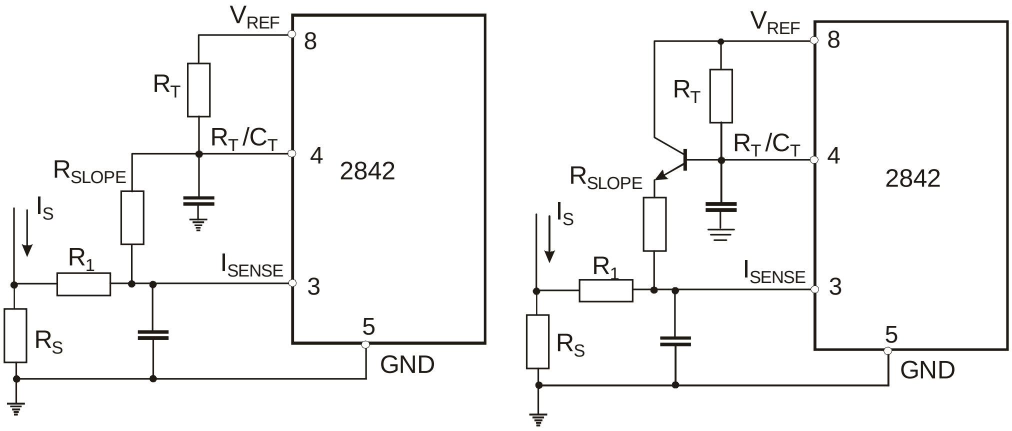
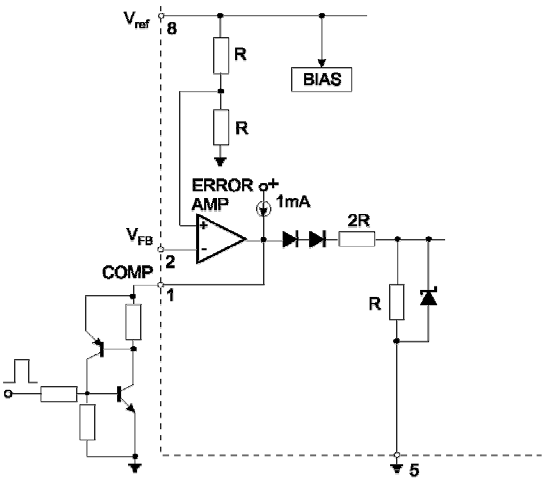
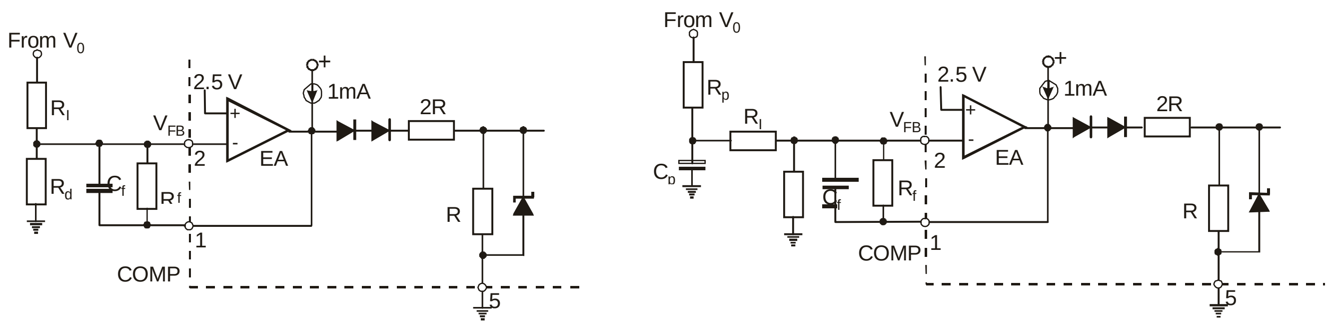


Figure 4. Slope Compensation Techniques



SCR must be selected for a holding current of less than 0.5mA.
The simple two transistor circuit can be used in place of the SCR as shown.

Figure 5. Latched Shutdown



Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.

Error Amp compensation circuit for stabilizing current-mode boost and flyback topologies operating with continuous inductor current.

Figure 6. Error Amplifier Compensation

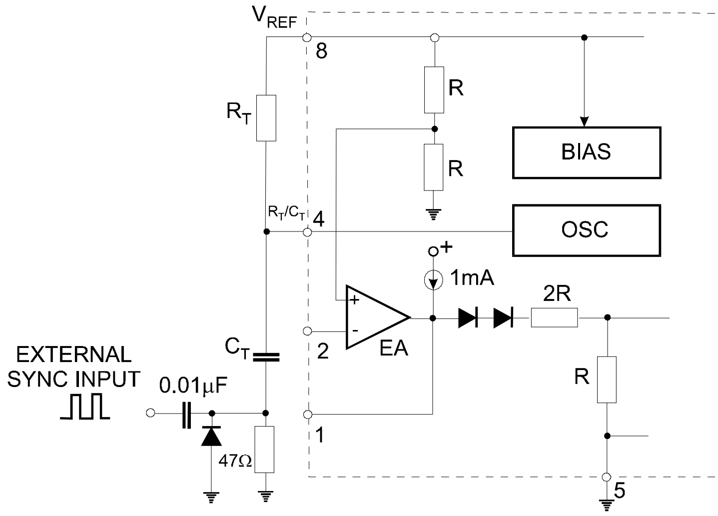


Figure 7. External Clock Synchronization

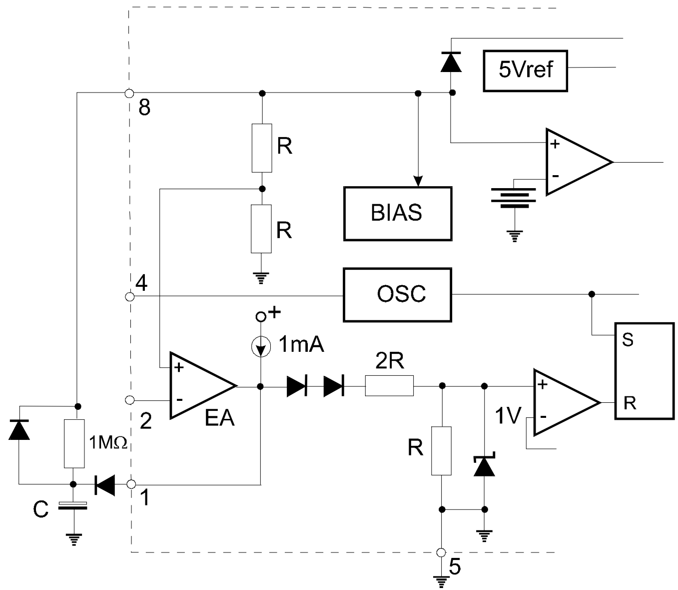


Figure 8. Soft-Start Circuit

Typical Performance Characteristics

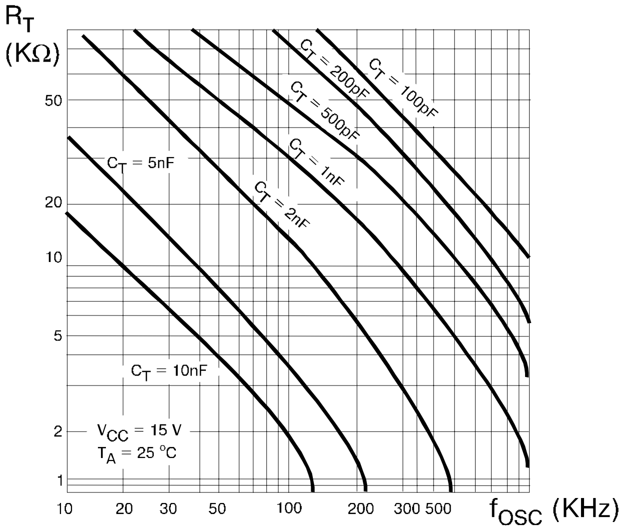


Figure 1. Timing Resistor vs. Oscillator Frequency

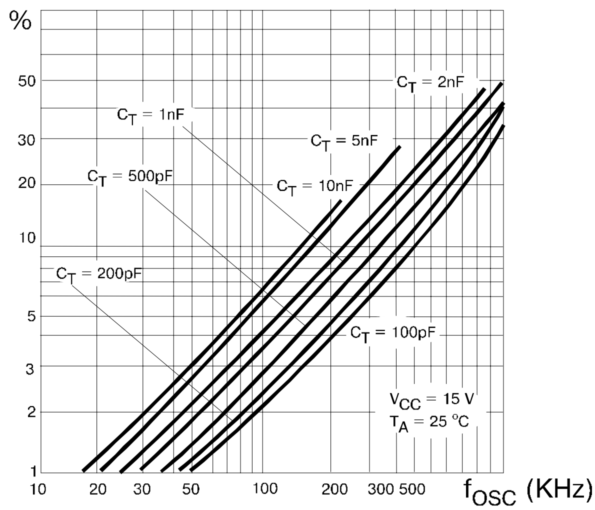


Figure 2. Output Dead-Time vs. Oscillator Frequency

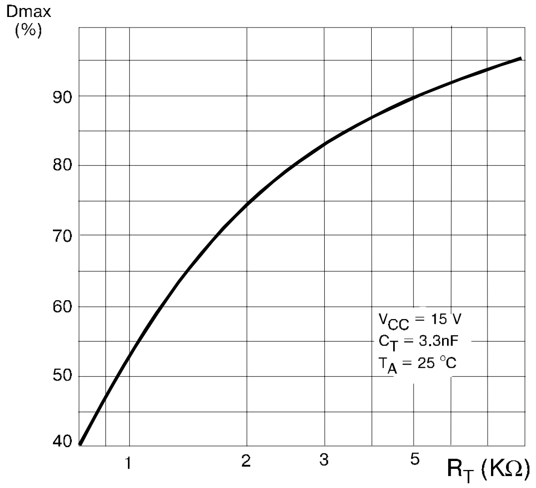


Figure 3. Maximum Output Duty Cycle vs. Timing Resistor (UC3842/43)

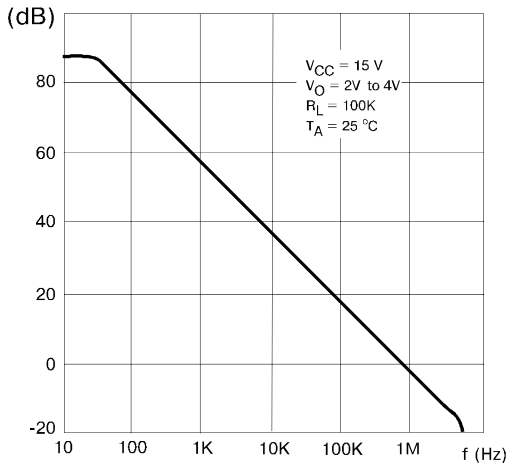


Figure 4. Error Amp Open-Loop Gain vs. Frequency

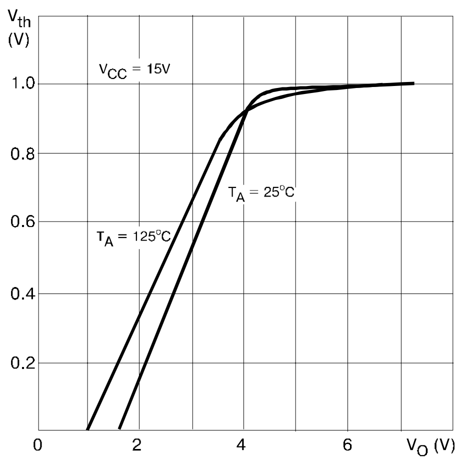


Figure 5. Current Sense Input Threshold vs. Error Amp Output Voltage

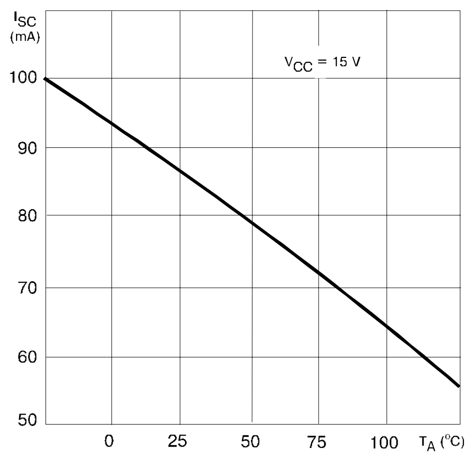


Figure 6. Reference Short Circuit Current vs. Temperature

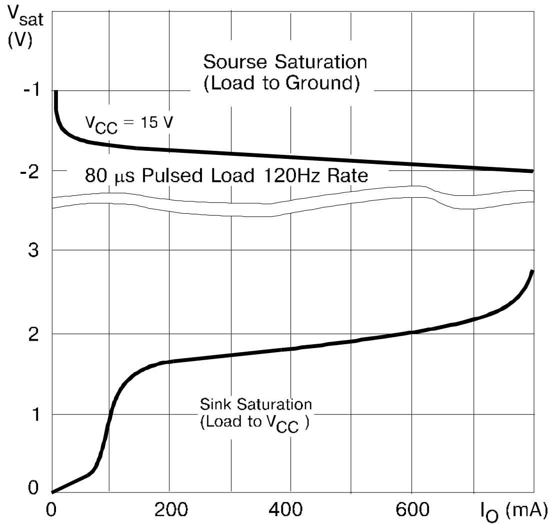


Figure 7. Output Saturation Voltage vs. Load Current
$T_A = 25°C$

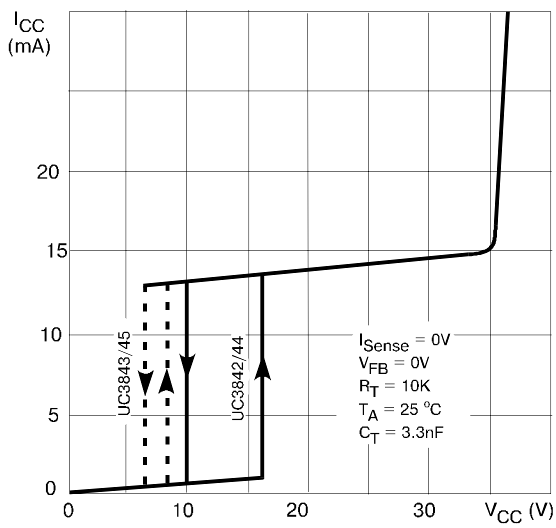


Figure 8. Supply Current vs. Supply Voltage

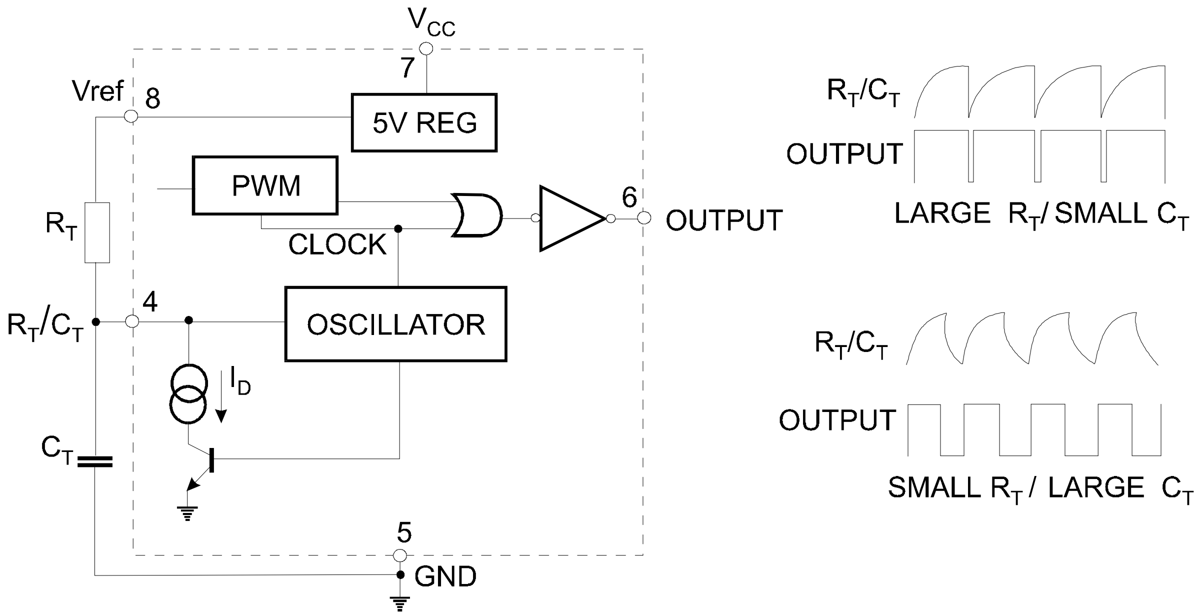


Figure 9. Oscillator and Output Waveforms

Ordering information