I²C-Compatible (2-wire) Serial EEPROM

2K bits

DATASHEET

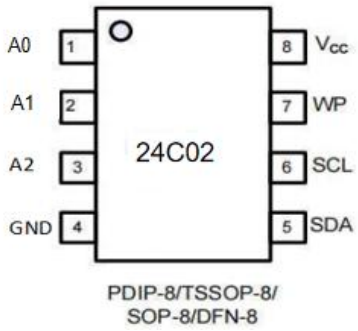
Features

- Compatible with all I²C bidirectional data transfer protocol
- Memory array:
  - 2K bits of EEPROM
  - Page size: 8 bytes
- Single supply voltage and high speed
  - Minimum operating voltage down to 1.6V
  - 1 MHz clock from 2.5V to 5.5V
  - 400kHz clock from 1.7V to 5.5V
- Random and sequential Read modes
- Write:
  - Page Write within 5 ms
  - Partial Page Writes Allowed
- Write Protect Pin for Hardware Data Protection
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- Enhanced ESD/Latch-up protection
  - HBM 4000V
  - +/- 200mA
- 8-lead SOP8-150 / TSSOP8 / SOT23-5 /SOT23-6 packages

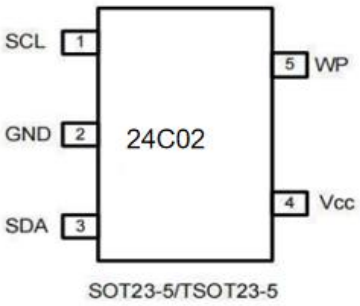
Description

- The ZD24C02B provides 2048 bits of serial electrically erasable and programmable read- only memory (EEPROM), organized as 256 words of 8 bits each.
- The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential.

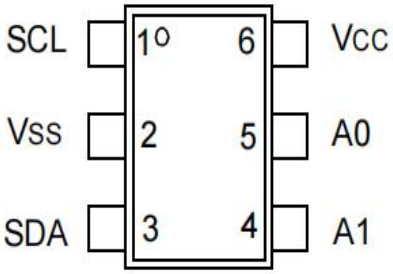
1. Pin Descriptions and Pinouts



PDIP-8/TSSOP-8/
SOP-8/DFN-8



SOT23-5/TSOT23-5



SOT23-6L

Table 1-1.Pin Descriptions

Name	Type	Description
A0/A1/A2	Input	Slave Address Setting
Vss	Ground	Ground
SDA	I/O	Serial Data Input and Serial Data Output
SCL	Input	Serial Clock Input
WP	Input	Write Control, Low Enable Write
VCC	Power	Power

Serial Clock (SCL): The SCL input is used to positive-edge clock data in and negative-edge clock data out of each device.

Serial Data (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

Device Addresses (A2, A1, A0): The A2, A1 and A0 pins are device address inputs. Typically, the A2, A1 and A0 pins are for hardware addressing and a total of 8 devices can be connected on a single bus system. If these pins are left floating, the A2, A1 and A0 pins will be internally pulled down to Vss.

Write Control (WP): The Write Control input, when WP is connected directly to VCC, all write operations to the memory are inhibited. When connected to Vss, allows normal write operations. If the pin is left floating, the WP pin will be internally pulled down to Vss. As shown in the following table1.

WP Pin Status	ZD24C02B
At VCC	Full(2K)Array
At GND	Normal Read/Write perations

Table1

2. Device Block Diagram and System Configuration

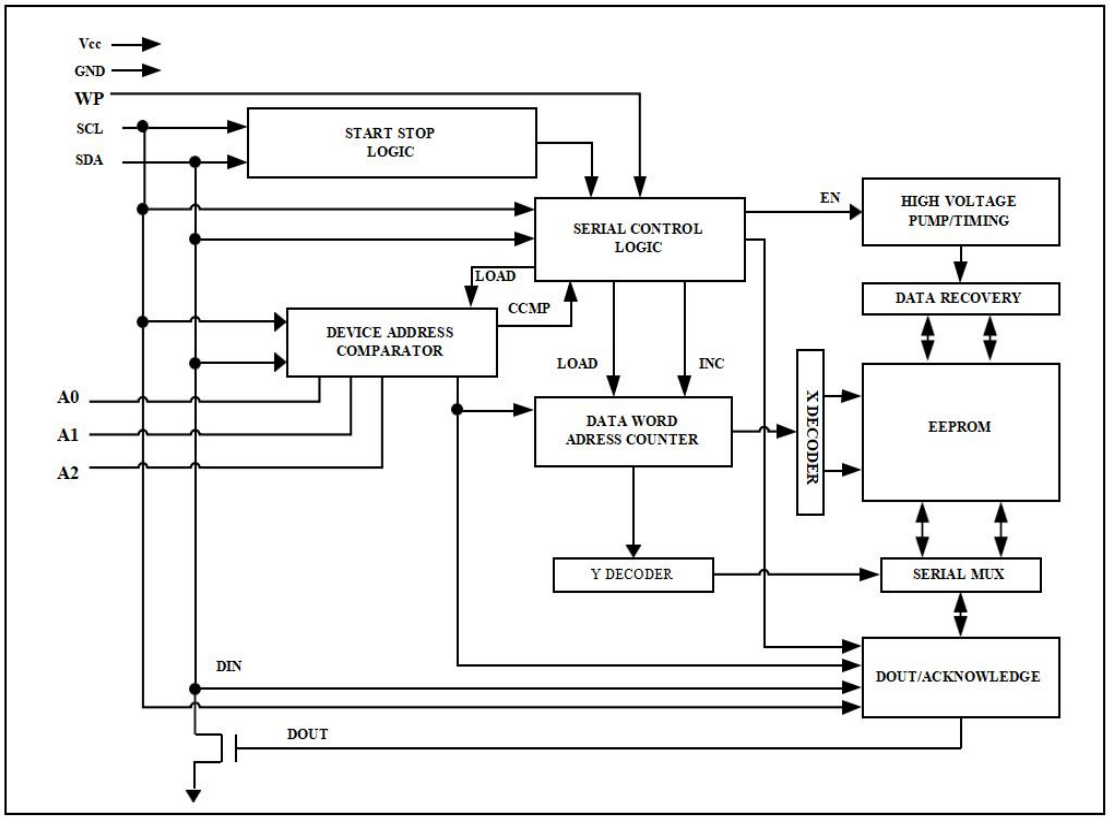


Figure 2-2.System Configuration Using 2-Wire Serial EEPROM

3. Functional Description

1.Memory Organization

ZD24C02B, 2K SERIAL EEPROM: Internally organized with 32 pages of 8 bytes each, the 2K requires a 8-bit data word address for random word addressing.

2.Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see **Figure 2**). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see **Figure 3**).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see **Figure 3**).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.(see **Figure 4**).

STANDBY MODE: The ZD24C02B features a low-power standby mode which is enabled:

1. After a fresh power up.

2. After receiving a STOP bit in read mode.

3. After completing a self-time internal programming operation.

MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

1.Clock up to 9 cycles.

2.Look for SDA high in each cycle while SCL is high.

3.Create a start condition.

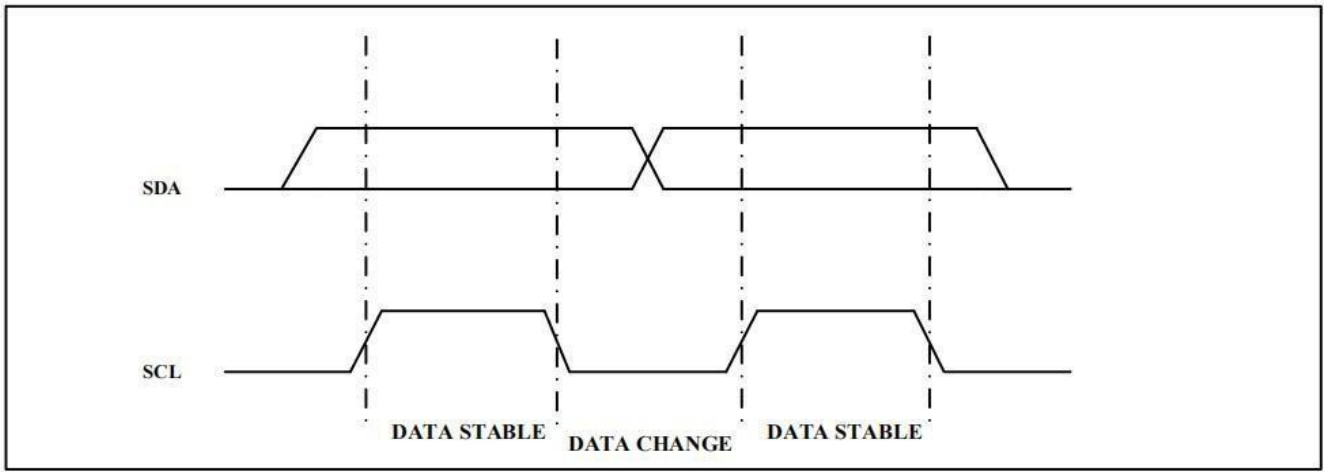


Figure 2. Data Validity

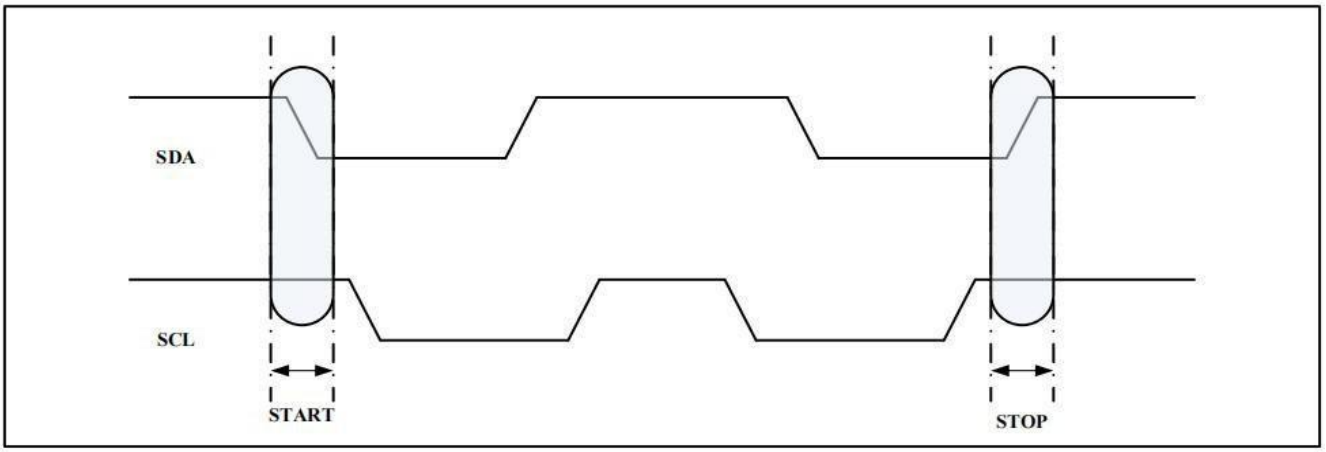


Figure 3. Start and Stop Definition

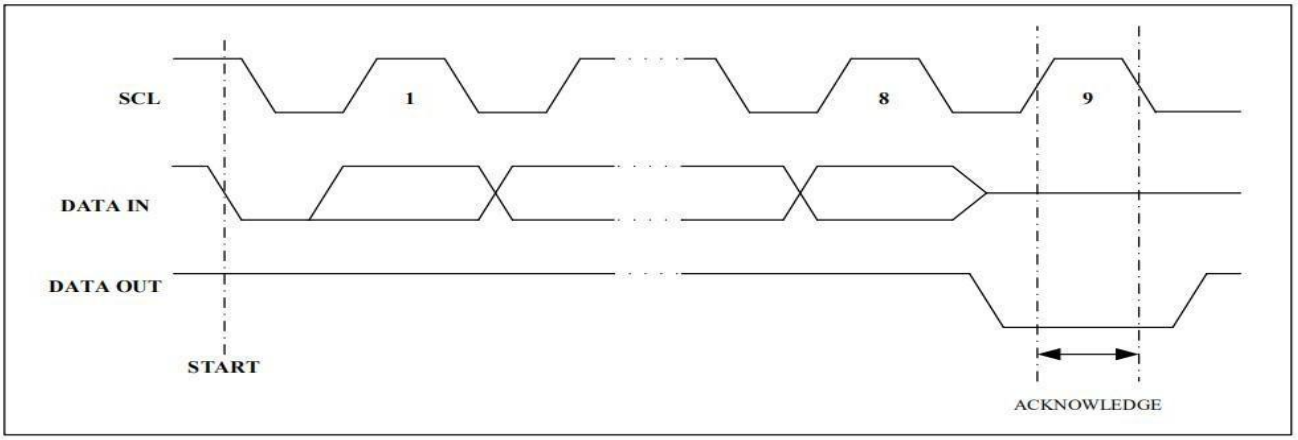


Figure 4. Output Acknowledge

4. Device Addressing

The 2K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Table 4-1)

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices..

These page addressing bits on the 2K devices should be considered the most significant bits of the data word address which follows.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.

Table 4-1. Device Address

	MSB							LSB
Access area	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Normal Area	1	0	1	0	A2	A1	A0	R/W

Table 4-2. Word Address

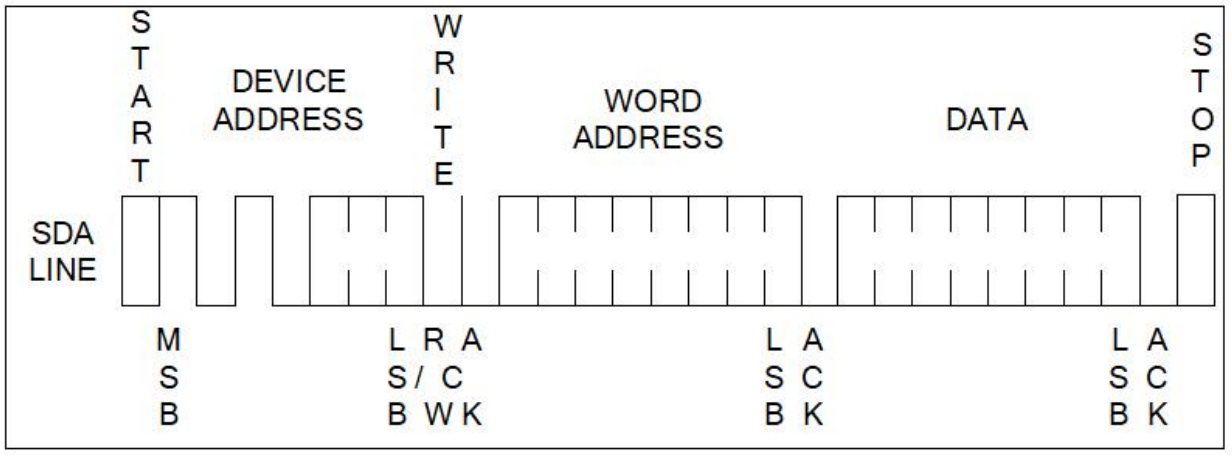
Data	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Normal Area	A7	A6	A5	A4	A3	A2	A1	A0

5. Write Operations

5.1 Byte Write

A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, tWR, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 5-1)

Figure 5-1

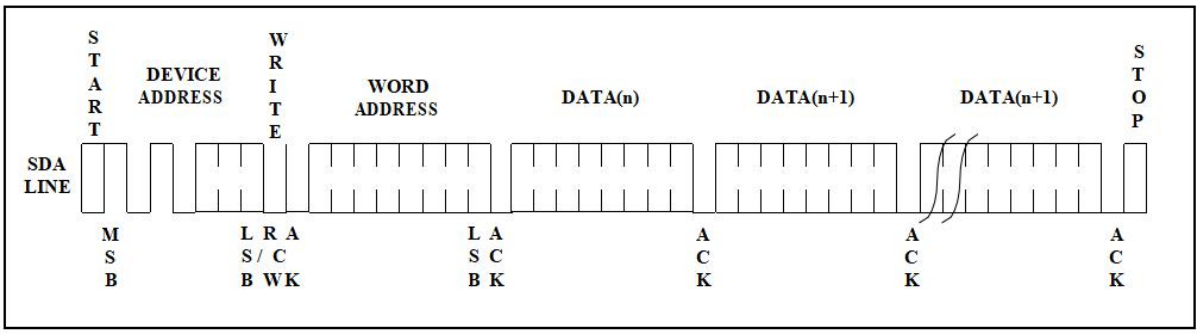


5.2 Page Write

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit more data words. The EEPROM will respond with a "0" after each data word received. The microcontroller must terminate the page write sequence with a stop condition (**see Figure 5-2**).

The lower three bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight data words are transmitted to the ZD24C02B, the data word address will roll-over, and previous data will be overwritten. The address roll-over during write is from the last byte of the current page to the first byte of the same page.

Figure 5-2



5.3 Acknowledge Polling

Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

6. Read Operations

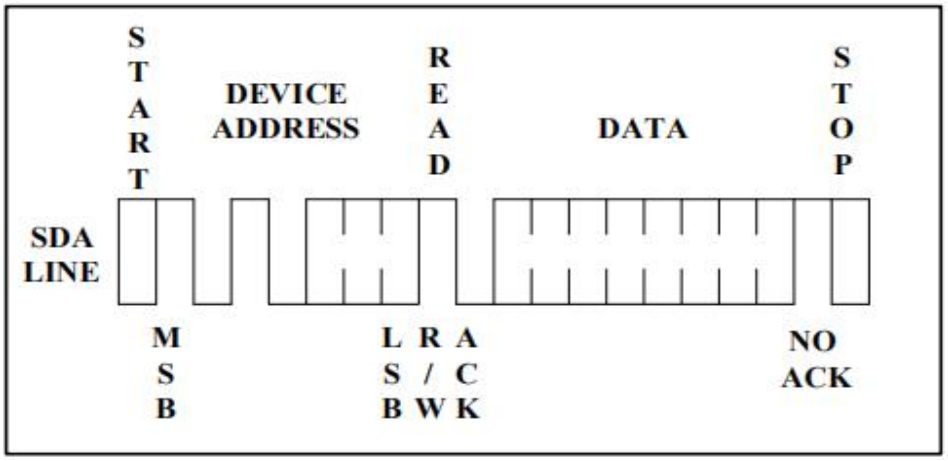
Read operations are initiated the same way as Write operations with the exception that the Read/Write Select bit in the Device Address word must be a Logic 1. There are three Read operations:

- Current Address Read
- Random Address Read
- Sequential Read

6.1 Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 6-1).

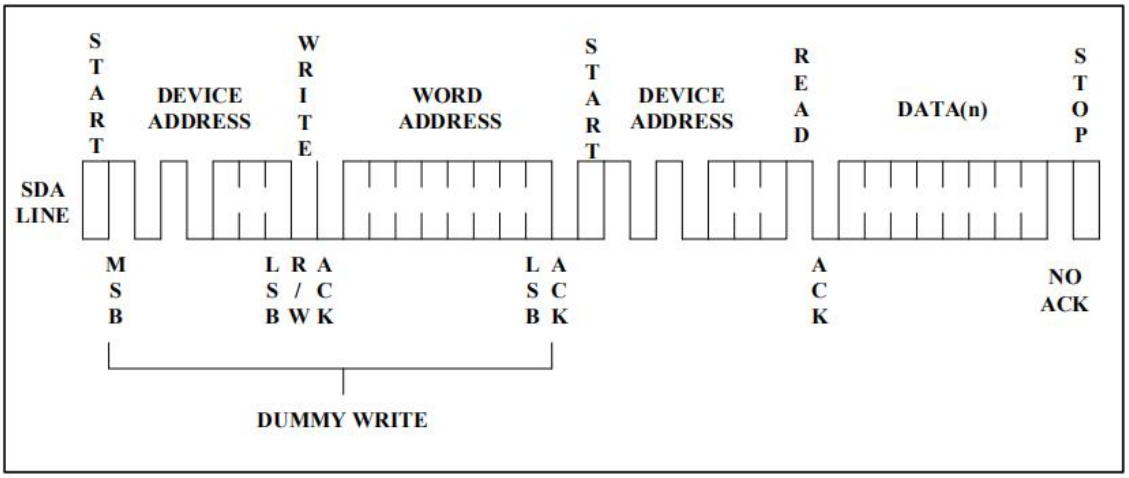
Figure 6-1



6.2 Random Read

A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 6-2**)

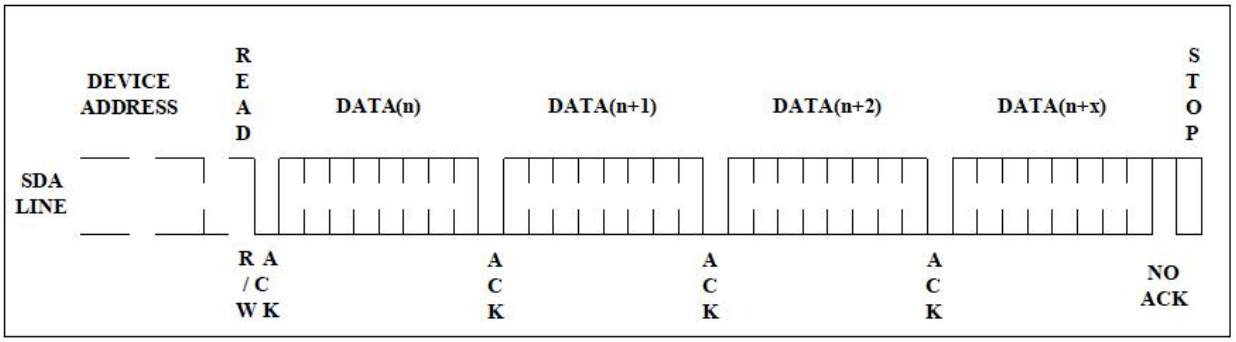
Figure 6-2



6.3 Sequential Read

Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see **Figure 6-3**).

Figure 6-3



7. Electrical Specifications

7.1 Absolute Maximum Ratings

- DC Supply Voltage.....-0.5V to +6.25V
- Input / Output Voltage.....-1.0V to +6.25V
- Operating Ambient Temperature.....-40℃ to +125℃
- Storage Temperature.....-65℃ to +150℃
- DC output current(SDA=0)..... 5mA
- Electrostatic pulse (Human Body model) 4000V

Comments:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Pin Capacitance [1]

Symbol	Parameter	Max.	Units	Test Condition
$C_{I/O}$	Input / Output Capacitance (SDA)	8	pF	$V_{I/O}$= Vss
C_{IN}	Input Capacitance (A0,A1,A2,WP,SCL)	6	pF	V_{IN}= Vss

8.DC Characteristics

Applicable over recommended operating range from: TA = -40℃ to +125℃, VCC = +1.7V to +5.5V (unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
Vcc	Supply Voltage	1.6	-	5.5	V	
		1.7	-	5.5	V	
Isb	Standby Current	-	-	1.0	uA	Vcc = 3.3V
		-	-	3.0	uA	Vcc = 5.5V
I_{CC1}	Supply Current	-	0.15	0.45	mA	Vcc=5.5V, Read at 400khz
I_{CC2}	Supply Current	-	0.75	1.65	mA	Vcc=5.5V Write at 400khz
I_{LI}	Input Leakage Current	-	0.10	1.0	μA	V_{IN} = Vcc or Vss
I_{LO}	Output Leakage Current	-	0.05	1.0	μA	V_{OUT} = Vcc or Vss
V_{IL}	Input Low Level	–0.6	-	0.3Vcc	V	
V_{IH}	Input High Level	0.7Vcc	-	Vcc+0.5	V	
V_{OL1}	Output Low Level Vcc = 1.7V (SDA)	-	-	0.2	V	I_{OL} = 1.5 mA
V_{OL2}	Output Low Level Vcc = 3.0V (SDA)	-	-	0.4	V	I_{OL} = 2.1 mA

9. AC Characteristics

Applicable over recommended operating range from TA = -40℃ to +125℃, VCC = +1.7V to +5.5V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	1.7≤V_{CC}≤5.5			2.5≤V_{CC}≤5.5			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{SCL}	Clock Frequency, SCL	-	-	400	-	-	1000	kHz
t_{LOW}	Clock Pulse Width Low	1.35	-	-	0.43	-	-	μs
t_{HIGH}	Clock Pulse Width High	0.55	-	-	0.45	-	-	μs
t_{AA}	Clock Low to Data Out Valid	0.05	-	1.0	0.05	-	0.55	μs
t_I	Noise Suppression Time	-	-	0.1	-	-	0.05	μs
t_{BUF}	Time the bus must be free before a new transmission can start	1.3	-	-	0.5	-	-	μs
$t_{HD.STA}$	Start Hold Time	0.6	-	-	0.25	-	-	μs
$t_{SU.STA}$	Start Setup Time	0.65	-	-	0.28	-	-	μs
$t_{HD.DAT}$	Data In Hold Time	0	-	-	0	-	-	μs
$t_{SU.DAT}$	Data In Setup Time	0.1	-	-	0.1	-	-	μs
t_R	Inputs Rise Time[1]	-	-	0.3	-	-	0.3	μs
t_F	Inputs Fall Time[1]	-	-	0.3	-	-	0.1	μs
$t_{SU.STO}$	Stop Setup Time	0.63	-	-	0.26	-	-	μs
t_{DH}	Data Out Hold Time	0.05	-	-	0.05	-	-	μs
$t_{SU.WP}$	WP pin Setup Time	1.2	-	-	0.65	-	-	μs
$t_{HD.WP}$	WP pin Hold Time	1.25	-	-	0.6	-	-	μs
t_{WR}	Write Cycle Time	-	-	5	-	-	5	ms

Notes:

1. This parameter is characterized and is not 100% tested.
2. AC measurement conditions:
   RL (connects to VCC): 1.3 k
   Input pulse voltages: 0.3 VCC to 0.7
   VCC Input rise and fall time: 50 ns
   Input and output timing reference voltages: 0.5 VCC
   The value of RL should be concerned according to the actual loading on the user's system.

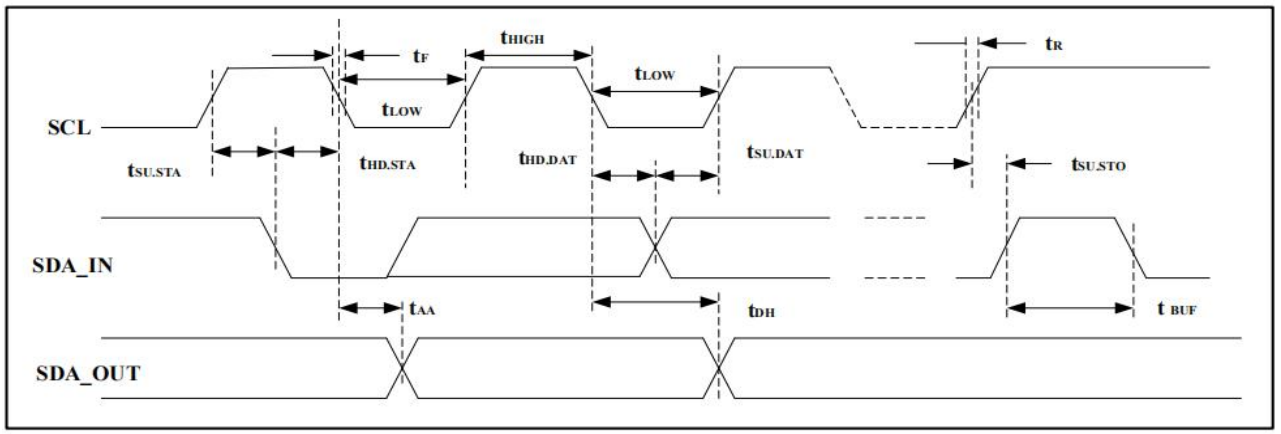
Reliability Characteristic [1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
EDR [2]	Endurance	1,000,000			Write cycles
DRET	Data retention	100			Years

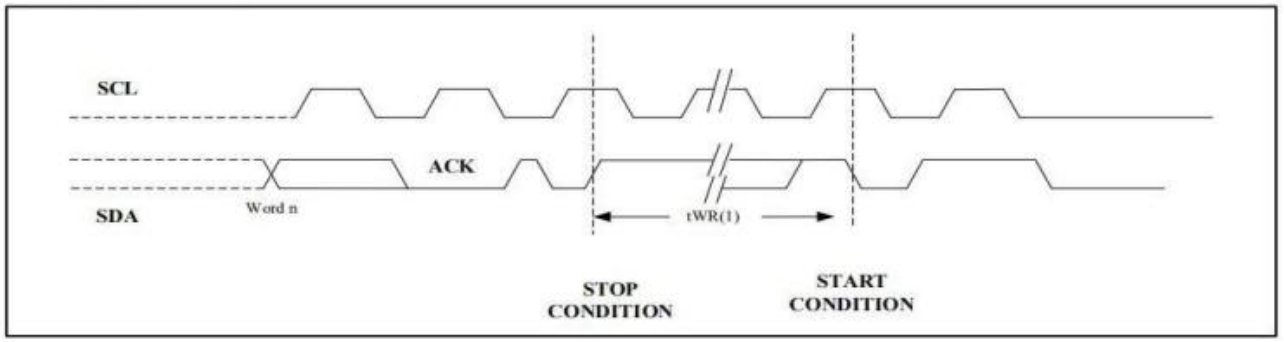
Note: [1] This parameter is ensured by characterization and is not 100% tested

[2] Under the condition: 25°C, 3.3V, Page mode

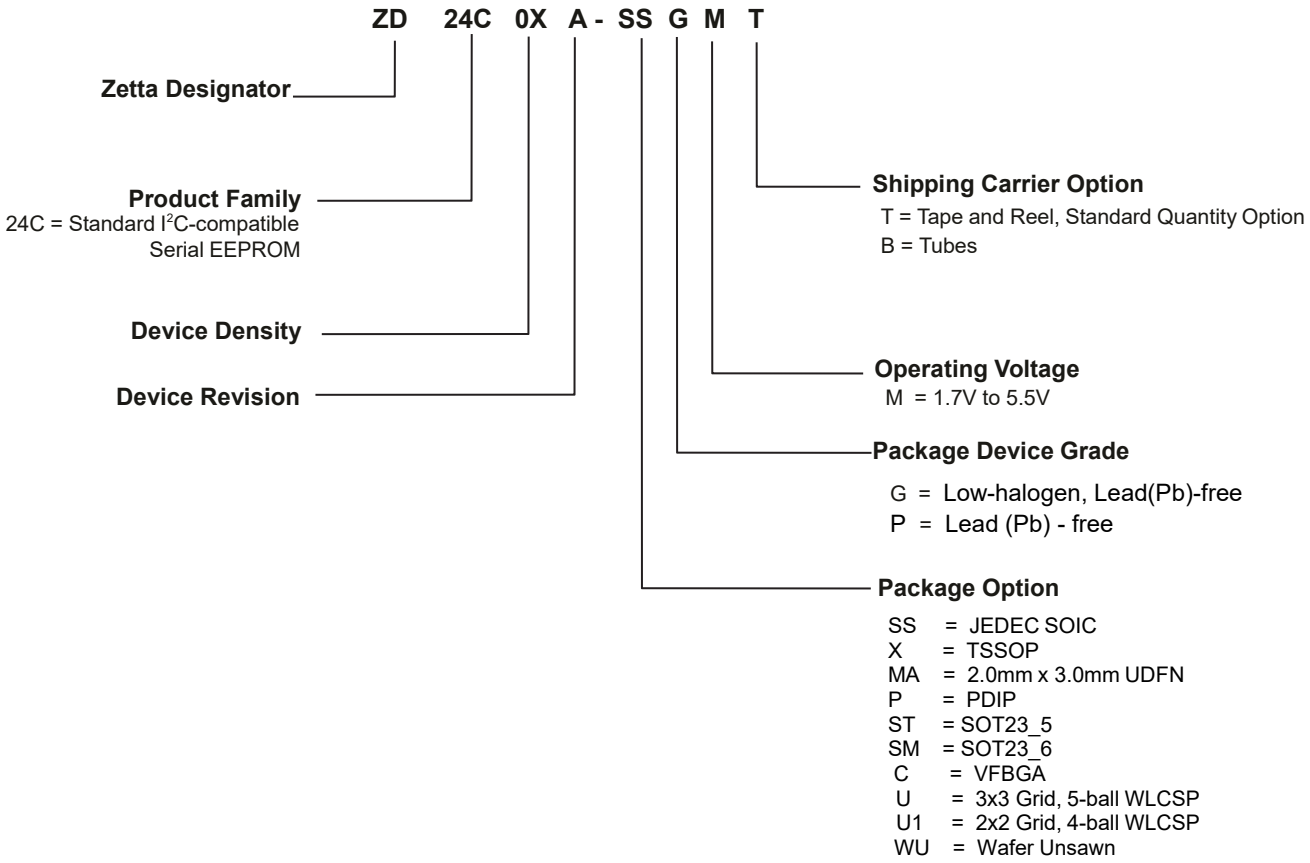
Bus Timing



Write Cycle Timing

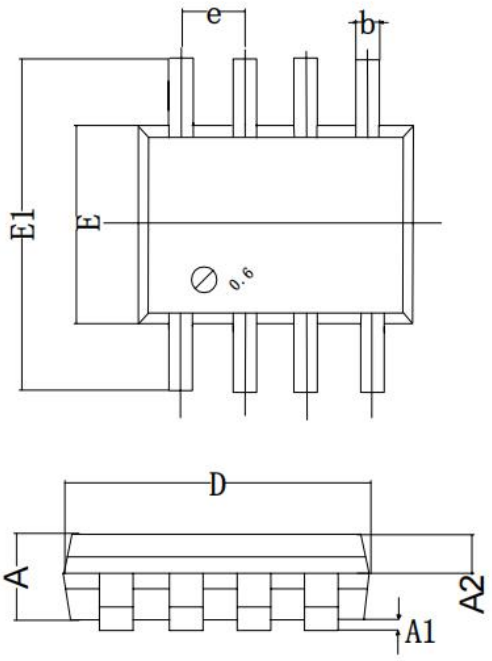


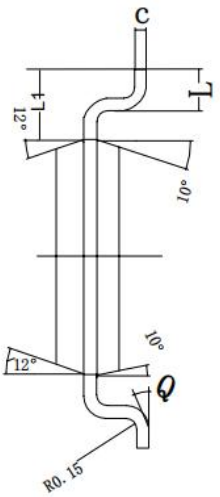
10. Ordering Information



11. Packaging Information

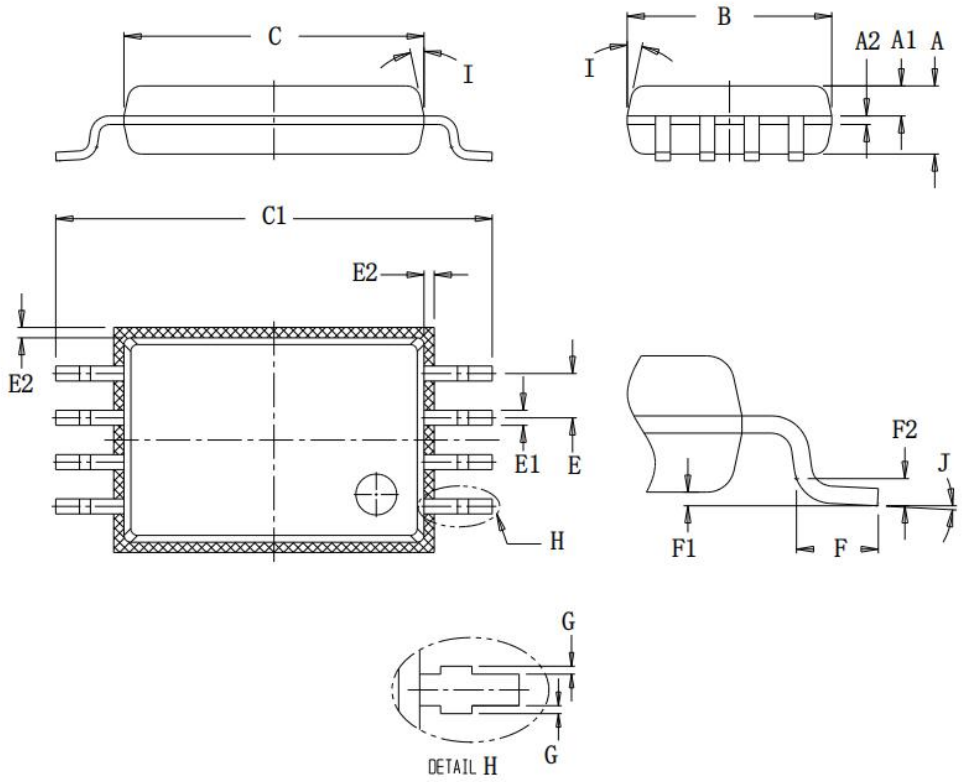
11.1 SOP8





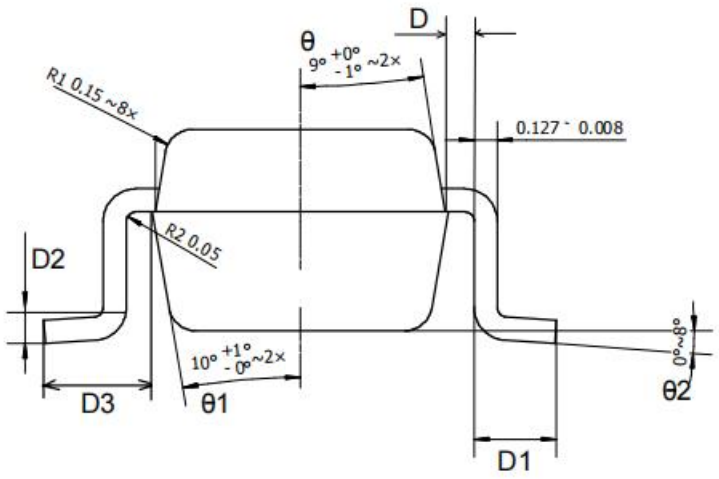
COMMON DIMENSIONS CUNITS MEASURE=MILLIMETER			
SYMBOL	MIN	NOM	MAX
A	1.35	1.45	1.55
A1	0.00	0.05	0.10
A2	0.65	0.70	0.75
b	0.30	0.40	0.45
c	0.18	0.20	0.22
D	4.70	4.90	5.10
e	-	1.27TYP	-
E1	5.80	6.00	6.20
E	3.80	3.90	4.00
L	0.40	0.60	0.80
Q	0°	/	8°
L1	1.05REF		

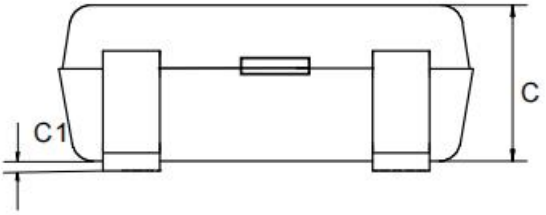
11.2 TSSOP

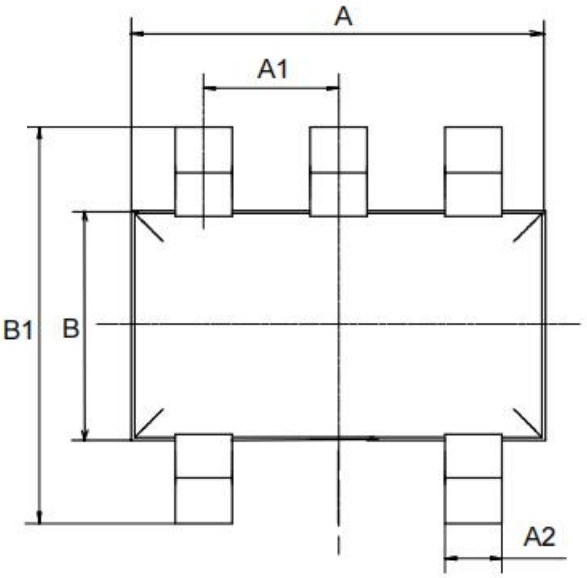


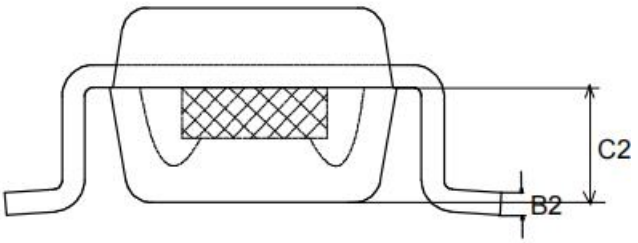
COMMON DIMENSIONS CUNITS MEASURE=MILLIMETER			
SYMBOL	MIN	NOM	MAX
A	0.95	1.00	1.05
A1	0.39	0.44	0.49
A2	-	0.127	-
B	2.95	3.00	3.05
C	4.35	4.40	4.45
C1	6.30	6.40	6.50
E	-	0.65TYP	-
E1	0.195	0.22	0.245
E2	-	0.12	-
F	0.5	0.60	0.7
F1	0	0.05	0.1
F2	-	0.2	-
G	-	0.075	-
I	10°	12°	14°
J	0°	3°	6°

11.3 SOT23-5L





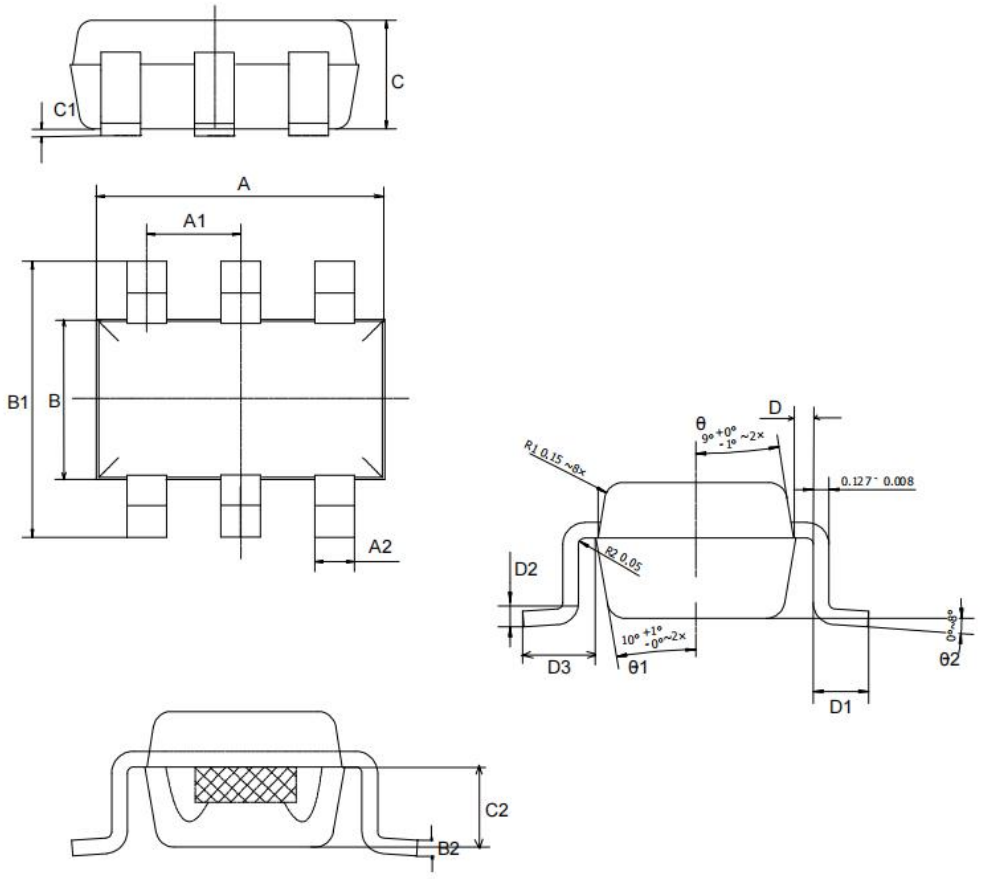




COMMON DIMENSIONS CUNITS MEASURE=MILLIMETER			
SYMBOL	MIN	NOM	MAX
A	2.82	2.92	3.02
A1	0.90	0.95	1.0
A2	0.33	0.40	0.43
B	1.52	1.62	1.72
B1	2.80	2.90	3.0
B2	0.12	0.128	0.135
C	1.05	1.10	1.15
C1	0.03	0.08	0.13
C2	0.6	0.65	0.7
D	0.03	0.08	0.13
D1	0.4	0.45	0.5
D2	0.25TYP		
D3	0.6	0.65	0.7

11.4 SOT23-6L

SOT23-6L 12/14排框架



COMMON DIMENSIONS CUNITS MEASURE=MILLIMETER			
SYMBOL	MIN	NOM	MAX
A	2.82	2.92	3.02
A1	0.90	0.95	1.0
A2	0.33	0.40	0.43
B	1.52	1.62	1.72
B1	2.80	2.90	3.0
B2	0.12	0.128	0.135
C	1.05	1.10	1.15
C1	0.03	0.08	0.13
C2	0.6	0.65	0.7
D	0.03	0.08	0.13
D1	0.4	0.45	0.5
D2	0.25TYP		
D3	0.6	0.65	0.7

12. Revision History

Rev.	Date	Description
1.0	2022-10-10	Initial Release
1.1	2023-01-02	Modify Package Information

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