64 Megabit Serial Flash Memory with 4Kbytes Uniform Sector

ZD25LQ64

FEATURES

Family of SPI Flash Memories
- ZD25LQ: 64M-bit / 8M-byte
- Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
- Dual SPI: CLK, /CS, IO_0, IO_1, /WP, /Hold
- Quad SPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3
- QPI: CLK, /CS, IO_0, IO_1, IO_2, IO_3

Highest Performance Serial Flash
- 133MHz Standard/Dual/Quad SPI clocks
- More than 100,000 erase/program cycles
- More than 20-year data retention
- Comparable to X16 Parallel Flash

Low Power consumption

- 8 mA typical active current
- <2μA Power-down (typ.)

Flexible Architecture with 4KB sectors
- Uniform Sector Erase (4K-bytes)
- Uniform Block Erase (32K and 64K-bytes)
- Program 1 to 256 byte per programmable page

Advanced Security Features

- Write protect all/portion of memory via software
- Enable/Disable protection with WP# Pin
- 4K-Bit secured OTP

Space Efficien Packaging

- 8-pin SOIC 208-mil / VSOP8
- 8-pad WSON 6x5-mm
- SOP16 (300mil)
- Contact Zetta for KGD and other options

GENERAL DESCRIPTION

The ZD25LQ64 supports the standard Serial Peripheral Interface (SPI), and Quad Peripheral Interface (QPI): Serial Clock, Chip Select, Serial Data I/O0(DI), I/O1(DO), I/O2(/WP), and I/O3(/HOLD). SPI clock frequencies of up to 133MHz are supported allowing equivalent clock rates of 266MHz for Dual Output and 532MHz for Quad Output when using the QPI and Fast Read Dual/Quad I/O instructions.

The ZD25LQ64 array is organized into 32,768 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time using the Page Program instructions. Pages can be erased Sector, 32KB Block, 64KB Block or the entire chip.

The devices operate on a single 1.65V to 1.95V power supply with current consumption as low as 5mA active and 2μA for Deep Power-down. All devices offered in space-saving packages. The device supports JEDEC standard manufacturer and device identification with a 4K-bit Secured OTP.

1. ORDERING INFORMATION

ZD25LQ XX X X X X X

Packaging Type
T:Tube
R:Tape & Reel
Y:Tray

Green Code
G: Low-halogen, Lead(Pb)-free
P: Lead (Pb) - free

Temperature Range
I: Industriial(-40℃~85℃)
A: Automotive (-40℃~125℃)

Package Type
S: 208mil SOP8
W: WSON 5 mm x 6 mm
V: 208mil VSOP8

Version
A: A Version
B: B Version
C: C Version

Device Density
32: 32Mbit
64: 64Mbit
128: 128Mbit

Base Part Number
ZD: Zetta Device
25LQ:1.8V Serial 4Kbyte Uniform-sector Flash

Figure 1, Ordering Information

2. BLOCK DIAGRAM

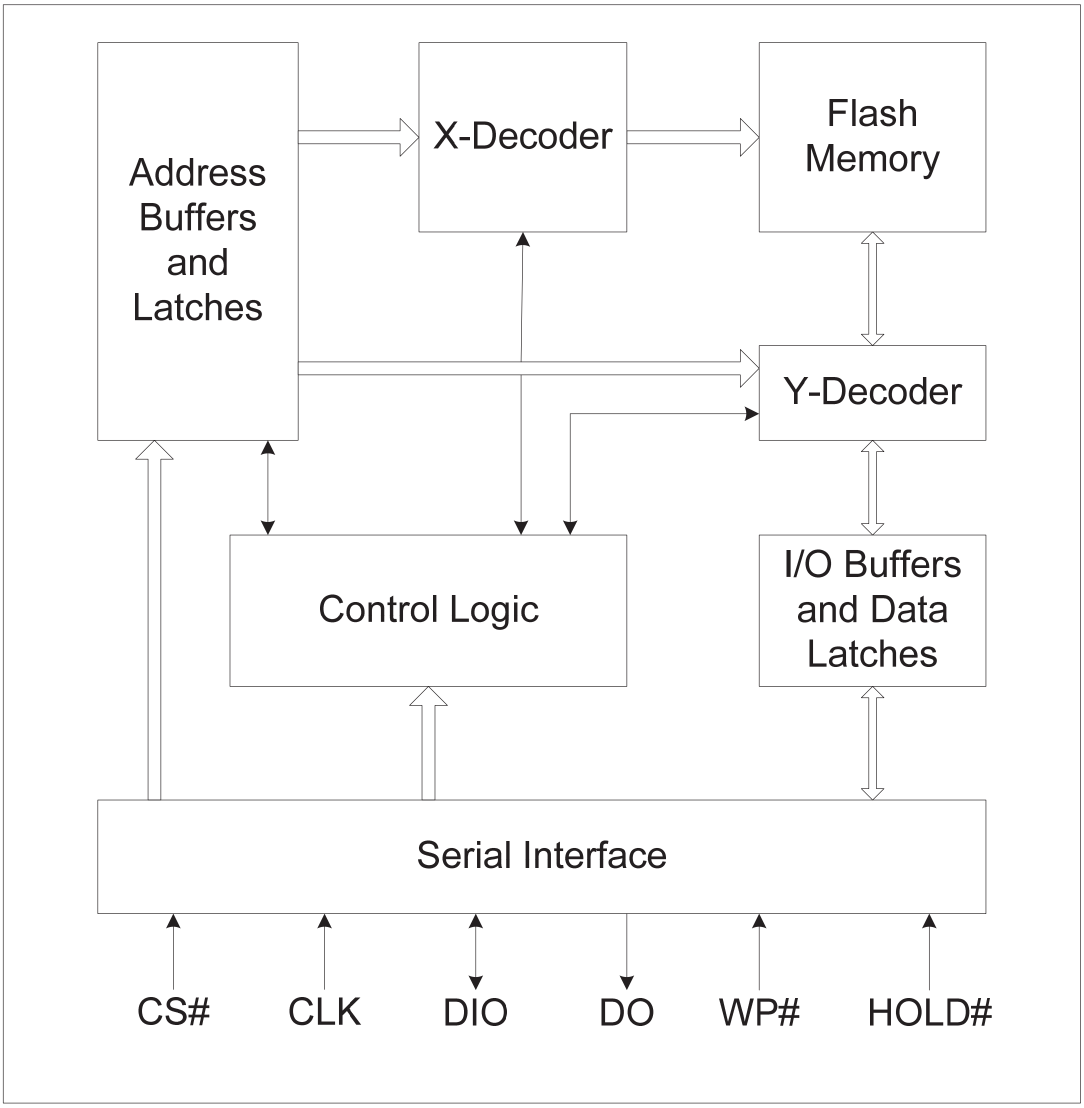


Figure 2, Block Diagram

3. CONNECTION DIAGRAMS

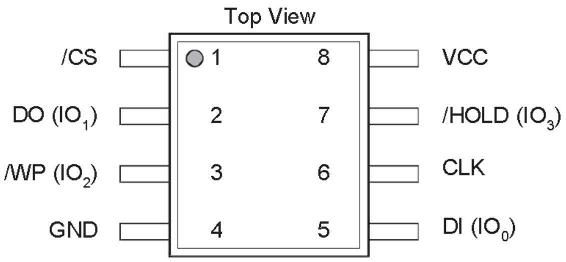


Figure 3.1, 8-pin SOP (208mil)

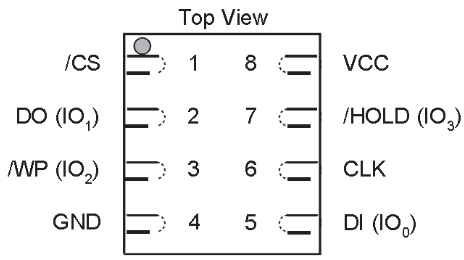


Figure 3.2, 8-Contact 6 x 5 mm WSON

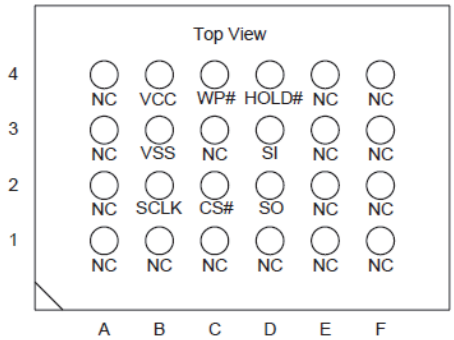


Figure 3.3, 24-BALL TFBGA

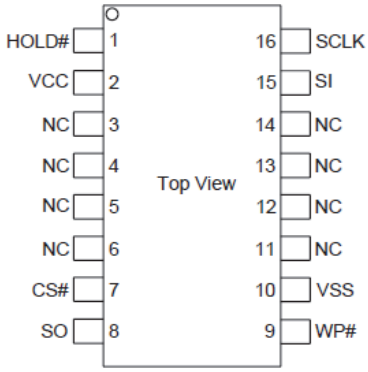


Figure 3.4, 16-LEAD SOP

4. SIGNAL DESCRIPTIONS

Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)
The ZD25LQ64 supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK. Dual/Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. When use Quad Output instructions, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

Serial Clock (CLK)
The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Mode")

Chip Select (CS#)
The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high, the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low, the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up and power-down. If needed a pull-up resister on /CS can be used to accomplish this.

Write Protect (WP#)
The Write Protect (/WP) pin can be used to prevent the Status Registers from being written. Used in Conjunction with the Status Register's Block Protect (CMP, SEC, TB, BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion as small as a 4KB sector or the entire memory array can be hardware protected. The /WP pin is active low.

Accelerated Programming (ACC)
The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput at the factory.
If the system asserts VHH on this pin, the device uses the higher voltage on the pin to reduce the time required for program operations. Removing VHH from the ACC pin returns the device to normal operation.
Note that the ACC pin must not be at VHH for operations other than accelerated programming, or device damage may result. In addition, the ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.
***Note:** The ACC function is only available during standard SPI Mode.

HOLD (/HOLD)
The /HOLD pin is used to pause any serial communications with the device without deselecting the device. When /HOLD goes low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). When /HOLD goes high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set Quad I/O, the /HOLD pin function is not available since this pin used for IO3.

Table1, Pin Descriptions

Symbol	Pin Name
/CS	Chip Select Input
DO (IO1)	Data Output (Data Input Output 1)*[1]
/WP (IO2)	Write Protect Input (Data Input Output 2)*[2]
GND	Ground
DI (IO0)	Data Input (Data Input Output 0)*[1]
CLK	Serial Clock Input
/HOLD (IO3)	Hold Input (Data Input Output 3)*[2]

*1 IO0 and IO1 are used for Standard and Dual SPI instructions

*2 IO3 are used for Quad SPI instructions

5. MEMORY ORGANIZATIONS

The memory is organized as:
- 8,388,608bytes
- Uniform Sector Architecture
  128 blocks of 64-Kbyte
  2,048 sectors of 4-Kbyte
  32,768 pages (256 bytes each)

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector, Block or Chip Erasable but not Page Erasable.

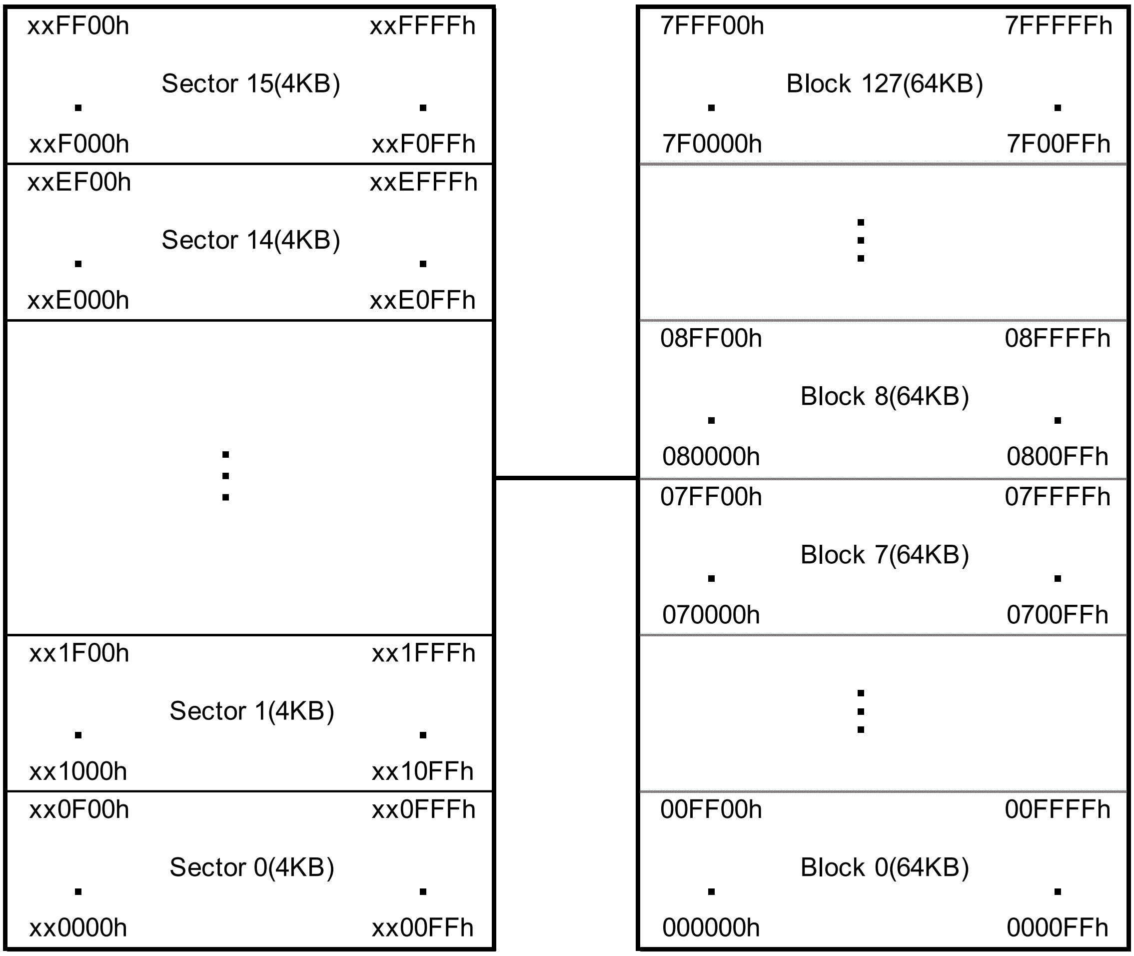


Figure 4, Memory Organization

6. FUNCTION DESCRIPTION

Standard SPI Instructions

The ZD25LQ64 is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3, the CLK signal is normally high on the falling and rising edges of /CS.

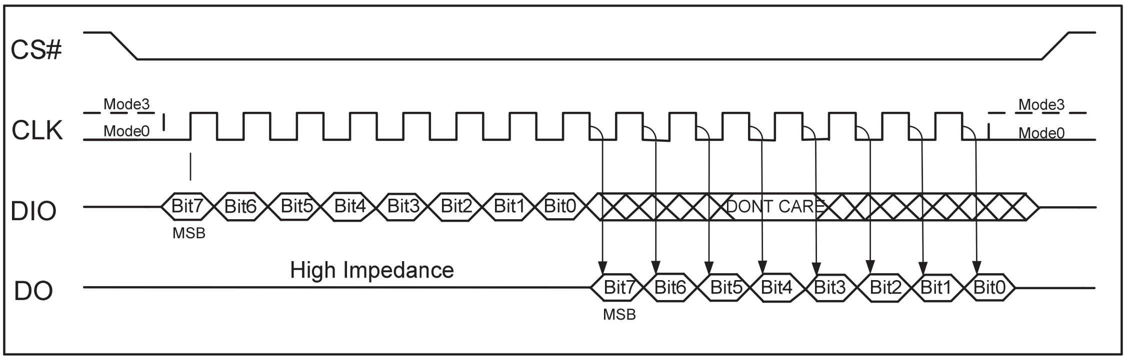


Figure 5, SPI Modes

Dual SPI

The ZD25LQ64 supports Dual SPI operation. This instruction allows data to be transferred to or from the device at two times the rate of the standard SPI. The Dual Read instruction is ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed- critical code directly from the SPI bus (XIP). When using Dual SPI instructions the DI and DO pins become bidirectional I/0 pins; IO0 and IO1.

Quad SPI

The ZD25LQ64 supports Quad SPI operation. This instruction allows data to be transferred to or from the device at four times the rate of the standard SPI. The Quad Read instruction offers a significant improvement in continuous and random access transfer rates allowing fast code- shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instruction the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

QPI Function

The ZD25LQ64 supports Quad Peripheral Interface (QPI) operation when the device is switched from Standard/ Dual/ Quad SPI mode to QPI mode using the “Enable QPI (38h)” instruction. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set. When using QPI instructions, the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively.
The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via DI pin in eight serial clocks. The QPI mode utilizes all four IO pins to input the instruction code, thus only two serial clocks are required. This can significantly reduce the SPI instruction overhead and improve system performance in an XIP environment. Standard/ Dual/ Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time, “Enable QPI” and “Disable QPI/ Disable QPI 2” instructions are used to switch between these two modes. Upon power-up or after software reset using “Reset (99h) instruction, the default state of the device is Standard/ Dual/ Quad SPI mode.

Hold

The HOLD# function is only available when QE=0, If QE=1, The HOLD# functions is disabled, the pin acts as dedicated data I/O pin.
The HOLD# signal goes low to stop any serial communications with the device, but doesn’t stop the operation of write status register, programming, or erasing in progress.
The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD

condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

The SO is high impedance, both SI and SCLK don’t care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

7. STATUS REGISTERS

The Read Status Register instruction can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled the state of write protection and the Quad SPI setting. The Write Status Register instruction can be used to configure the devices writes protection features and Quad SPI setting. Write access to the Status Register is controlled by in some cases of the /WP pin.

S7	S6	S5	S4	S3	S2	S1	S0
SRP0	SEC	TB	BP2	BP1	BP0	WEL	BUSY
Status Register Protect 0 (Non-Volatile)	Sector Protect (Non-Volatile)	Top/Bottom Write Protect (Non-Volatile)	Block Protect (Non-Volatile)	Block Protect (Non-Volatile)	Block Protect (Non-Volatile)	Write Enable Latch	Erase or Write in Progress

Figure 6a, Status Register-1

- **BUSY**
  BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction. During this time the device will ignore further instructions except for the Read Status Register instruction (see tW, tPP, tSE, tBE, and tCE in AC Characteristics). When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

- **Write Enable Latch (WEL)**
  Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to a 1 after executing a Write Enable Instruction. The WEL status bit is cleared to a 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register.

- **Block Protect Bits (BP2, BP1, BP0)**
  Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3 and S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tW in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected. The Block Protect bits can not be written to if the Status Register Protect (SRP) bit is set to 1 and the Write Protect (/WP) pin is low.

- **Top/Bottom Block protect (TB)**
  The Top/Bottom bit (TB) is non-volatile bits in the status register (S5) that controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP0, SRP1 and WEL bits.

- **Sector/Block Protect (SEC)**
  The Sector protect bit (SEC) is non-volatile bits in the status register (S6) that controls if the Block Protect Bits (BP2, BP1, BP0) protect 4KB Sectors (SEC=1) or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory protection table. The default setting is SEC=0.

- **Status Register protect (SRP1, SRP0)**
  The Status Register Protect bits (SRP1 and SRP0) are non-volatile read/write bits in the status register (S8 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

SRP1	SRP0	/WP	Status Register	Description
0	0	X	Software Protection	/WP pin no control. The register can be written to After a Write Enable instruction, WEL=1. [Factory Default]
0	1	0	Hardware Protected	When /WP pin is low the Status Register locked and can not Be written to.
0	1	1	Hardware Unprotected	When /WP pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1
1	0	X	Power Supply Lock-Down	Status Register is protected and cannot be written to again until the next power-down, power-up cycle(1)
1	1	X	One Time Program	Status Register is permanently protected and cannot be written to.

Note:
1. When SRP1, SRP0 = (1,0), a power-down, power-up cycle will change SRP1, SRP0 to(0,0) state.

- **Complement Protect (CMP)**
  The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction the SEC, TB, BP2-BP0 bits to provide more flexibility for the array protection. Please see the Status registers Memory Protection table for details. The default setting is CMP=0.

S15	S14	S13	S12	S11	S10	S9	S8
SUS	CMP	(R)	(R)	(R)	(R)	QE	SRP1
Suspend Status	Complement Protect (Non-Volatile)	Reserved	Reserved	Reserved	Reserved	Quad Enable (Non-Volatile)	Status Register Protect 1 (Non-Volatile)

Figure 6b, Status Register-2

- **Quad Enable (QE)**
  The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad SPI operation. When the QE bit is set to a 0 state, the /WP pin and /HOLD are enabled. When the QE bit is set to a 1, the Quad IO2 and IO3 pins are enabled, and /WP and /HOLD functions are disabled.

  WARNING: If the /WP or /HOLD pins are tied directly to the power supply or ground during standard SPI or Dual SPI operation, the QE bit should never be set to a 1.

- **Erase/Program Suspend Status (SUS)**
  The Suspend Status bit (SUS) is a read only bit in the status register (S15) that is set to 1 after executing an Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

- **Reserved Bits**
  There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of those bits. During a “Write Status Register” instruction, the Reserved Bits can be written as “0”, but there will not be any effects.

ZD25LQ64 Status Register Memory Protection (CMP = 0)

STATUS REGISTER					MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	126 and 127	7E0000h-7FFFFFh	128KB	Upper 1/64
0	0	0	1	0	124 thru 127	7C0000h-7FFFFFh	256KB	Upper 1/32
0	0	0	1	1	120 thru 127	780000h-7FFFFFh	512KB	Upper 1/16
0	0	1	0	0	112 thru 127	700000h-7FFFFFh	1MB	Upper 1/8
0	0	1	0	1	96 thru 127	600000h-7FFFFFh	2MB	Upper 1/4
0	0	1	1	0	64 thru 127	400000h-7FFFFFh	4MB	Upper 1/2
0	1	0	0	1	0 and 1	000000h-01FFFFh	128KB	Lower 1/64
0	1	0	1	0	0 thru 3	000000h-03FFFFh	256KB	Lower 1/32
0	1	0	1	1	0 thru 7	000000h-07FFFFh	512KB	Lower 1/16
0	1	1	0	0	0 thru 15	000000h-0FFFFFh	1MB	Lower 1/8
0	1	1	0	1	0 thru 31	000000h-1FFFFFh	2MB	Lower 1/4
0	1	1	1	0	0 thru 63	000000h-3FFFFFh	4MB	Lower 1/2
X	X	1	1	1	0 thru 127	000000h-7FFFFFh	8MB	ALL
1	0	0	0	1	127	7FF000h-7FFFFFh	4KB	U – 1/2048
1	0	0	1	0	127	7FE000h-7FFFFFh	8KB	U – 1/1024
1	0	0	1	1	127	7FC000h-7FFFFFh	16KB	U – 1/512
1	0	1	0	X	127	7F8000h-7FFFFFh	32KB	U – 1/256
1	1	0	0	1	0	000000h-000FFFh	4KB	L – 1/2048
1	1	0	1	0	0	000000h-001FFFh	8KB	L – 1/1024
1	1	0	1	1	0	000000h-003FFFh	16KB	L – 1/512
1	1	1	0	X	0	000000h-007FFFh	32KB	L – 1/256

Note:
1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

- **ZD25LQ64 Status Register Memory Protection (CMP = 1)**

STATUS REGISTER					MEMORY PROTECTION			
SEC	TB	BP2	BP1	BP0	BLOCK(S)	ADDRESSES	DENSITY	PORTION
X	X	0	0	0	0 thru 127	000000h - 7FFFFFh	8MB	ALL
0	0	0	0	1	0 thru 125	000000h – 7DFFFFh	8,064KB	Lower 63/64
0	0	0	1	0	0 and 121	000000h – 7BFFFFh	7,936KB	Lower 31/32
0	0	0	1	1	0 thru 119	000000h – 77FFFFh	7,680KB	Lower 15/16
0	0	1	0	0	0 thru 111	000000h – 6FFFFFh	7,168KB	Lower 7/8
0	0	1	0	1	0 thru 95	000000h – 5FFFFFh	6MB	Lower 3/4
0	0	1	1	0	0 thru 63	000000h – 3FFFFFh	4MB	Lower 1/2
0	1	0	0	1	2 thru 127	020000h - 7FFFFFh	8,064KB	Upper 63/64
0	1	0	1	0	4 and 127	040000h - 7FFFFFh	7,936KB	Upper 31/32
0	1	0	1	1	8 thru 127	080000h - 7FFFFFh	7,680KB	Upper 15/16
0	1	1	0	0	16 thru 127	100000h - 7FFFFFh	7,168KB	Upper 7/8
0	1	1	0	1	32 thru 127	200000h - 7FFFFFh	6MB	Upper 3/4
0	1	1	1	0	64 thru 127	400000h - 7FFFFFh	4MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 thru 127	000000h - 7FEFFFh	8,188KB	L – 2047/2048
1	0	0	1	0	0 thru 127	000000h - 7FDFFFh	8,184KB	L – 1023/1024
1	0	0	1	1	0 thru 127	000000h - 7FBFFFh	8,176KB	L – 511/512
1	0	1	0	X	0 thru 127	000000h - 7F7FFFh	8,160KB	L – 255/256
1	1	0	0	1	0 thru 127	001000h - 7FFFFFh	8,188KB	U – 2047/2048
1	1	0	1	0	0 thru 127	002000h - 7FFFFFh	8,184KB	U – 1023/1024
1	1	0	1	1	0 thru 127	004000h - 7FFFFFh	8,176KB	U – 511/512
1	1	1	0	X	0 thru 127	008000h - 7FFFFFh	8,160KB	U – 255/256

Note:
1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

8 INSTRUCTIONS

The instruction set of the ZD25LQ64 consists of fifteen basic instructions that are fully controlled through the SPI bus (see Instruction Set table). Instructions are initiated with the falling edge of Chip Select (CS#). The first byte of data clocked into the DIO input provides the instruction code. Data on the DIO input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge CS#. Clock relative timing diagrams for each instruction are included in figures 7 through 43. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (CS driven high after a full 8-bits have been clocked) otherwise the instruction will be terminated. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

Instruction Set Table (Single/Dual/Quad SPI Instruction)

INSTRUCTION NAME	BYTE1 CODE	BYTE2	BYTE3	BYTE4	BYTE5	BYTE6	BYTE7	N-BYTES
Write Enable	06h							
Volatile SR Write Enable	50h							
write Disable	04h							
Read Status Register-1	05h	(S7-S0)(2)						
Read Status Register-2	35h	(S15-S8)(2)						
Write Status Register-1	01h	S7-S0	S15-S8					
Write Status Register-2	31h	S15-S8						
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	(Next byte)	Continuous
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(D7-D0)	(Next byte) continuous
Enable QPI	38h							
Fast Read Dual Output	3Bh	A23-A16	A15-A8	A7-A0	dummy	I/O= (D6,D4,D2,D0) O= (D7,D5,D3,D1)	(One byte per 4 clocks, continuous)	
Dual I/O Fast Read	BBh	A23-A16	A15-A8	A7-A0	M7-M0	I/O= (D6,D4,D2,D0) O= (D7,D5,D3,D1)	(One byte per 4 clocks, continuous)	
Fast Read Quad Output	6Bh	A23-A16	A15-A8	A7-A0	dummy	IO0 = (D4, D0) IO1 = (D5, D1) IO2 = (D6, D2) IO3 = (D7, D3)	(One byte per 2 clocks, continuous)	
Quad I/O Fast Read	EBh	A23-A16	A15-A8	A7-A0	M7-M0	dummy	dummy	(D7-D0)
Quad I/O Word Fast Read	E7h	A23-A16	A15-A8	A7-A0	M7-M0	dummy	(D7-D0)	(D7-D0)
Page Program	02h	A23-A16	A15-A8	A7-A0	(D7-D0)(3)	(Next byte)	Up to 256	
Quad Page Program	33h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	Up to 256	
Block Erase(64KB)	D8h	A23-A16	A15-A8	A7-A0				
Half Block Erase(32KB)	52h	A23-A16	A15-A8	A7-A0				
Sector Erase(4KB)	20h	A23-A16	A15-A8	A7-A0				
Chip Erase	C7/60h							

Enable Reset	66h							
Reset	99h							
Set Burst with Wrap	77h	dummy						
Enter Secured OTP	B1h							
Exit Secured OTP	C1h							
Read security Register	2Bh	(SC7 – SC0)						
Write security Register	2Fh							
Power-down	B9h							
Release Power-down /Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)(2)			
Manufacturer /Device ID(3)	90h	dummy	dummy	00h	(MID7-MID0)	(ID7-ID0)		
JEDEC ID	9Fh	(MID7-MID0)	(ID15-ID8) Memory Type	(ID7-ID0) Capacity				

Notes:
1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data output from the device on either 1, 2 or 4 IO pins.
2. The Status Register contents and Device ID will repeat continuously until /CS terminates the instruction.
3. At least one byte of data input is required for Page Program, Quad Page Program, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.

Instruction Set Table (QPI instruction)

INSTRUCTION NAME	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7	BYTE 8	BYTE 9
(CLOCK NUMBER)	(0 , 1)	(2 , 3)	(4 , 5)	(6 , 7)	(8 , 9)	(10 , 11)	(12 , 13)	(14 , 15)	(16 , 17)
Write Enable	**06h**								
Write Enable for Volatile Status Register	**50h**								
Write Disable	**04h**								
Read Status Register-1	**05h**	(SR7-SR0) (2)							
Read Status Register-2	**35h**	(SR15-SR8)(2)							
Write Status Register-1	**01h**	(SR7-SR0)	(SR15-SR8)						
Write Status Register-2	**31h**	(SR15-SR8)							
Fast Read Data >80MHz	**0Bh**	A23-A16	A15-A8	A7-A0	dummy	dummy	(D7-D0)		
Fast Read Data >108MHz	**0Bh**	A23-A16	A15-A8	A7-A0	dummy	dummy	dummy	(D7-D0)	
Fast Read Data >133MHz	**0Bh**	A23-A16	A15-A8	A7-A0	dummy	dummy	dummy	dummy	(D7-D0)
Page Program	**02h**	A23-A16	A15-A8	A7-A0	(D7-D0) (3)				
Sector Erase(4KB)	**20h**	A23-A16	A15-A8	A7-A0					
Block Erase(32KB)	**52h**	A23-A16	A15-A8	A7-A0					
Block Erase(64KB)	**D8h**	A23-A16	A15-A8	A7-A0					
Chip Erase	**60h/ C7h**								
Erase/Program Suspend	**75h**								
Erase/Program Resume	**7Ah**								
Deep Power-down	**B9h**								
Release Deep power down	**ABh**								

Read Manufacturer/ Device ID		**90h**	00h	00h	00h or 01h	(MID7-MID0)	(DID7-DID0)			
Read JEDEC ID		**9Fh**	(MID7-MID0) Manufacturer	(D7-D0) Memory Type	(D7-D0) Capacity Type					
Enter Security		**B1h**								
Exit Security		**C1h**								
Read Security Register		**2Bh**	(SC7-SC0) (10)							
Write Security Register		**2Fh**								
Fast Read Quad I/O	>80MHz	**EBh**	A23-A16	A15-A8	A7-A0	(M7-M0)	dummy	(D7-D0)		
	>108MHz		A23-A16	A15-A8	A7-A0	(M7`-M0)	dummy	dummy	(D7-D0)	
	>133MHz		A23-A16	A15-A8	A7-A0	(M7`-M0)	dummy	dummy	dummy	(D7-D0)
Reset Enable		**66h**								
Reset		**99h**								
Disable QPI		**FFh**								
Burst Read with Wrap	>80MHz	**0Ch**	A23-A16	A15-A8	A7-A0	dummy	dummy	(D7-D0)		
	>108MHz		A23-A16	A15-A8	A7-A0	dummy	dummy	dummy	(D7-D0)	
	>133MHz		A23-A16	A15-A8	A7-A0	dummy	dummy	dummy	dummy	(D7-D0)
Set Read Parameter		**C0h**	P7-P0							
Quad Page Program		**33h**	A23-A16	A15-A8	A7-A0	(D7-D0)				

Table 2, Manufacturer and Device Identification

		ID code	Instruction
Manufacturer ID		BAh	90h, 92h, 94h, 9Fh
Device ID	ZD25LQ64	16h	90h, 92h, 94h, ABh
Memory Type ID	SPI / QPI	43h	9Fh
Capacity Type ID	64M	17h	9Fh

8.1 Write Enable (06h)

The Write Enable instruction (Figure 7) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register instruction. The Write Enable instruction is entered by driving CS# low, shifting the instruction code "06h" into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

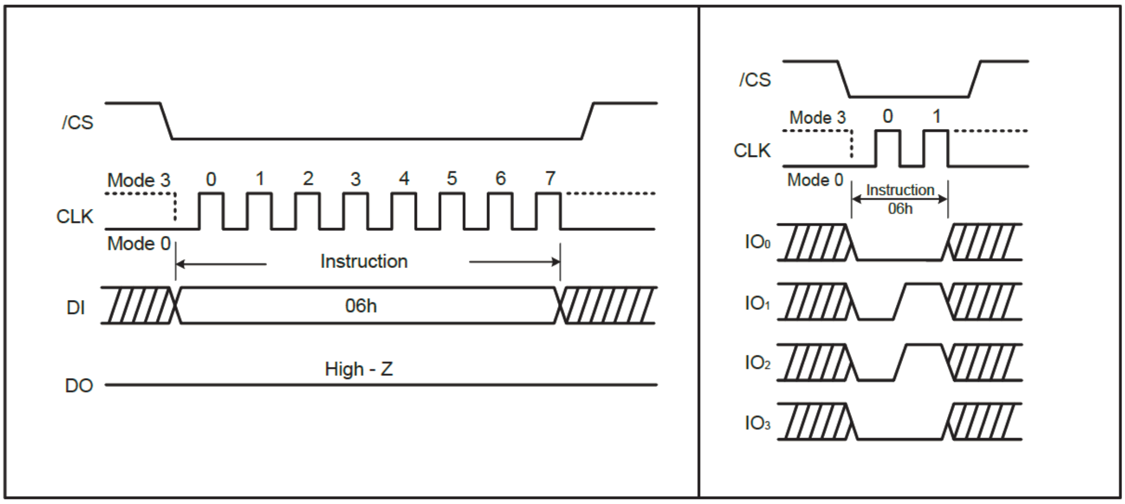


Figure 7, Write Enable Instruction Sequence Diagram and QPI Mode (right)

8.2 Write Disable (04h)

The Write Disable instruction (Figure 8) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving CS# low, shifting the instruction code “04h” into the DIO pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase instructions.

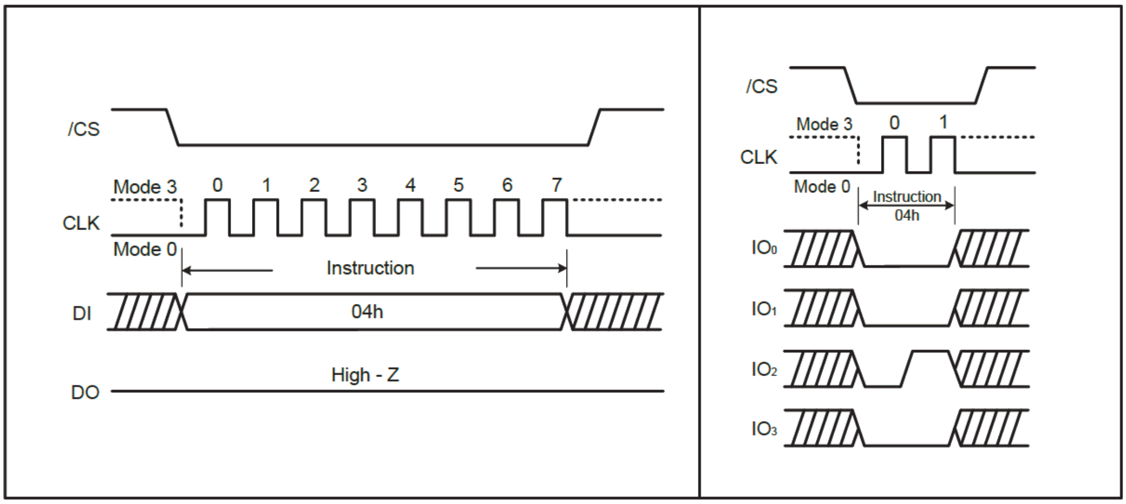


Figure 8, Write Disable Instruction Sequence Diagram and QPI Mode (right)

8.3 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

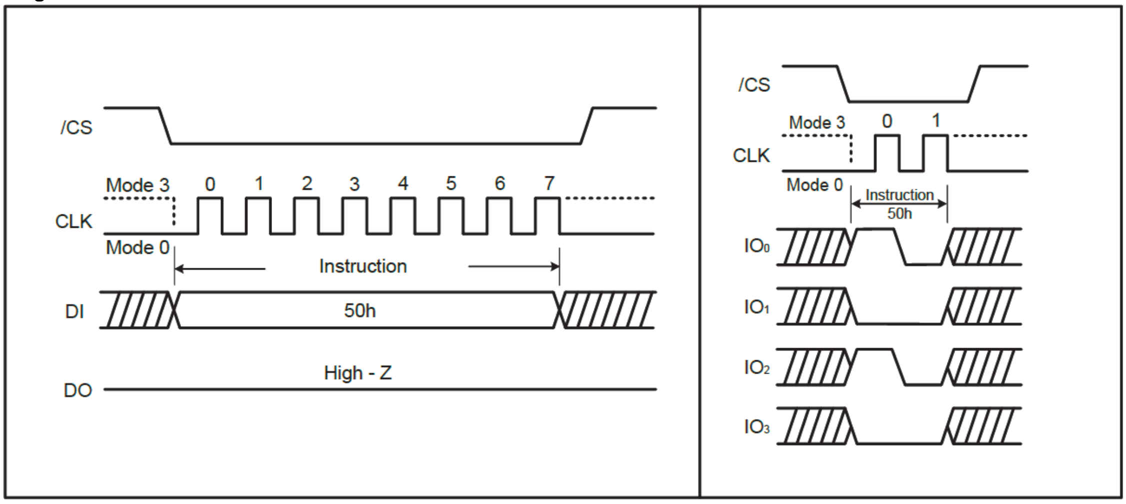


Figure 9, Write Enable for Volatile Status Register Sequence Diagram and QPI Mode (right)

8.4 Read Status Register (RDSR) (05H or 35H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code "05H" / "35H", the SO will output Status Register bits S7~S0 / S15-S8.

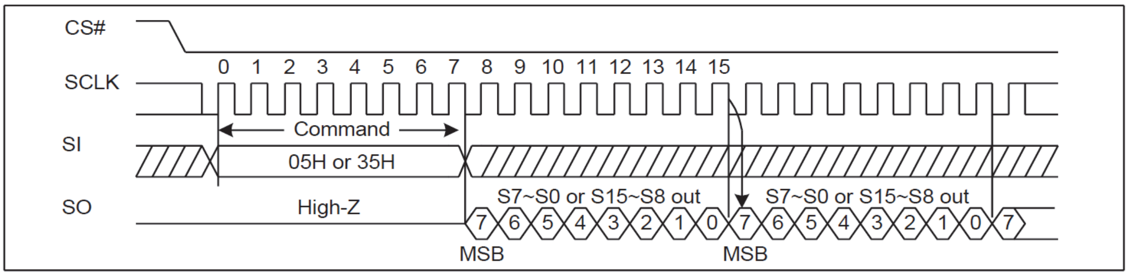


Figure 10a, Read Status Register Instruction Sequence Diagram

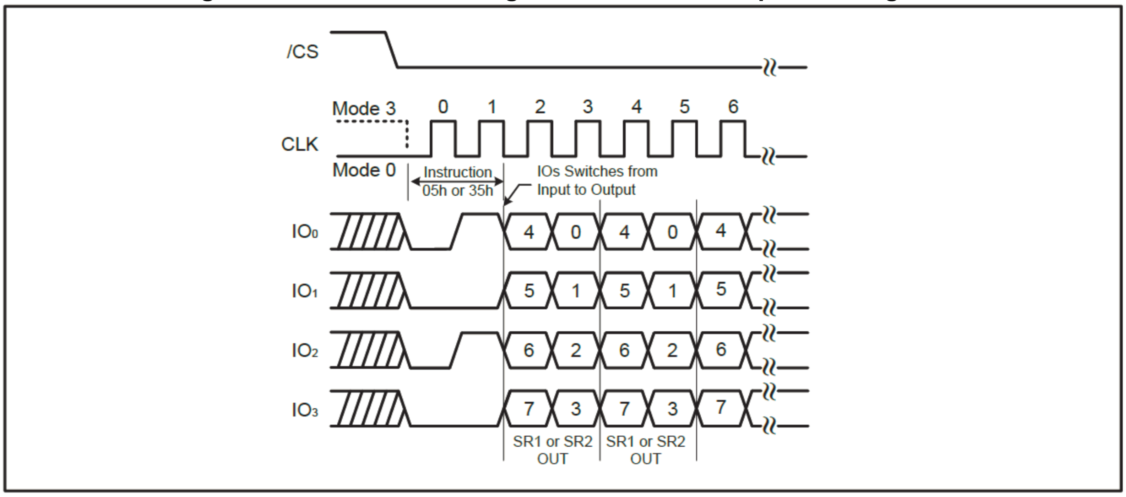


Figure 10b. Read Status Register Instruction (QPI Mode)

8.5 Write Status Register (WRSR) (01H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on S1 and S0 of the Status Register. CS# must be driven high after the eighth or sixteen bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the BUSY bit. The BUSY bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the BUSY is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (CMP, SEC, TB, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered.

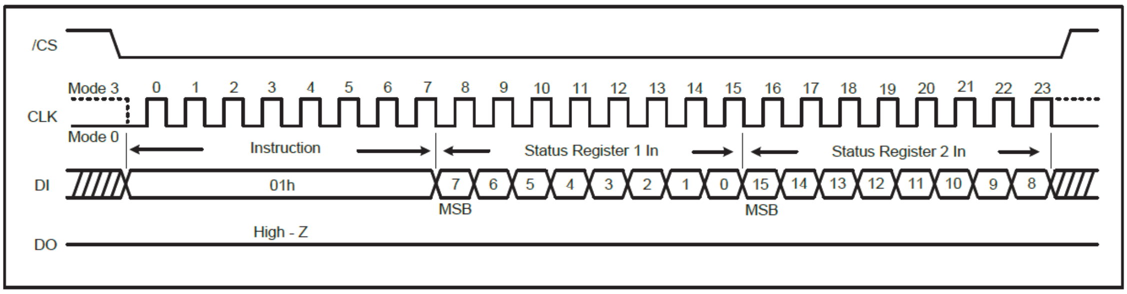


Figure 11a, Write Status Register Instruction Sequence Diagram

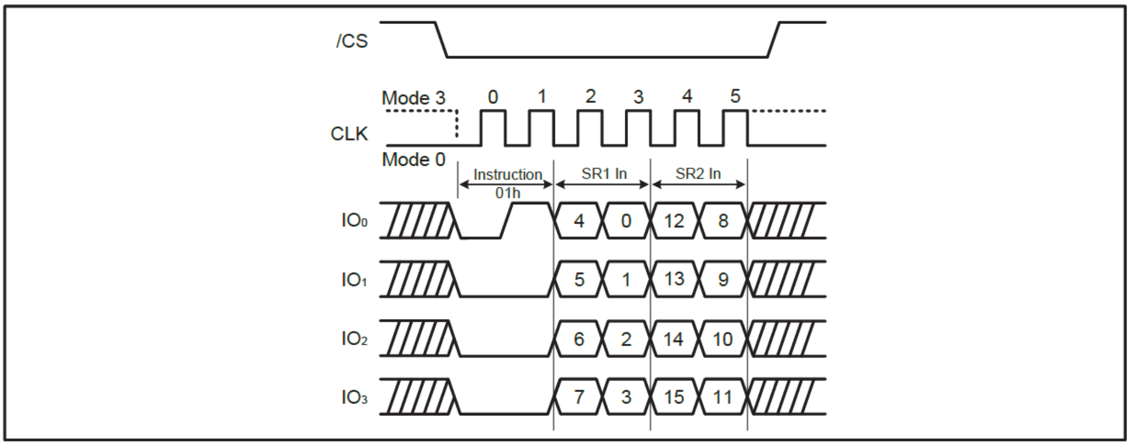


Figure 11b. Write Status Register Instruction (QPI Mode)

8.6 Write Status Register-2 (31H)

The Write Status Register-2instruction is to write only non-volatile Status Register-2bits (CMP, QE and SRP1).

A Write Enable instruction must previously have been issued prior to setting Write Status Register Instruction (Status Register bit WEL must equal 1). Once write is enabled, the instruction is entered by driving /CS low, sending the instruction code, and then writing the status register data byte as illustrated in figure 12.

Using Write Status Register-2(31h) instruction, software can individually access each one-byte status registers via different instructions.

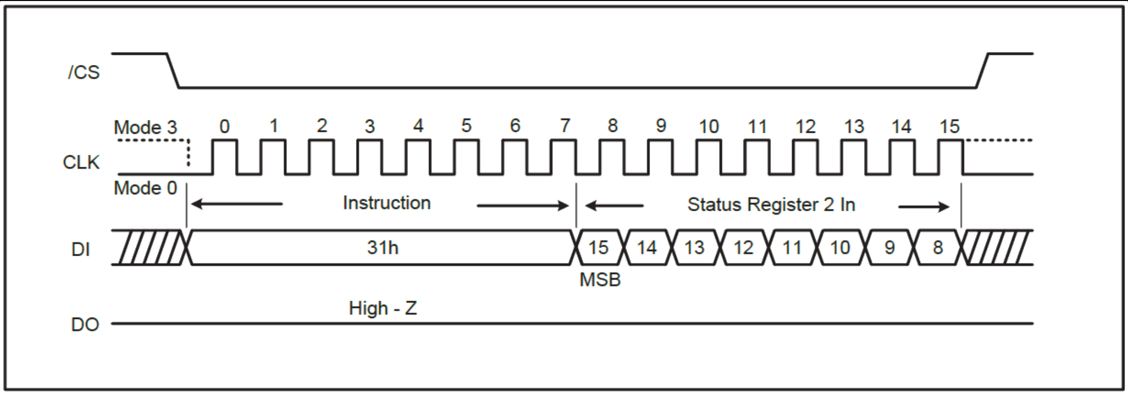


Figure 12a. Write Status Register-2 Instruction

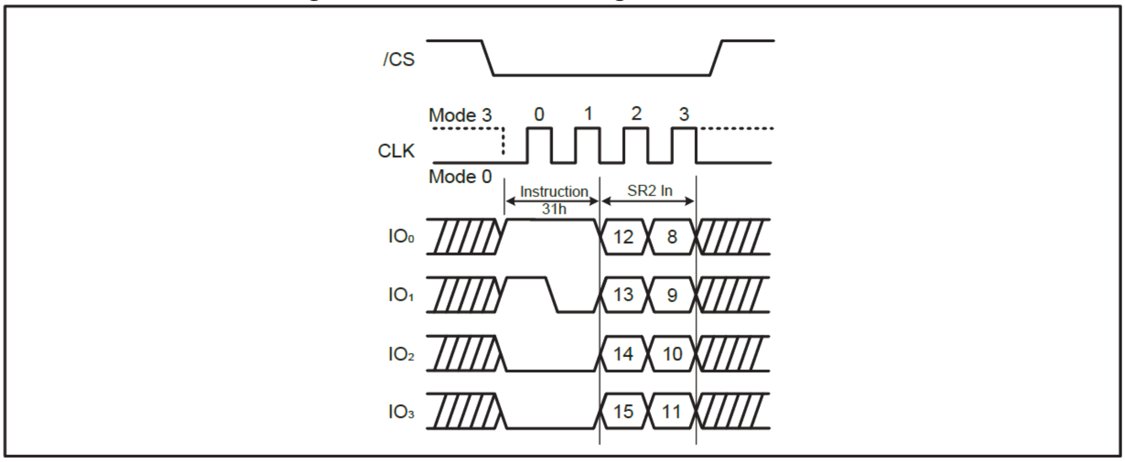


Figure 12b. Write Status Register-2 Instruction (QPI Mode)

8.7 Read Data (Read) (03h)

The Read Data instruction allows one more data bytes to be sequentially read from the memory. The instruction is initiated by driving the CS# pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DIO pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving CS# high.

The Read Data instruction sequence is shown in figure 13. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of fR (see AC Electrical Characteristics).

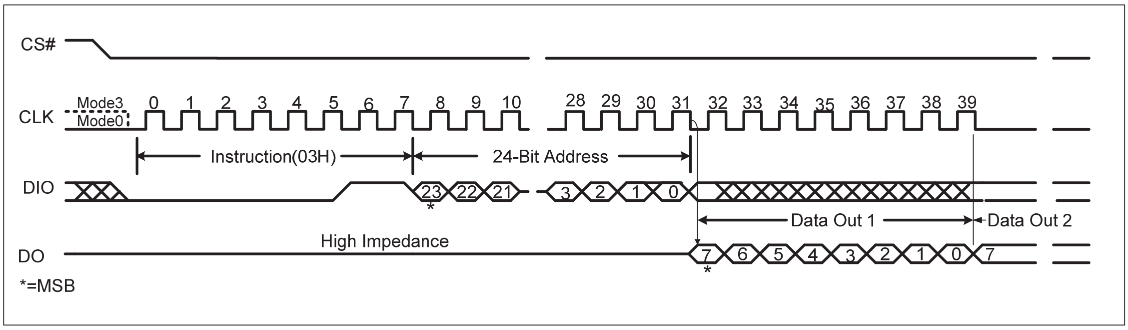


Figure 13. Read Data Instruction Sequence Diagram

8.7 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in figure 14. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the DIO pin is a “don’t care”.

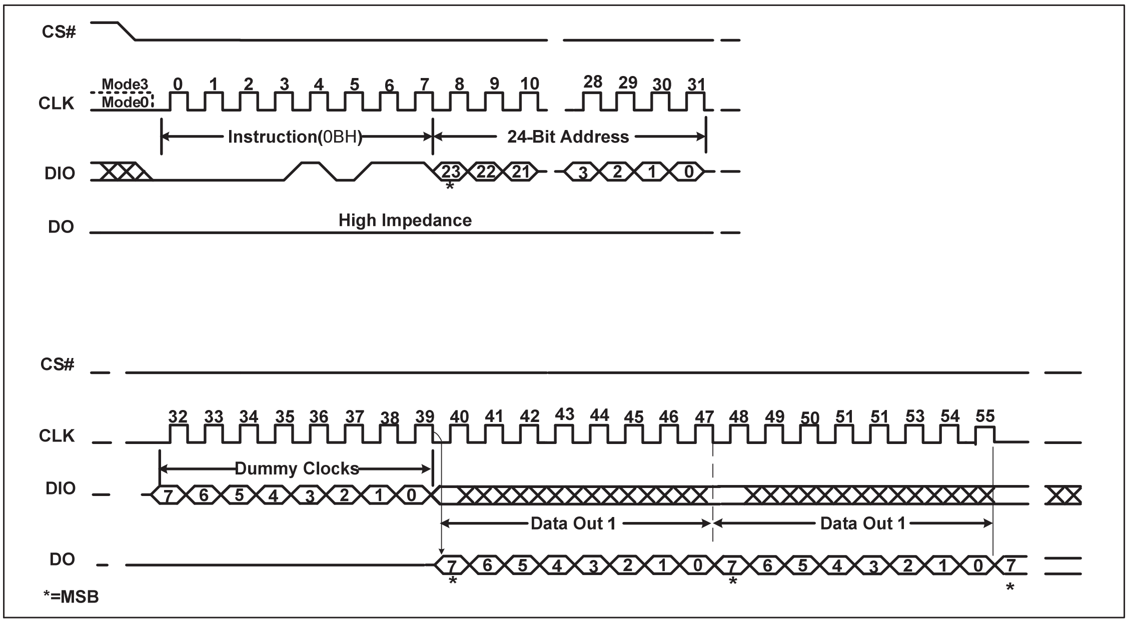


Figure 14a, Fast Read Instruction Sequence Diagram

Fast Read in QPI Mode

When QPI mode is enabled, the number of dummy clock is configured by the “Set Read Parameters (C0h)” instruction to accommodate wide range applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bit P[4]and P[5]setting, the number of dummy clocks can be configured as either 4, 6 or 8. The default number of dummy clocks upon power up or after a Reset instruction is 4.(Please refer to figure 14b, 14c, 14d).

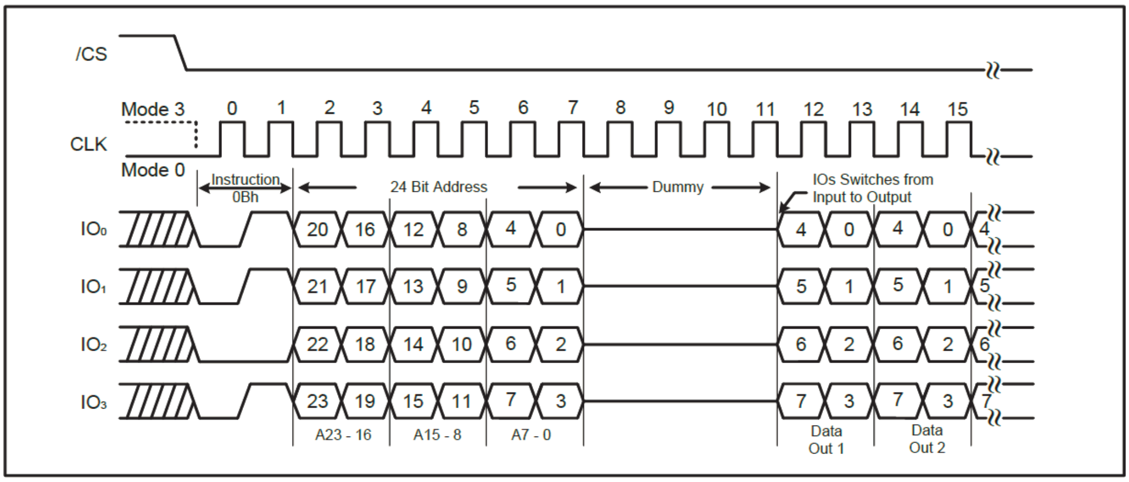


Figure 14b. Fast Read instruction (QPI Mode, 80MHz)

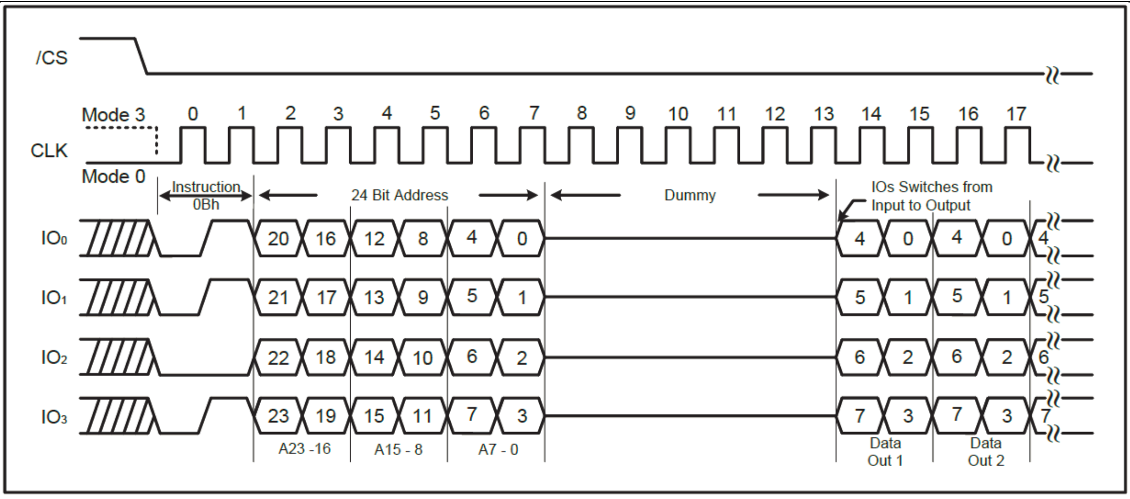


Figure 14c. Fast Read instruction (QPI Mode, 108MHz)

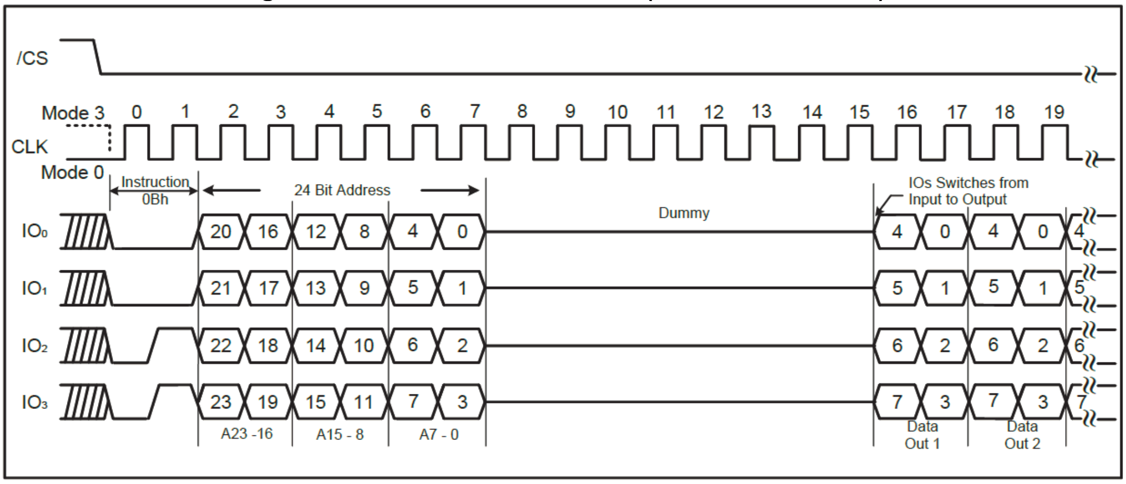


Figure 14d. Fast Read instruction (QPI Mode, 133MHz)

8.8 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins, DO and DIO, instead of just DO. This allows data to be transferred from the ZD25LQ64 at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in figure 15. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the DIO pin should be high-impedance prior to the falling edge of the first data out clock.

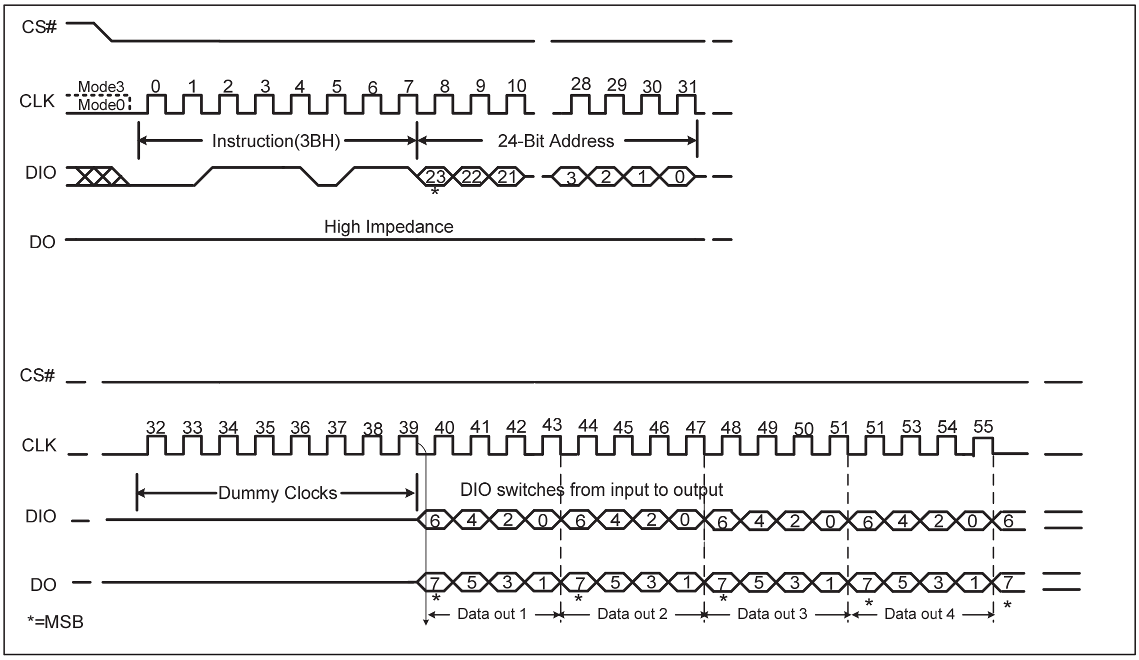


Figure 15, Fast Read Dual Output Instruction Sequence Diagram

8.9 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO_0, IO_1, IO_2, and IO_3. The Fast Read Quad Output Instruction allows data to be transferred from the ZD25LQ at four times the rate of standard SPI devices. The Fast Read Quad Output instruction can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in Figure 16. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

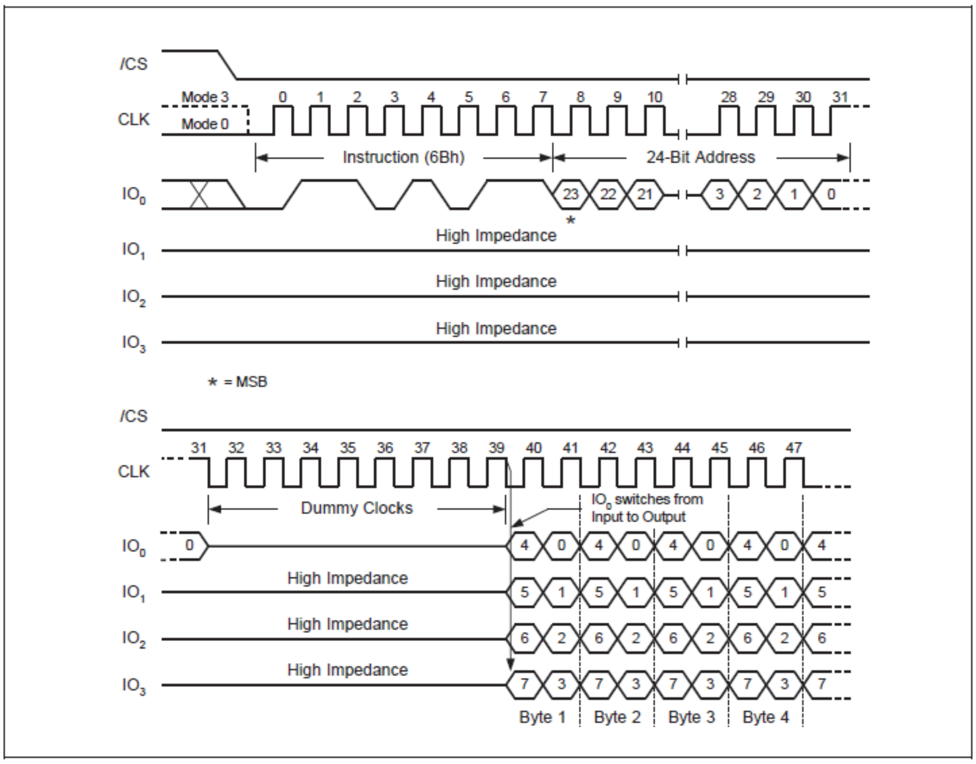


Figure 16, Fast Read Quad Output Instruction Sequence Diagram

8.10 Fast Read Dual I/O (BBh)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in followed Figure17. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Dual I/O Fast Read with “Continuous Read Mode”

The Dual I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-4) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in followed Figure18. If the “Continuous Read Mode” bits (M5-4) do not equal (1, 0), the next command requires the first BBH command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M5-4) before issuing normal command.

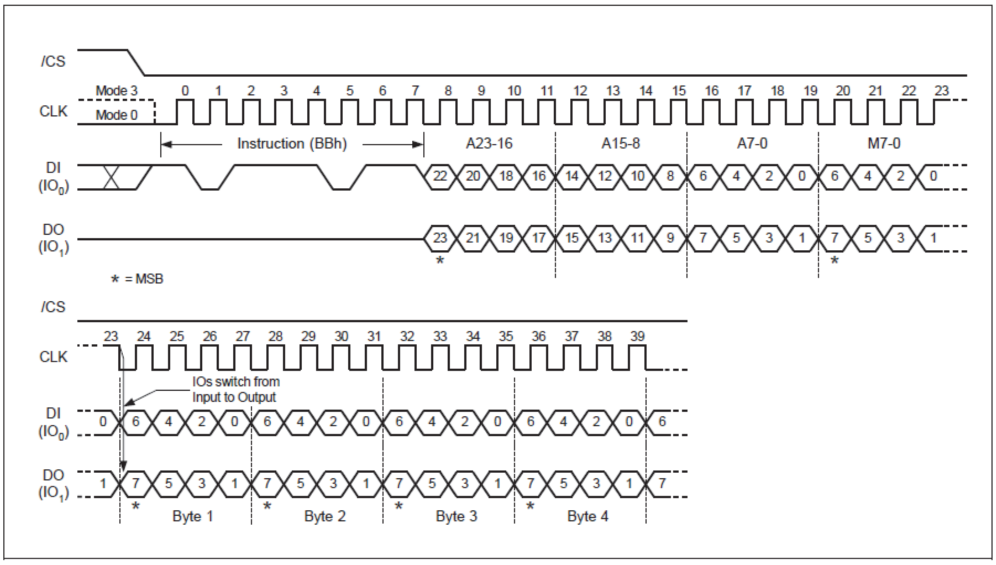


Figure 17, Dual I/O Fast Read Sequence Diagram (M5-4 ≠ (1, 0))

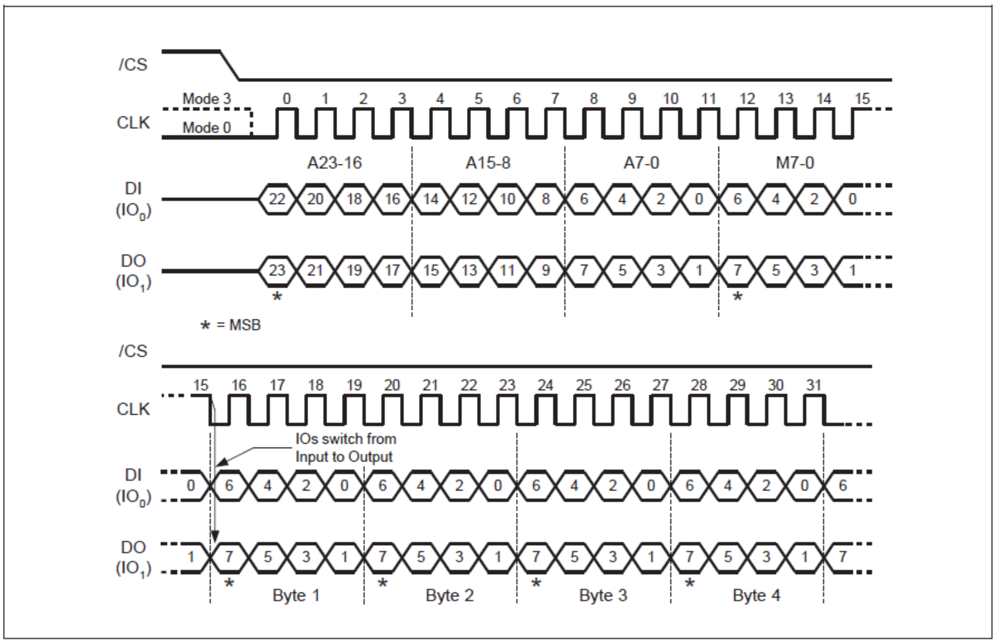


Figure 18, Dual I/O Fast Read Sequence Diagram (M5-4 = (1, 0))

8.11 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

Fast Read Quad I/O with "Continuous Read Mode"

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in Figure 19. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1, 0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown in Figure 20. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1, 0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

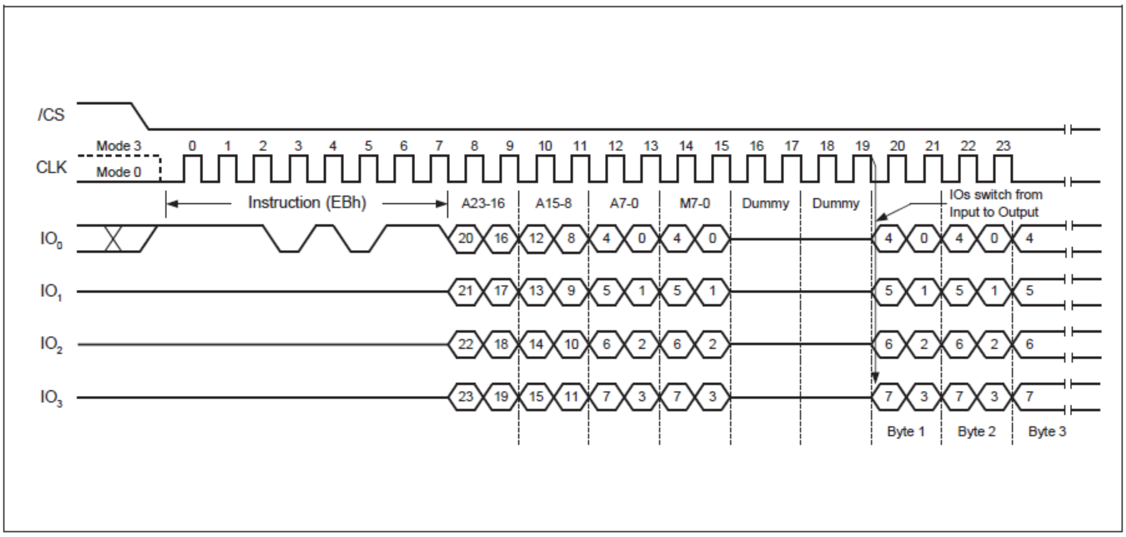


Figure 19, Quad I/O Fast Read Sequence Diagram (M5-4 ≠ (1, 0))

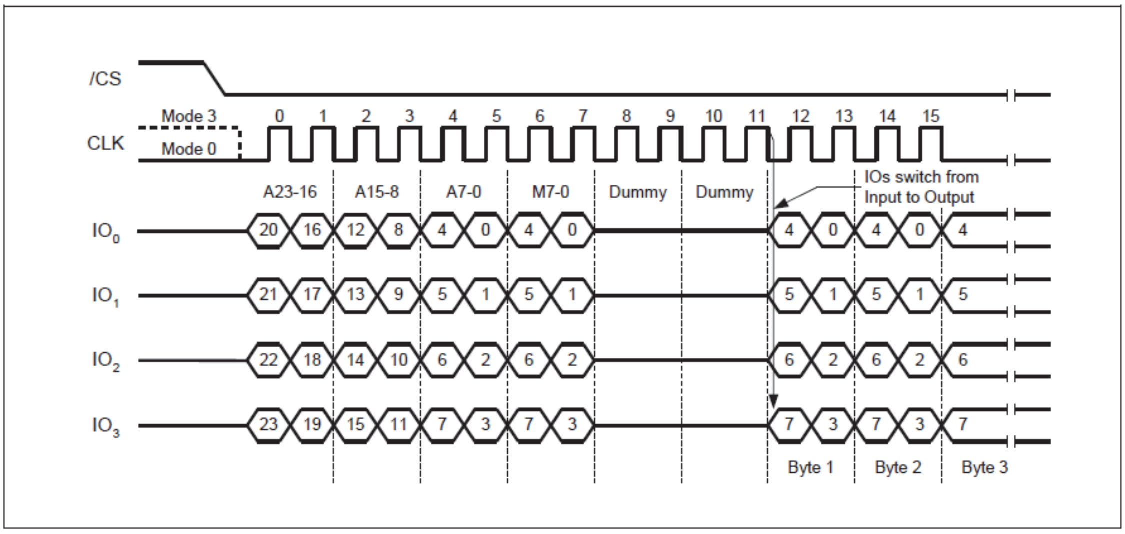


Figure 20, Quad I/O Fast Read Sequence Diagram (M5-4 = (1, 0))

Quad I/O Fast Read with “8/16/32/64-Byte Wrap Around” in Standard SPI mode

The Quad I/O Fast Read command can be used to access a specific portion within a page by issuing “Set Burst with Wrap” (77H) commands prior to EBH. The “Set Burst with Wrap” (77H) command can either enable or disable the “Wrap Around” feature for the following EBH commands. When “Wrap Around” is enabled, the data being accessed can be limited to either an8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The “Set Burst with Wrap” command allows three “Wrap Bits” W6-W4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-W5 is used to specify the length of the wrap around section within a page.

8.12 Quad I/O Word Fast Read (E7H)

The Quad I/O Word Fast Read command is similar to the Quad I/O Fast Read command except that the lowest address bit (A0) must equal 0 and only 2-dummy clock. The command sequence is shown in followed Figure 21. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Word Fast read command.

Quad I/O Word Fast Read with “Continuous Read Mode”

The Quad I/O Word Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next Quad I/O Word Fast Read command (after CS# is raised and then lowered) does not require the E7H command code. The command sequence is shown in followed Figure 22. If the “Continuous Read Mode” bits (M5-4) do not equal to (1, 0), the next command requires the first E7H command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M5-4) before issuing normal command.

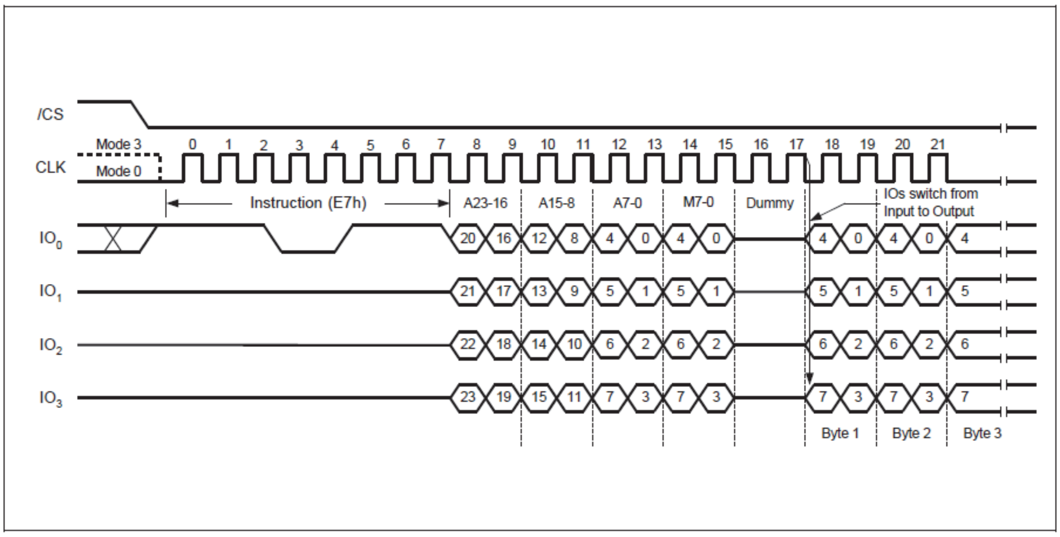


Figure 21, Quad I/O Word Fast Read Sequence Diagram (M5-4≠ (1, 0))

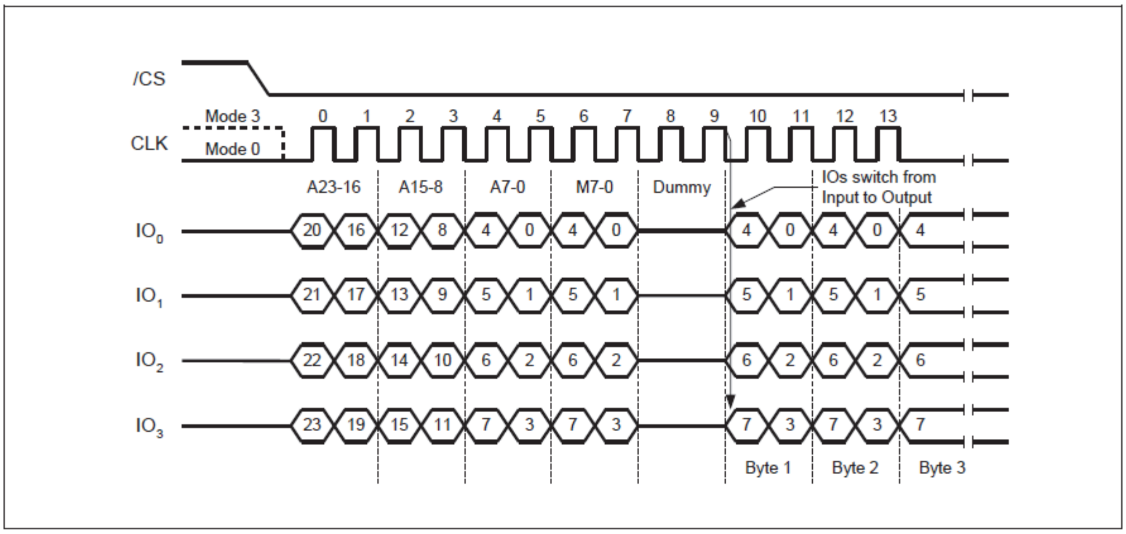


Figure 22, Quad I/O Word Fast Read Sequence Diagram (M5-4= (1, 0))

Quad I/O Word Fast Read with "8/16/32/64-Byte Wrap Around" in Standard SPI mode
The Quad I/O Word Fast Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77H) commands prior to E7H. The "Set Burst with Wrap" (77H) command can either enable or disable the "Wrap Around" feature for the following E7H commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.
The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

8.13 Set Burst with Wrap (77H)
The Set Burst with Wrap command is used in conjunction with "Quad I/O Fast Read" and "Quad I/O Word Fast Read" command to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode.
The Set Burst with Wrap command sequence: CS# goes low ➔ Send Set Burst with Wrap command ➔ Send 24 dummy bits ➔ Send 8 bits "Wrap bits" ➔ CS# goes high.

W6,W5	W4=0		W4=1 (default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0, 0	Yes	8-byte	No	N/A
0, 1	Yes	16-byte	No	N/A
1, 0	Yes	32-byte	No	N/A
1, 1	Yes	64-byte	No	N/A

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following "Quad I/O Fast Read" and "Quad I/O Word Fast Read" command will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1.

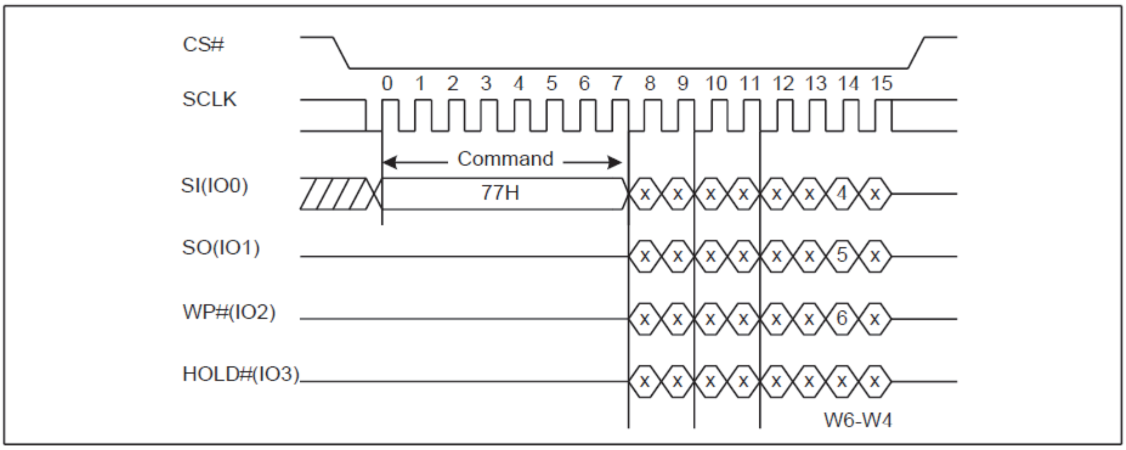


Figure 23. Set Burst with Wrap Sequence Diagram

8.14 Page Program (PP) (02h)

The Page Program instruction allows up to 256 bytes of data to be programmed at previously erased to all 1s (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DIO pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in figure 24.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceed the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks can not exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After CS# is driven high, the self-timed Page Program instruction will commence for a time duration of tpp (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2 - BP0) bits (see Status Register Memory Protection table).

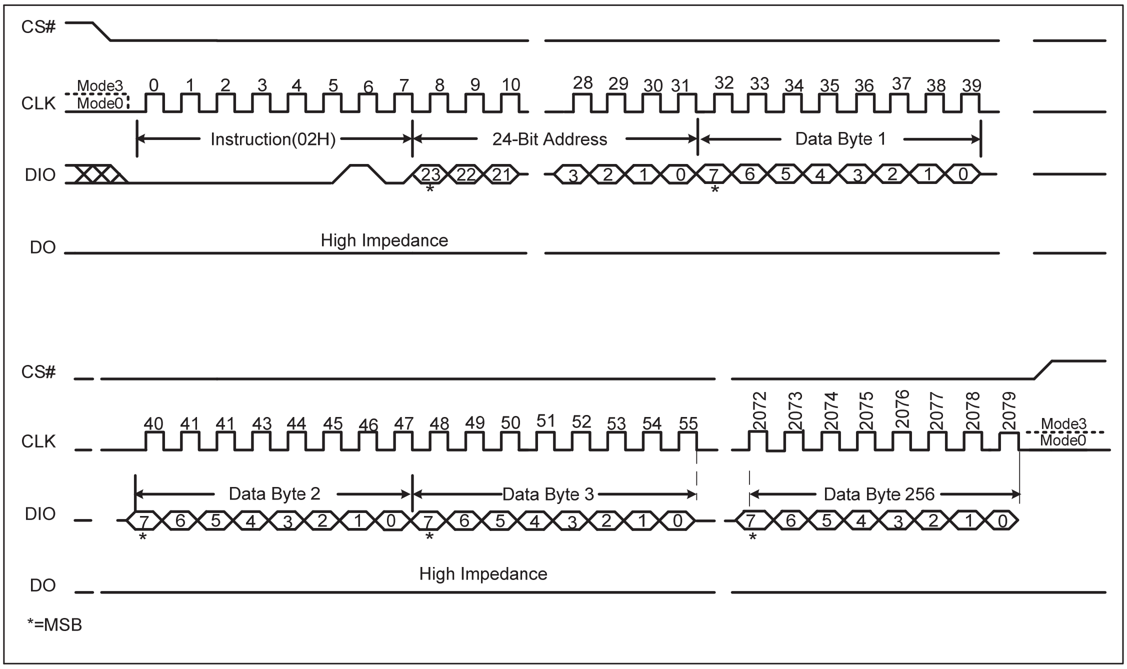


Figure 24a, Page Program Instruction Sequence Diagram

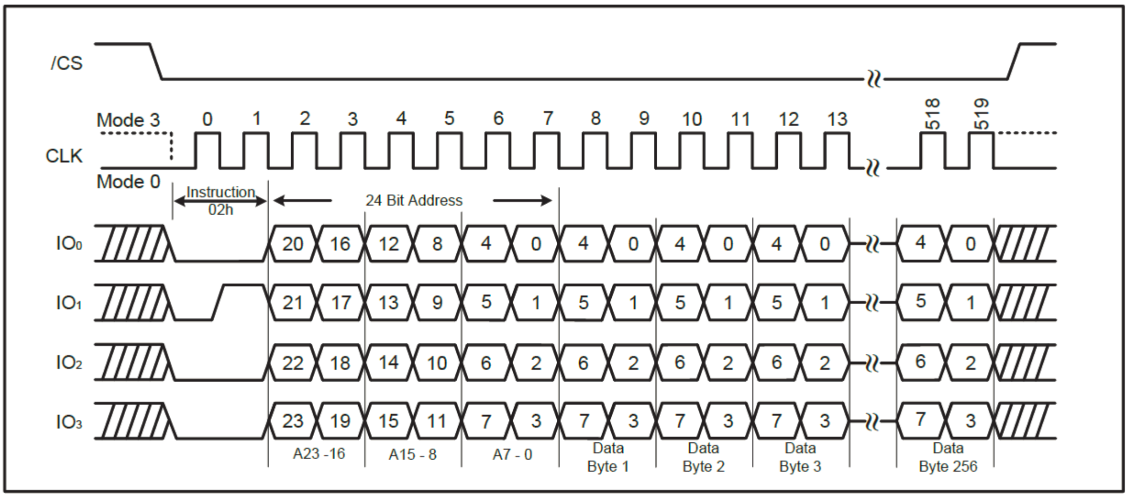


Figure 24b. Page Program Instruction (QPI Mode)

8.15 Quad Input Page Program (33h)

The Quad Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: IO0, IO1, IO2, and IO3. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it take to clock-in the data.

To use Quad Page Program the Quad Enable in Status Register-2 must be set (QE=1). A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “33h” followed by a 24-bit address (A23-A0) and at least one data byte, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The Quad Page Program instruction sequence is shown in Figure 25.

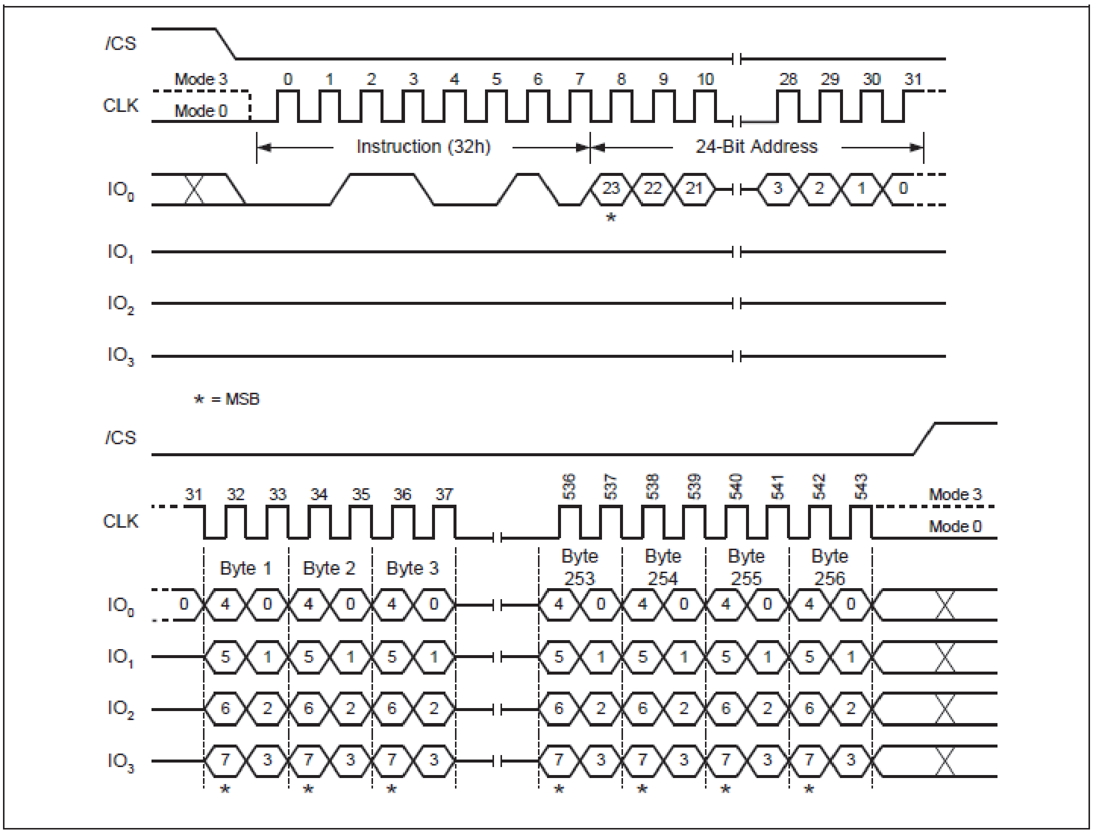


Figure 25a, Quad Page Program Sequence Diagram

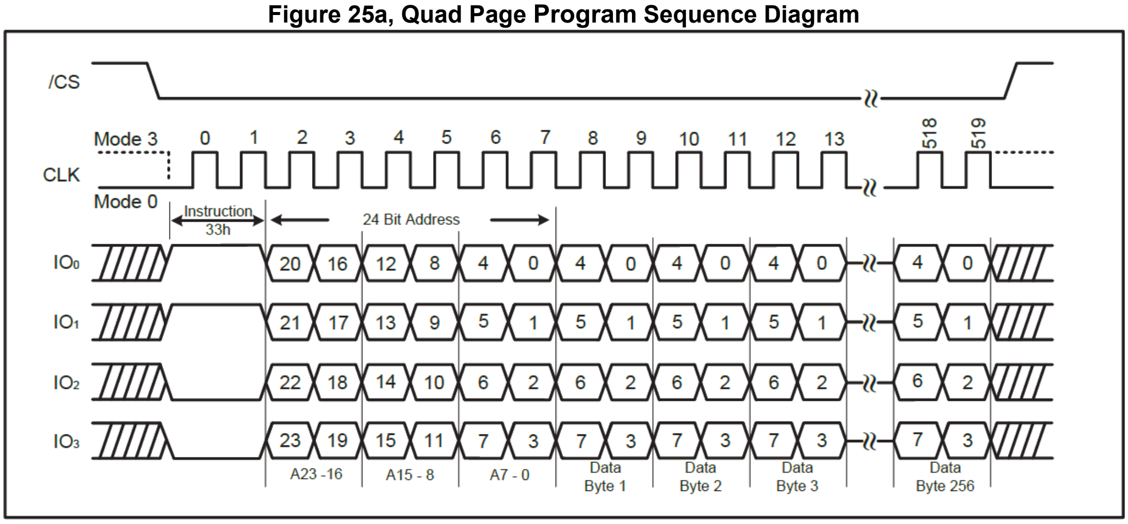


Figure 25b, Quad Page Program Sequence Diagram(QPI mode)

8.16 Sector Erase (SE) (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23-A0) (see Figure 2). The Sector Erase instruction sequence is shown in figure 26.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After CS# is driven high, the self-timed Sector Erase instruction will commence for a time duration of tSE (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2 - BP0) bits (see Status Register Memory Protection table).

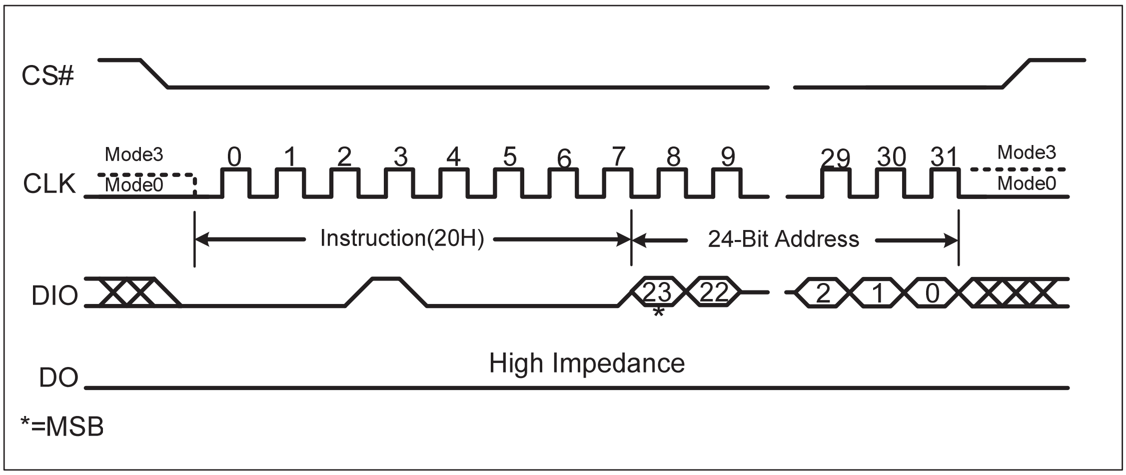


Figure 26a, Sector Erase Instruction Sequence Diagram

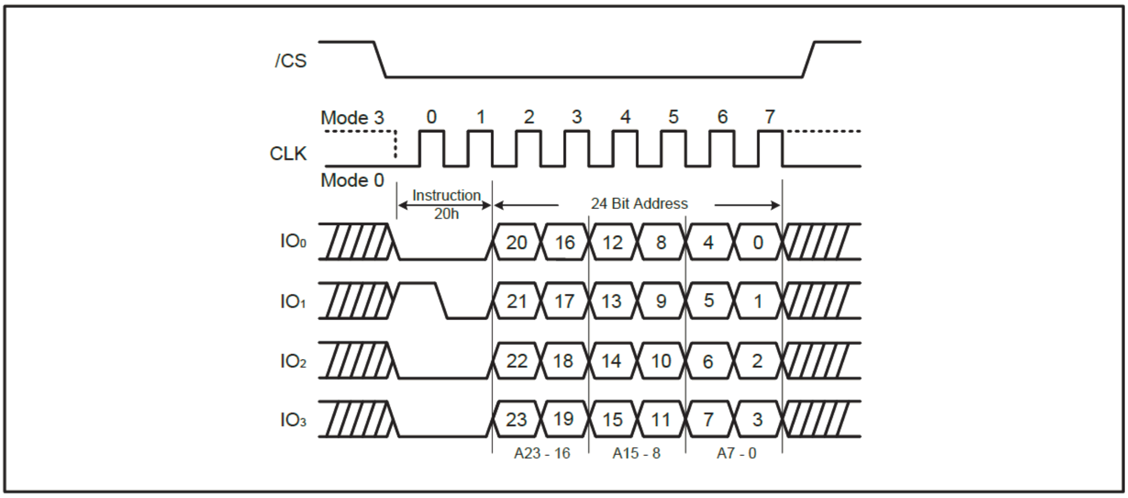


Figure 26b, Sector Erase Instruction Sequence Diagram(QPI Mode)

8.17 Block Erase (BE) (D8h) and Half Block Erase (52h)

The Block Erase instruction sets all memory within a specified block (64K-bytes) or half block (32K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “D8h” or “52h” followed a 24-bit block address (A23-A0) (see Figure 2). The Block Erase instruction sequence is shown in figure 27.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After CS# is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (CMP, SEC, TB, BP2 - BP0) bits (see Status Register Memory Protection table).

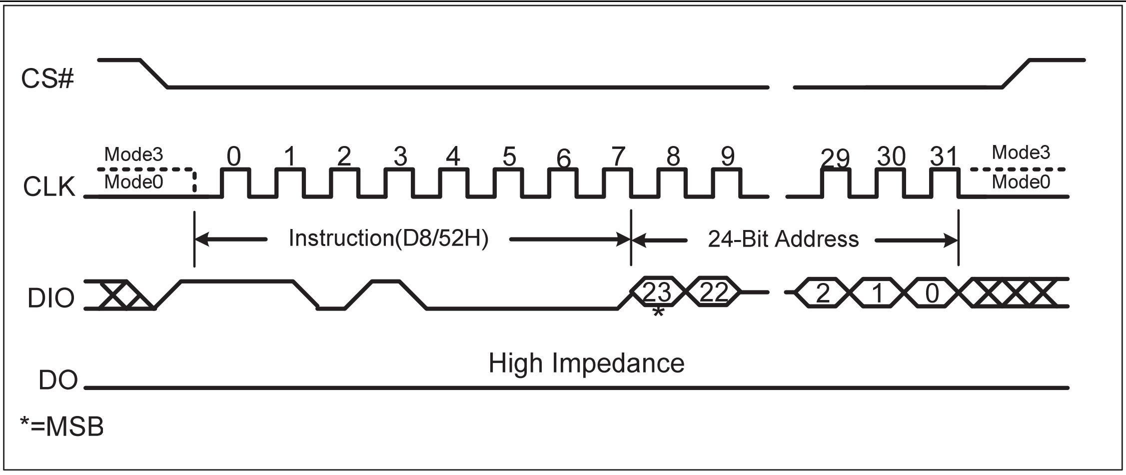


Figure 27a. Block Erase Instruction Sequence Diagram

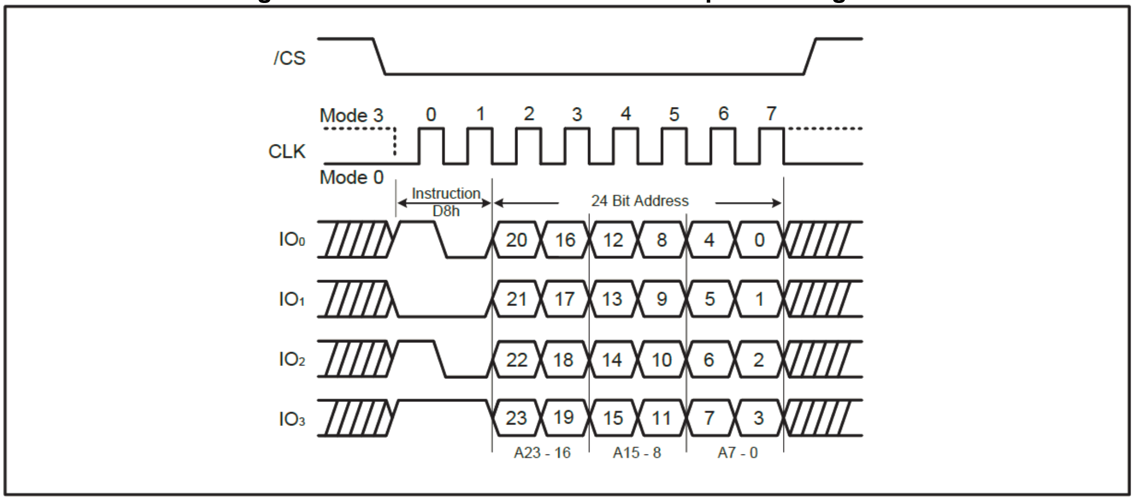


Figure 27b. Block Erase Instruction Sequence Diagram(QPI Mode)

8.18 Chip Erase (CE) (C7h or 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in figure 28.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After CS# is driven high, the self-timed Chip Erase instruction will commence for a time duration of tCE (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any page is protected by the Block Protect (CMP, SEC, TB, BP2 - BP0) bits (see Status Register Memory Protection table).

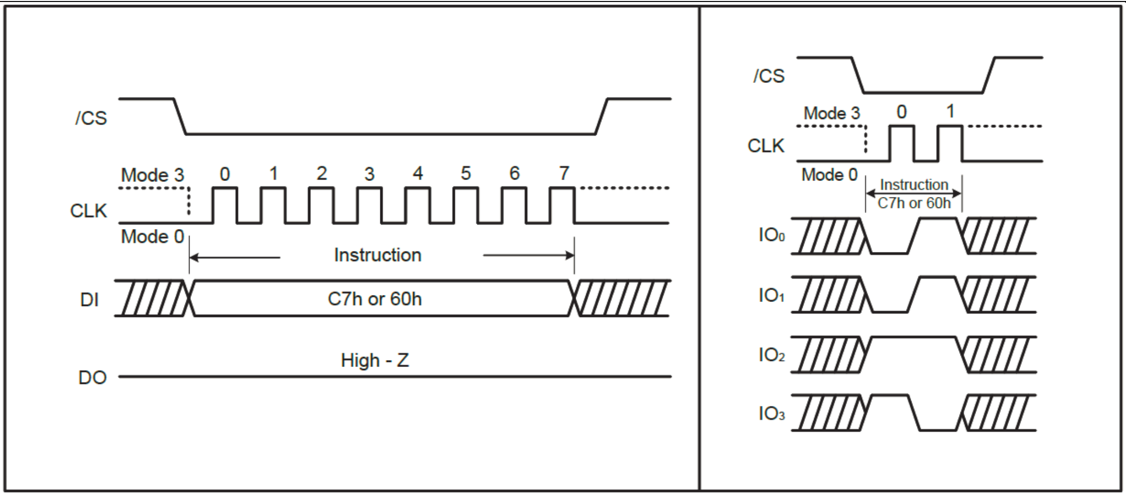


Figure 28, Chip Erase Instruction Sequence Diagram and QPI Mode(right)

8.19 Erase / Program Suspend (75h)

The Erase/Program Suspend instruction allows the system to interrupt a Sector Erase, Block Erase operation or a Page Program, Quad Data Input Page Program, Quad Page Program operation. Erase Suspend is valid only during the Sector or Block erase operation. The Write Status Register-1(01h), Write Status Register-2 (31h) instruction and Erase instructions (20h, 52h, D8h, C7h, 60h) are not allowed during Erase Suspend. During the Chip Erase operation, the Erase Suspend instruction is ignored.
Program Suspend is valid only during the Page Program, Quad Data Input Page Program or Quad Page Program operation. The Write Status Register-1(01h), Write Status Register-2 (31h) instruction and Program instructions (02h and 33h) are not allowed during Program Suspend.

The Erase/Program Suspend instruction “75h” will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction will be ignored by the device. A maximum of time of “tSUS” (See AC Characteristics) is required to suspend the erase or program operation. After Erase/Program Suspend, the SUS bit in the Status Register will be set from 0 to 1 immediately and The BUSY bit in the Status Register will be cleared from 1 to 0 within “tSUS”. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction “75h” is not issued earlier than a minimum of time of “tSUS” following the preceding Resume instruction “7Ah”.

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during erase/program suspend state.

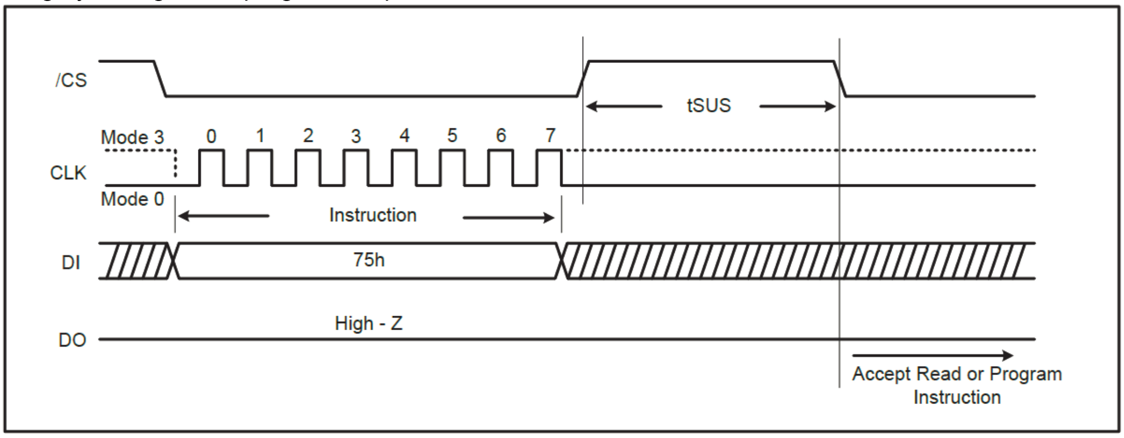


Figure 29a. Erase Suspend instruction

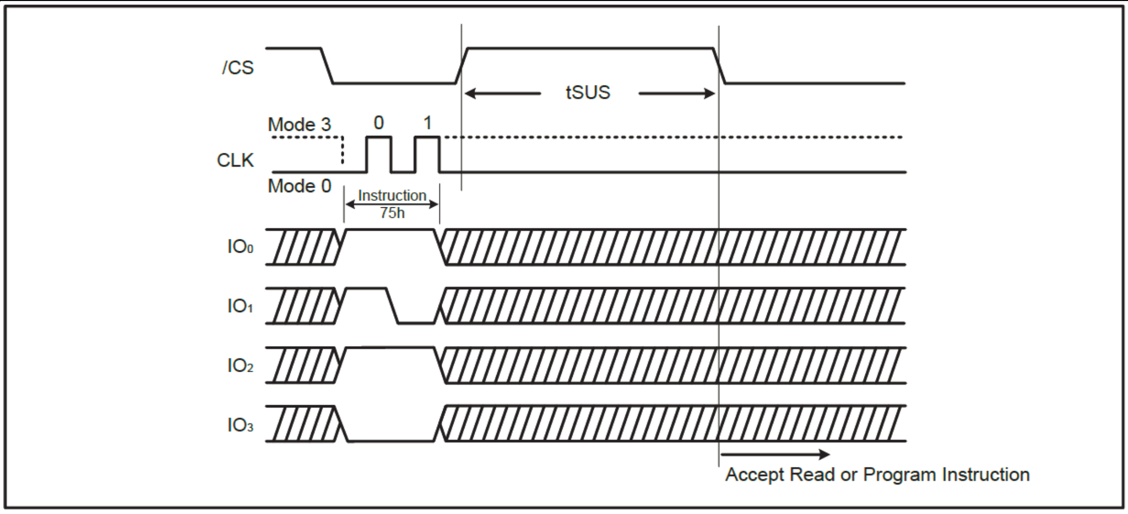


Figure 29b. Erase Suspend instruction (QPI Mode)

8.20 Erase / Program Resume (7Ah)

The Erase/Program Resume instruction "7Ah" is to re-work the Sector or Block Erase operation or the Page Program operation upon an Erase/Program Suspend. The Resume instruction "7Ah" will be accepted by the device only if the SUS bit in the Status Register equals to1 and the BUSY bit equals to 0. After issued, the SUS bit will be cleared from 1 to 0 immediately, the BUSY bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume instruction "7Ah" will be ignored by the device.

Resume instruction cannot be accepted if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of "tSUS" following a previous Resume instruction.

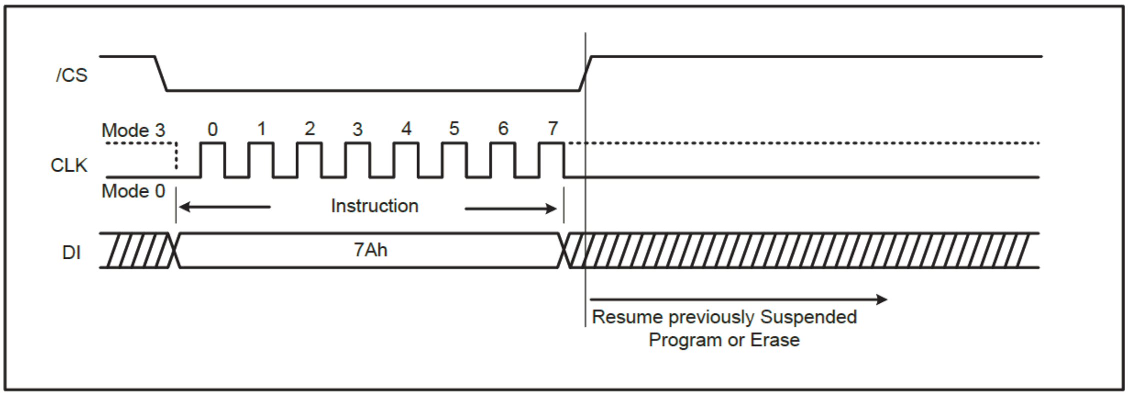


Figure 30a. Erase / Program Resume instruction

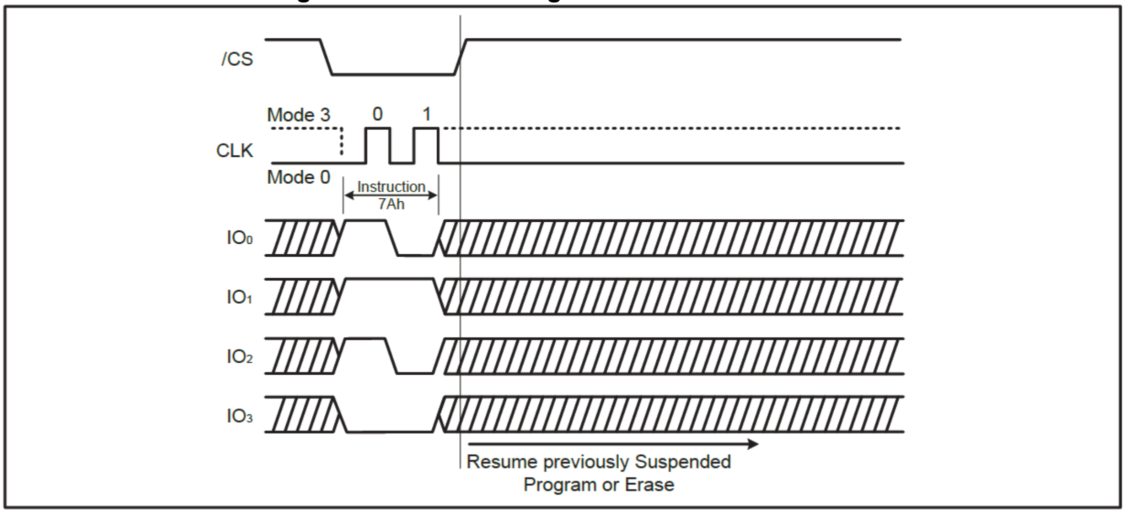


Figure 30b. Erase / Program Resume instruction(QPI Mode)

8.19 Deep Power-down (DP) (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the CS# pin low and shifting the instruction code "B9h" as shown in figure 31.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After CS# is driven high, the power-down state will enter within the time duration of tDP (See AC Characteristics). While in the power-down state only the Release from Power-down / Device ID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

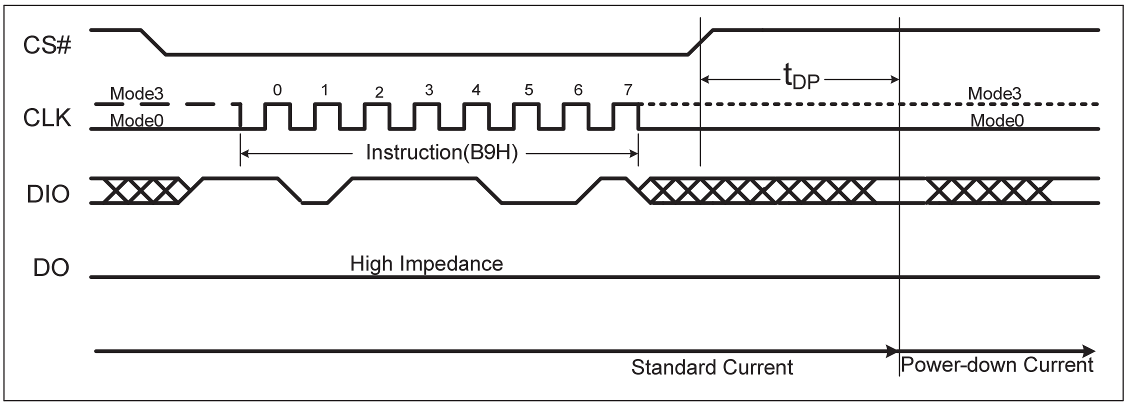


Figure 31a, Deep Power-down Instruction Sequence Diagram

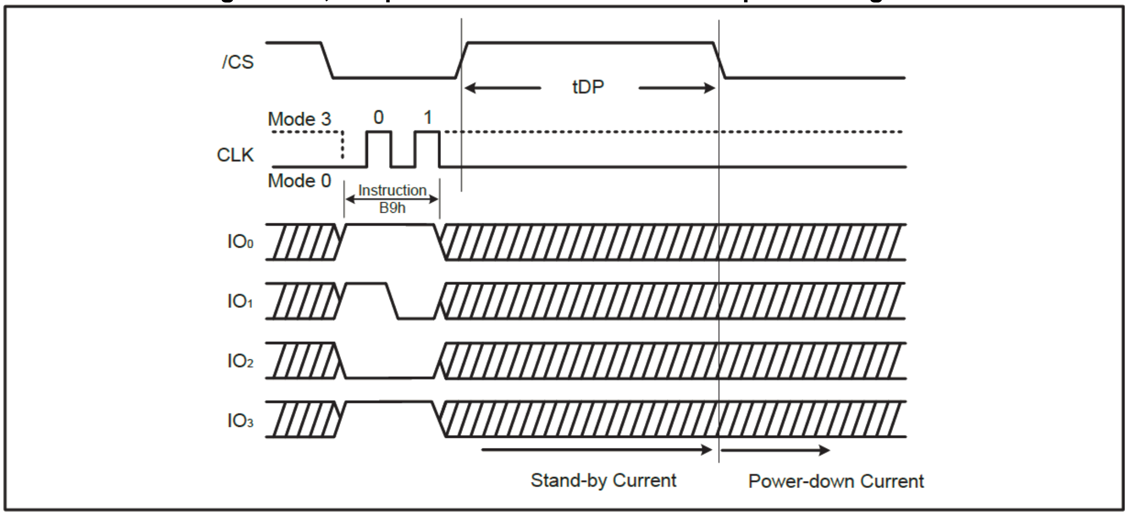


Figure 31b, Deep Power-down Instruction Sequence Diagram (QPI Mode)

8.20 Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, obtain the devices electronic identification (ID) number or do both.

When used only to release the device from the power-down state, the instruction is issued by driving the CS# pin low, shifting the instruction code "ABh" and driving CS# high as shown in figure 32a. After the time duration of tRES1 (See AC Characteristics) the device will resume normal operation and other instructions will be accepted. The CS# pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the CS# pin low and shifting the instruction code "ABh" followed by 3-dummy bytes. The

Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 32b. The Device ID value for the ZD25LQ64 is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving CS# high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in figure 32c, except that after CS# is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume normal operation and other instructions will be accepted. If the Release from Power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and will not have any effects on the current cycle.

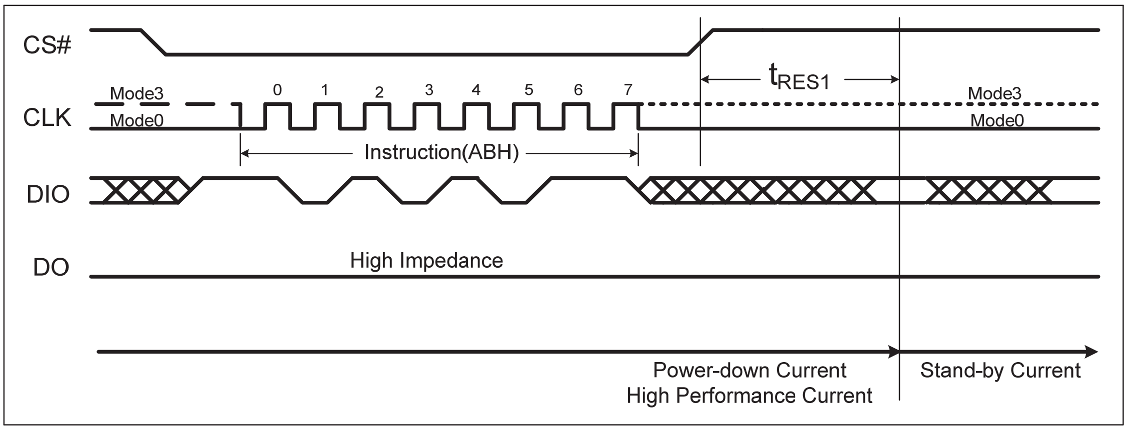


Figure 32a, Release Power-down Instruction Sequence

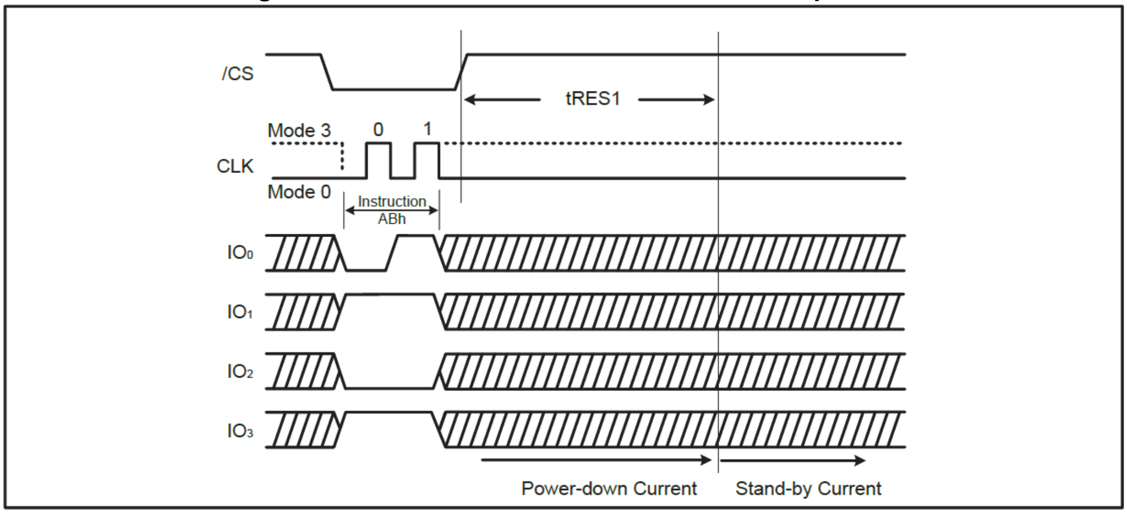


Figure 32b, Release Power-down Instruction Sequence (QPI Mode)

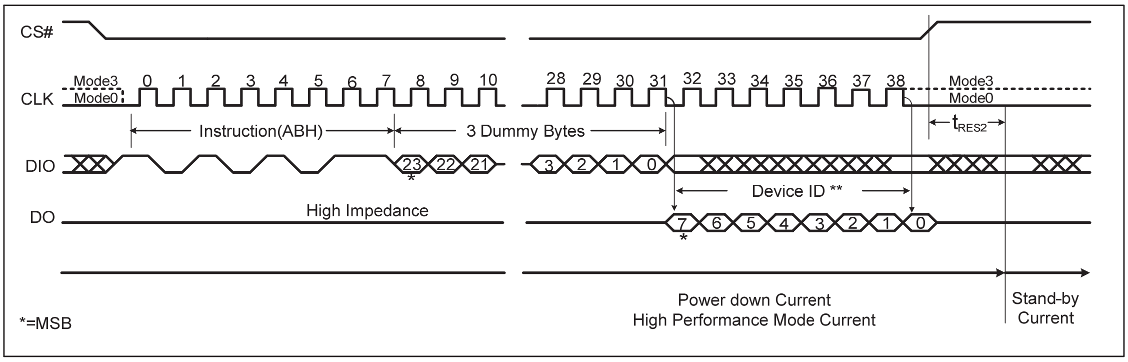


Figure 32c, Release Power-down / Device ID Instruction Sequence Diagram

8.21 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down /Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code "90h" followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Zetta Device (XXh) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 33. The Device ID values for the ZD25LQ64 are listed in Table 2. If the 24-bit address is initially set to 000001h the Device ID will be read first.

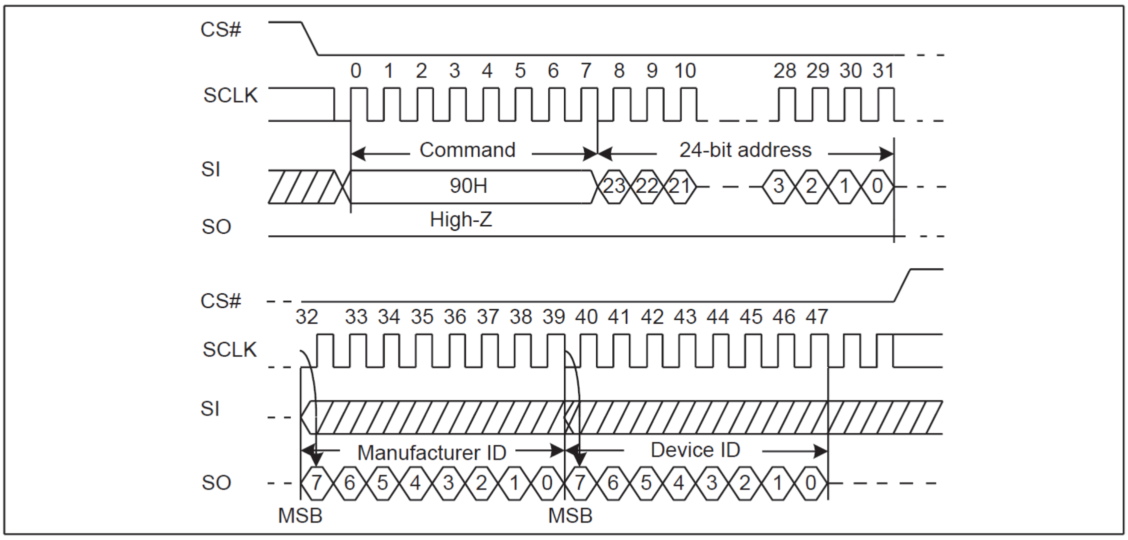


Figure 33a, Read Manufacturer / Device ID Diagram

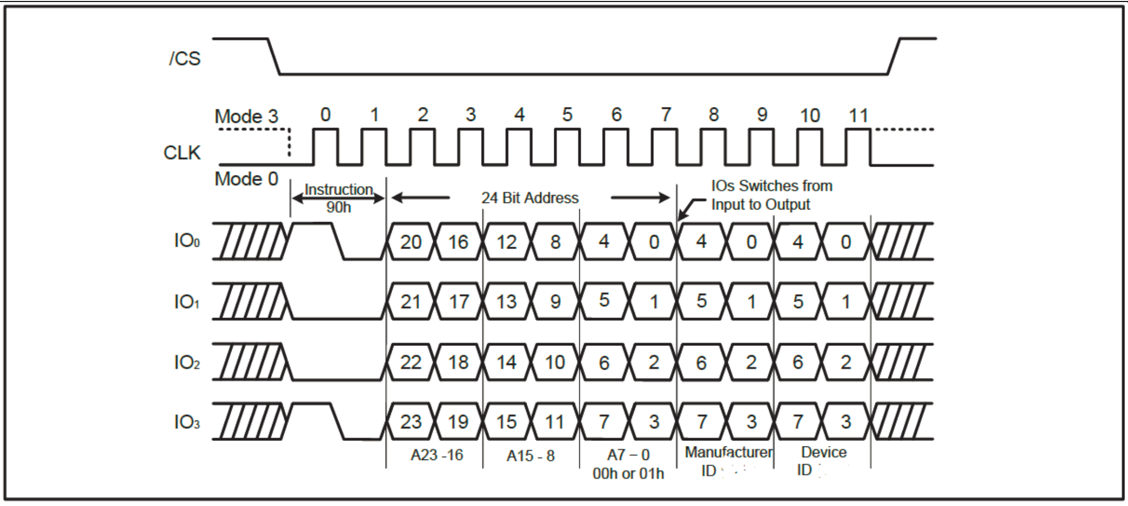


Figure 33b, Read Manufacturer / Device ID Diagram (QPI Mode)

8.22 Read Identification (RDID) (9Fh)

For compatibility reasons, the ZD25LQ64 provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003.

The instruction is initiated by driving the CS# pin low and shifting the instruction code "9Fh". The JEDEC assigned Manufacturer ID byte for Zetta Device (XXh) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 34. For memory type and capacity values refer to Manufacturer and Device Identification table.

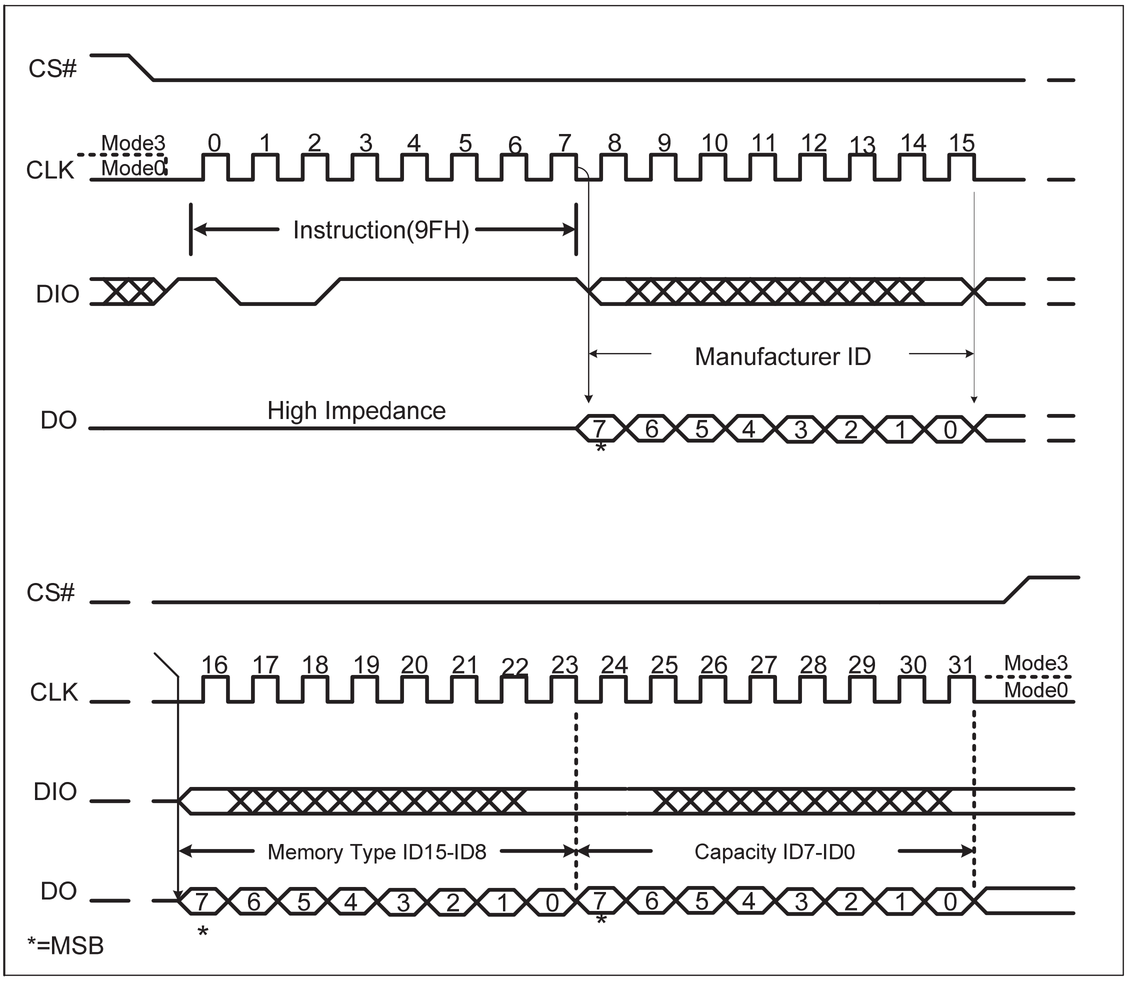


Figure 34a, Read JEDEC ID instruction Sequence Diagram

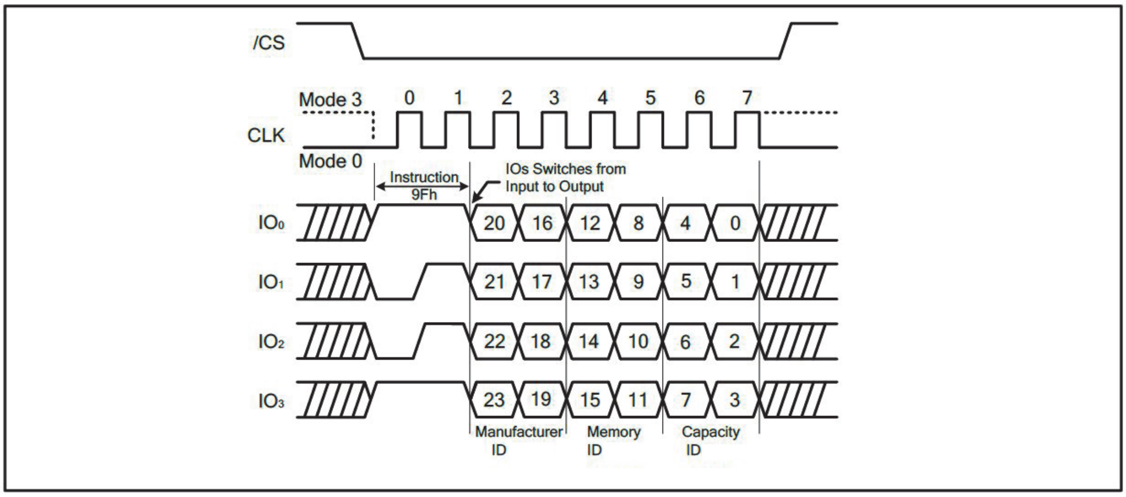


Figure 34b, Read JEDEC ID instruction Sequence Diagram (QPI Mode)

8.23 Enable QPI (38h)

The ZD25LQ64 support both Standard/Dual/Quad Serial Peripheral interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode cannot be used at the same time. Enable QPI instruction is the only way to switch the device from SPI mode to QPI mode.

In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register 2 must be set to 1 first, and an Enable QPI instruction must be issued. If the Quad Enable (QE) bit is 0, the Enable QPI instruction will be ignored and the device will remain in SPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

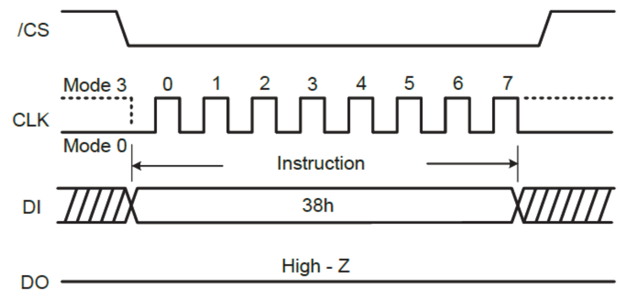


Figure 35, Enable QPI instruction

8.24 Disable QPI (FFh)

By issuing Disable QPI (FFh) instruction, the device is reset SPI mode. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

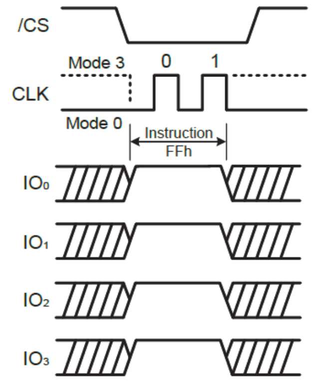


Figure 36. Disable QPI instruction for QPI mode

8.25 Burst Read with Wrap (0Ch)

The "Burst Read with Wrap (0Ch)" instruction provides an alternative way to perform the read operation with "Wrap Around" in QPI mode. The instruction is similar to the "Fast Read (0Bh)" instruction in QPI mode, except the addressing of the read operation will "Wrap Around" to the beginning boundary of the "Wrap Length" once the ending boundary is reached.

The "Wrap Length" and the number of dummy of clocks can be configured by the "Set Read Parameters (C0h)" instruction.

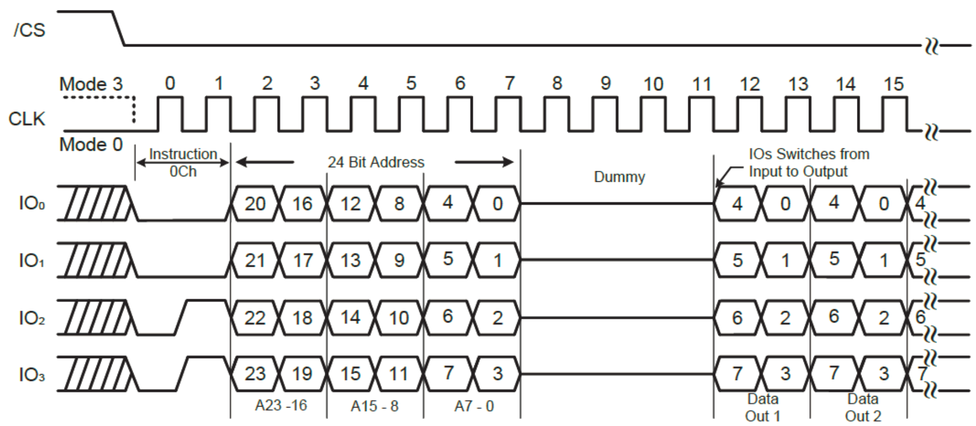


Figure 37a. Burst Read with Wrap instruction (QPI Mode, 80MHz)

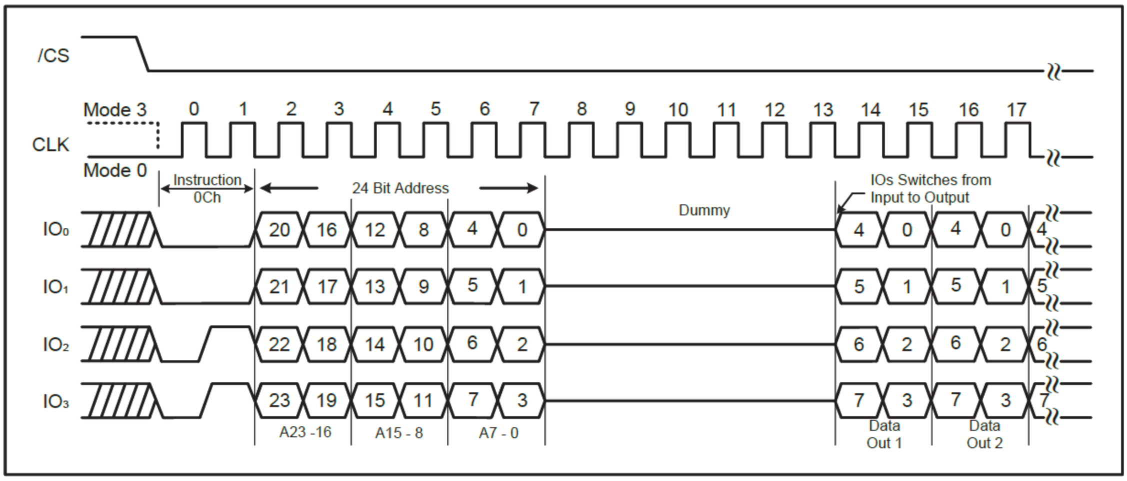


Figure 37b. Burst Read with Wrap instruction (QPI Mode, 108MHz)

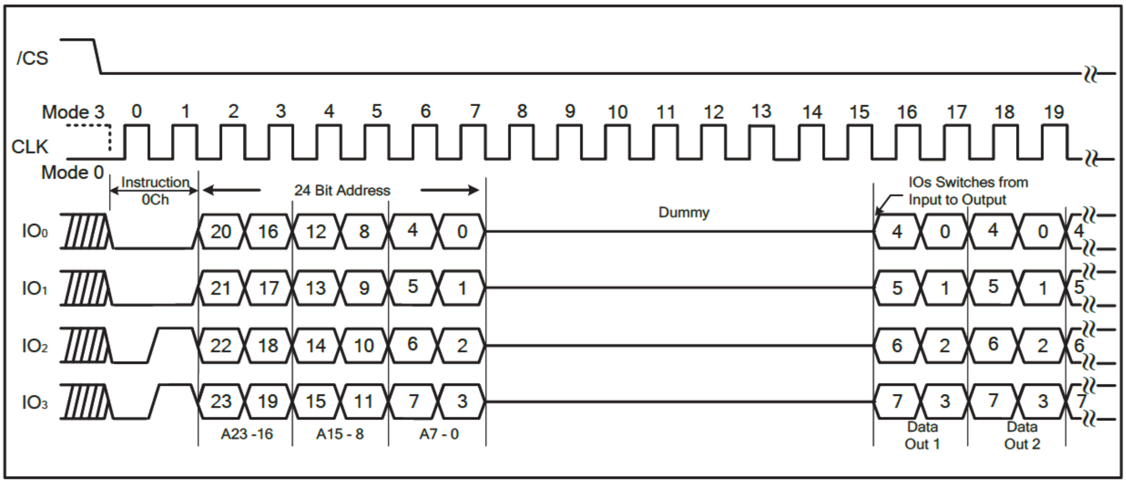


Figure 37c. Burst Read with Wrap instruction (QPI Mode, 133MHz)

8.24 Set Read Parameters (C0h)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, "Set Read Parameters (C0h)" instruction can be used to configure the number of dummy clocks for "Fast Read (0Bh)", "Fast Read Quad I/O (EBh)" & "Burst Read with Wrap (0Ch)" instructions, and to configure the number of bytes of "Wrap Length" for the "Burst Read with Wrap (0Ch)" instruction.

In Standard SPI mode, the "Set Read Parameters (C0h)" instruction is not accepted. The dummy clocks for various Fast Read instructions in Standard/Dual/Quad SPI mode are fixed, please refer to the instruction. Table for details. The "Wrap Length" is set by W6-5 bit in the "Set Burst with Wrap (77h)" instruction. This setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.

The default "Wrap Length" after a power up or a Reset instruction is 8 bytes, the default number of dummy clocks is 4.

P5, P4	Dummy Clocks	Maximum Read Freq.		P1, P0	Wrap Length
0 0	4	80MHz		0 0	8-byte
0 1	4	80MHz		0 1	16-byte
1 0	6	108MHz		1 0	32-byte
1 1	8	133MHz		1 1	64-byte

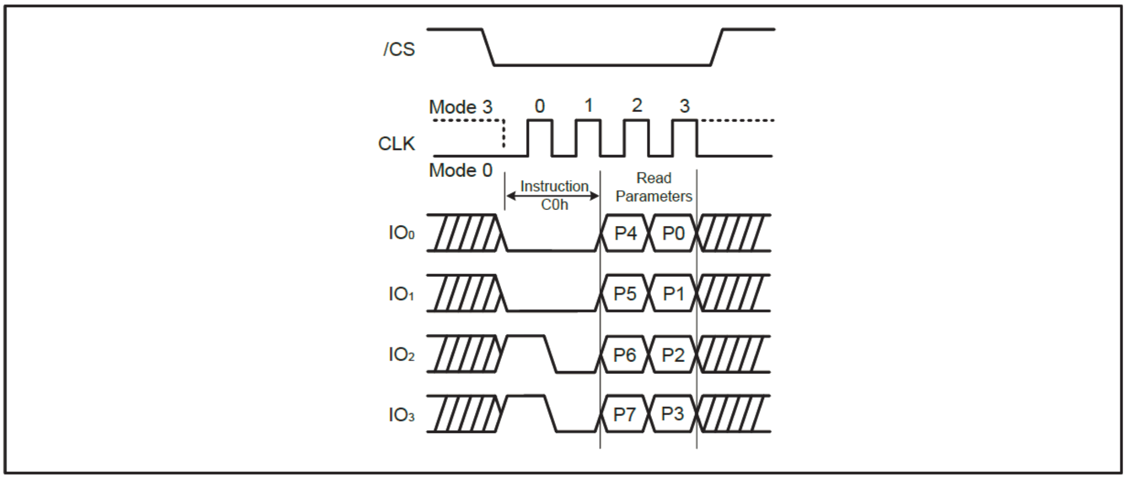


Figure 38. Set Read Parameters instruction (QPI Mode)

8.24 Enable Reset (66h) and Reset (99h)

The ZD25LQ64 provide a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Read parameter setting (P7-P0), Continuous Read Mode bit setting (M7-M0) and Wrap Bit setting (W6-W4).
"Enable Reset (66h)" and "Reset (99h)" instructions can be issued in SPI mode. To avoid accidental reset, both instructions must be issued in sequence. Any other commands other than "Reset (99h)" after the "Enable Reset (66h)" command will disable the "Reset Enable" state. A new sequence of "Enable Reset (66h)" and "Reset (99h)" is needed to reset the device. Once the Reset command is accepted by the device, the device will take approximately tRST=30us to reset. During this period, no command will be accepted.
Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

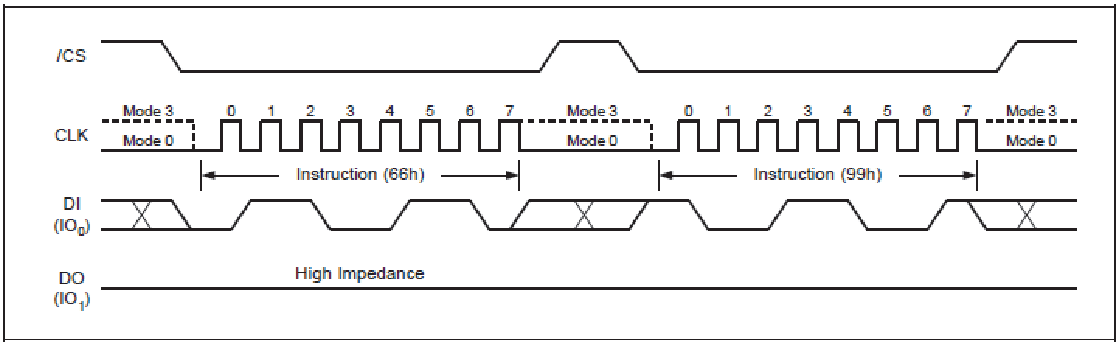


Figure 39a. Enable Reset and Reset command Sequence Diagram

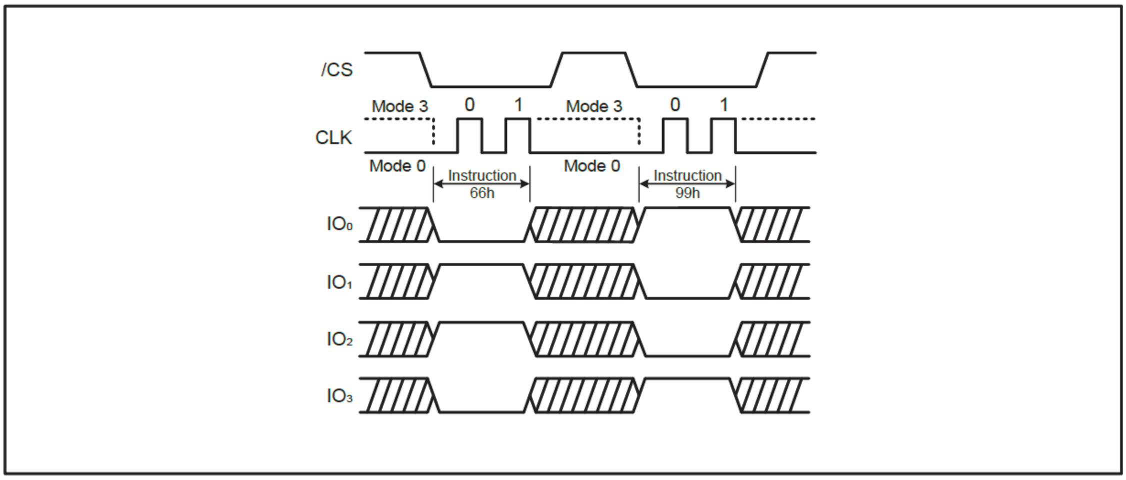


Figure 39b. Enable Reset and Reset Instruction (QPI Mode)

8.25 Enter Secured OTP (B1h)

The Enter Secured OTP instruction is for entering the additional 4K-bit secured OTP mode. The additional 4K-bit secured OTP is independent from main array, which may be used to store unique serial number for system identifier. After entering the Secured OTP mode, and then follow standard read or program, procedure to read out the data or update data. The Secured OTP data cannot be updated again once itis lock-down

Please note that Write Status Register-1, Write Status Register-2 and Write Security Register instructions are not acceptable during the access of secure OTP region. Once security OTP is lock down, only commands related with read are valid.

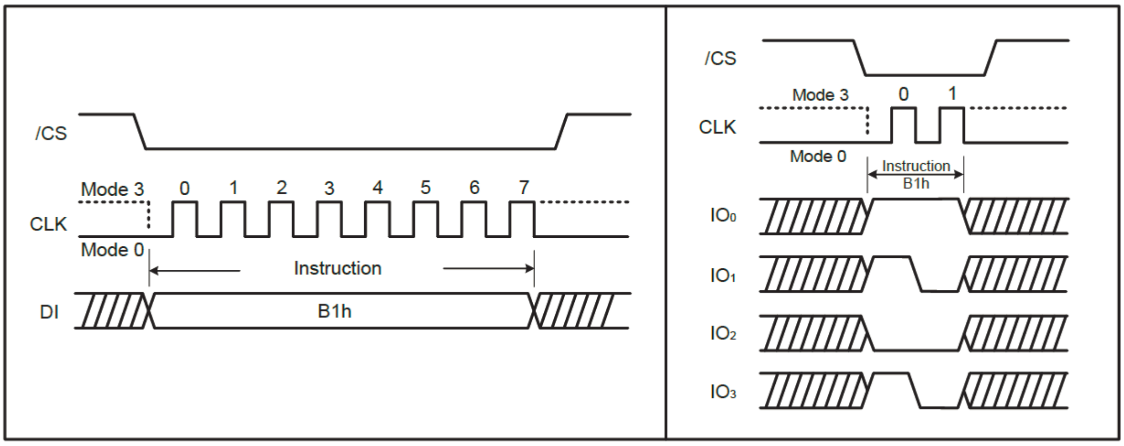


Figure 40. Enter Secured OTP instruction for SPI Mode and QPI Mode (right)

8.26 Exit Secured OTP (C1h)

The Exit Secured OTP instruction is for exiting the additional 4K-bit secured OTP mode.

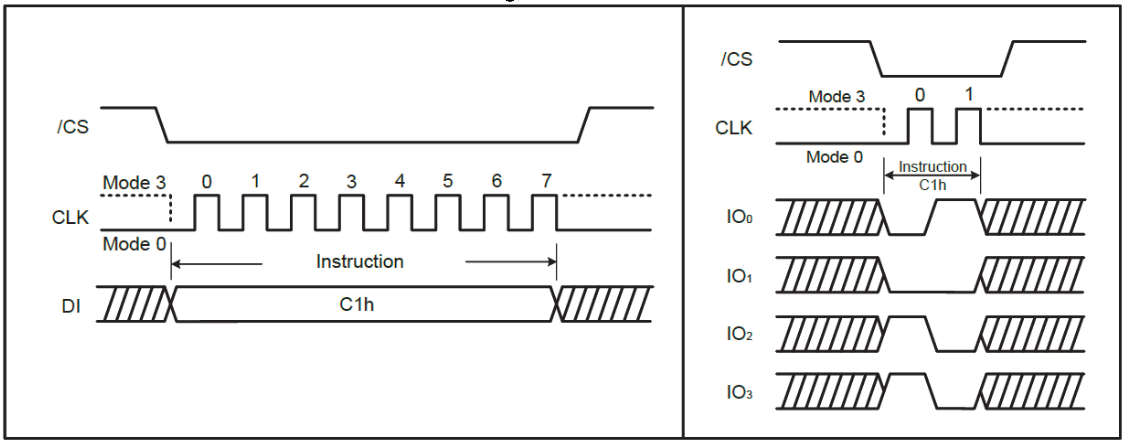


Figure 41. Exit Secured OTP instruction for SPI Mode and QPI Mode (right)

8.27 Read Security Register (2Bh)

The Read Security Register can be read the value of Security Register bits at any time (even in program/erase/write status register-1 and write status register-2 condition) and continuously.

Secured OTP Indicator bit. The Secured OTP indicator bit shows the chip is locked by factory before ex-factory or not. When it is "0", it indicates non-factory lock, "1" indicates factory-lock.

Lock-down Secured OTP (LDSO) bit. By writing Write Security Register instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit it set to "1" (Lock-down), the LDSO bit and the 4K-bit Secured OTP area cannot be updated any more. While it is in 4K-bit Secured OTP mode, array access is not allowed to write.

Security Register Definition

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
x	x	x	x	x	x	LDSO (indicate if lock-down)	Secured OTP indicator bit

reserved	reserved	reserved	reserved	reserved	reserved	0 = not lock-down 1 = lock-down(can not program/erase OTP)	0 = non factory lock 1 = factory lock
Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Non-Volatile bit	Non-Volatile bit

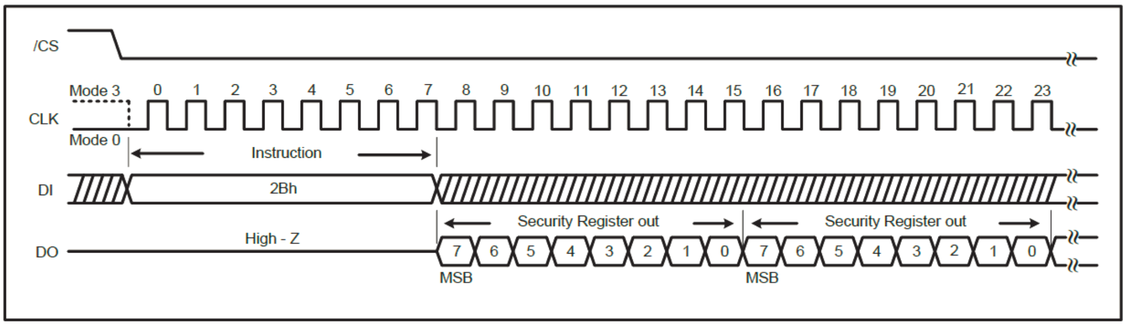


Figure 42a. Read Security Register instruction (SPI Mode)

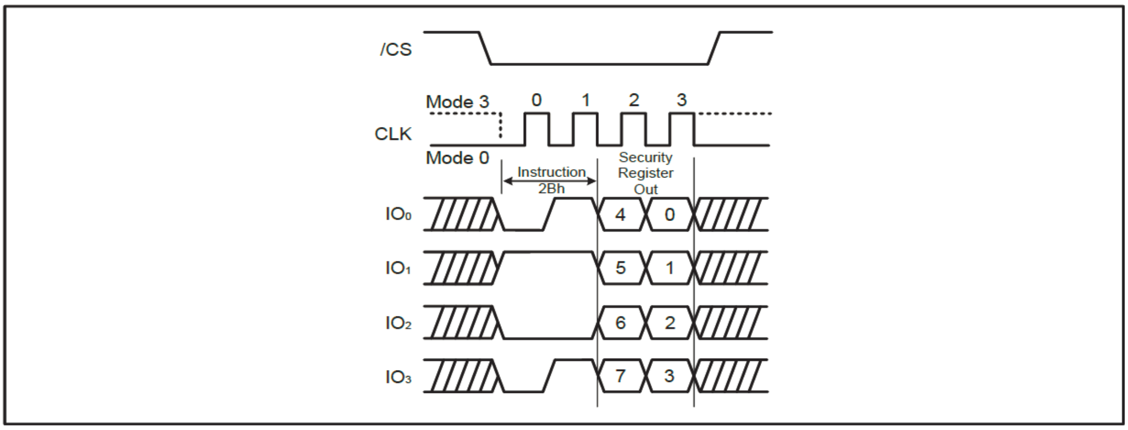


Figure 42b. Read Security Register instruction (QPI Mode)

8.28 Write Security Register (2Fh)

The Write Security Register instruction is for changing the values of Security Register bits. Unlike Write Status Register, the Write Enable instruction is not required before writing Write Security Register instruction. The Write Security Register instruction may change the value of bit1 (LDSO bit) for customer to lock-down the 4K-bit Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more.

The /CS must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

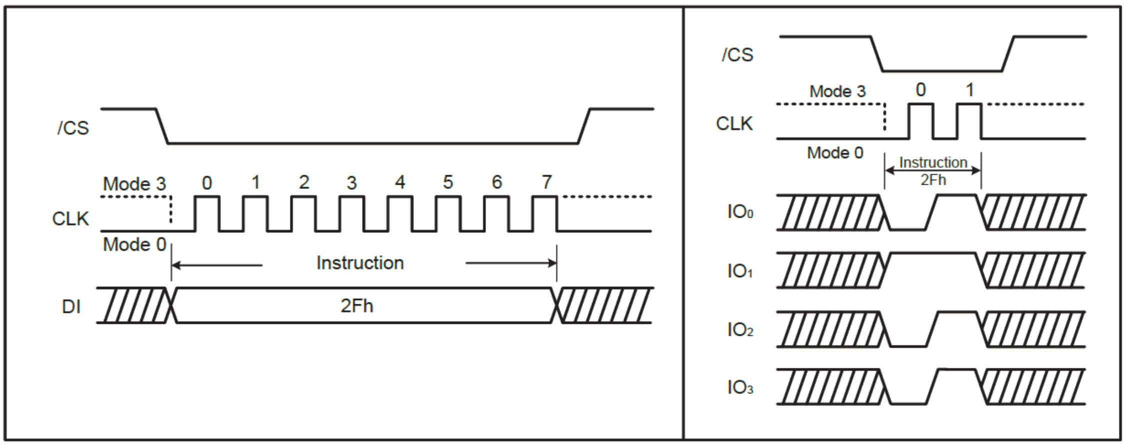


Figure 43. Write Security Register instruction for SPI Mode and QPI Mode (right)

8.29 4K-bit Secured OTP

It's for unique identifier to provide 4K-bit one-time-program area for setting device unique serial number which may be set by factory or system customer. Please refer to table of "4K-bit secured OTP definition".

- Security register bit 0 indicates whether the chip is locked by factory or not.
- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with ENSO command) and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing EXSO command
- Customer may lock-down bit1 as "1". Please refer to "table of security register definition" for security register bit definition and table of "4K-bit secured OTP definition" for address range definition.
- Note. Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit secured OTP mode, array access is not allowed to write.

4K-bit secured OTP definition

<table>
<tr><th>Address range</th><th>Size</th><th>Standard
Factory Lock</th><th>Customer Lock</th></tr>
<tr><td>000000 ~ 00000F</td><td>128-bit</td><td>ESN
(Electrical Serial Number)</td><td rowspan="2">Determined by customer</td></tr>
<tr><td>000010 ~ 0001FF</td><td>3968-bit</td><td>N/A</td></tr>
</table>

9 ELECTRICAL CHARACTERISTICS

9.1 Power-up Timing

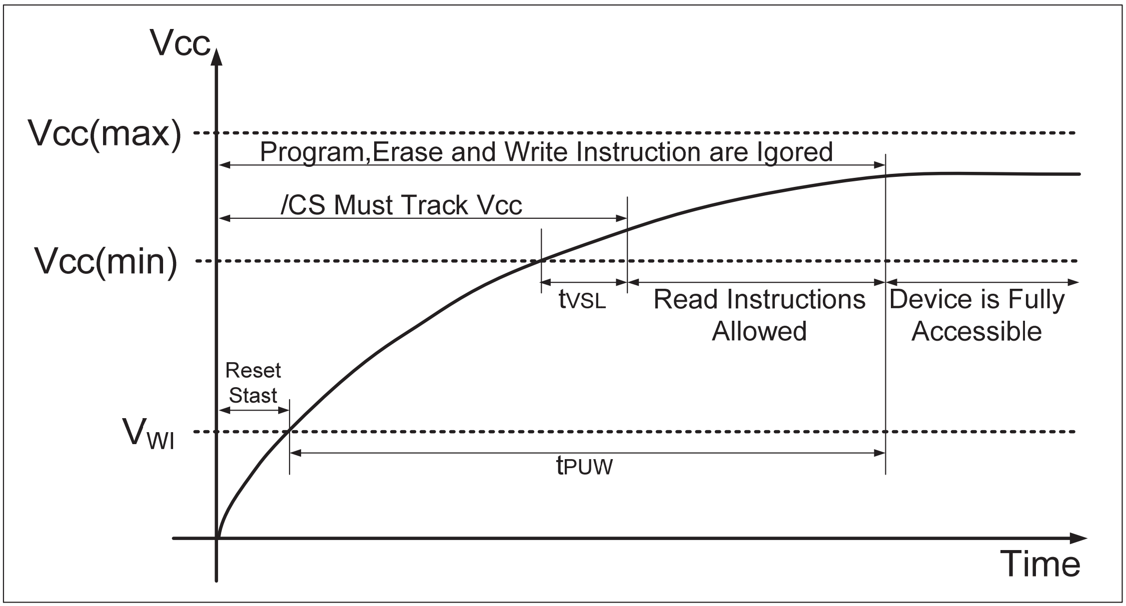


Figure 44, Power-up Timing

Table 3, Power-up Timing

PARAMETER	SYMBOL	TYPE		UNIT
		MIN	MAX	
Vcc(min) to CS# Low	tVSL(1)	10		µs
Time Delay Before Write Instruction	tPUW(1)	1	10	ms
Write Inhibit Threshold Voltage	VWI(1)	1	1.4	V

Note:
1.The parameters are characterized only.

9.2 Absolute Maximum Ratings

Stresses above the values so mentioned above may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values.

Table 4, Absolute Maximum Ratings

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		-0.6 to VCC+0.4	V
Voltage applied on any pin	V_{IO}	Relative to Ground	-0.6 to VCC+0.4	V
Transient Voltage on any Pin	V_{IOT}	<20ns Transient Relative to Ground	-1.0 to VCC+1.0	V
Storage Temperature	T_{STG}		-65 to +150	℃
Lead Temprature	T_{LEAD}		See Note(3)	℃
Electrostatic Discharge Voltage	V_{ESD}	Human Body Model(4)	-2000 to +2000	V

Notes:
1. Specification for ZD25LQ64 is preliminary. See preliminary designation at the end of this document.
2. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
3. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
4. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 ohms, R2=500 ohms).

9.3 INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH). The Status Register bits are set to 0.

9.4 Recommended Operating Ranges

Table 5, Recommended Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage	VCC	FR=104MHz,fR=50MHz	1.65	1.95	V
Ambient Temperature, Operating	TA	Industrial	-40	+85	℃

Notes: 1. Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.

9.5 Program Acceleration via ACC Pin

The program acceleration function requires applying VHH to the ACC input, and then waiting a period of tWC. Minimum tVHH (rise & fall times) is required for ACC to change to VHH from VIL or VIH. Removing VHH from the ACC pin returns the device to normal operation after a period of tWC.
Only Read Status Register and Page Program operation are allowed when ACC is at (VHH).
The start address must be entered by the multiples of 4-byte (for example xxxxx0, xxxxx4, xxxxx8, xxxxxC). Also the data must be entered with a minimum of 4-byte and multiples of 4-byte unit when Program Acceleration via ACC Pin.

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
/WP pin High Voltage	V_{HH}(1)	8.5	9.5	V
/WP pin Voltage rise and fall time	tVHH(1)	2.2		μs
/WP at V_{HH} and V_{IL} or V_{IH} to first instruction	tWC(1)	5		μs

Note:

1. These parameters are characterized only.

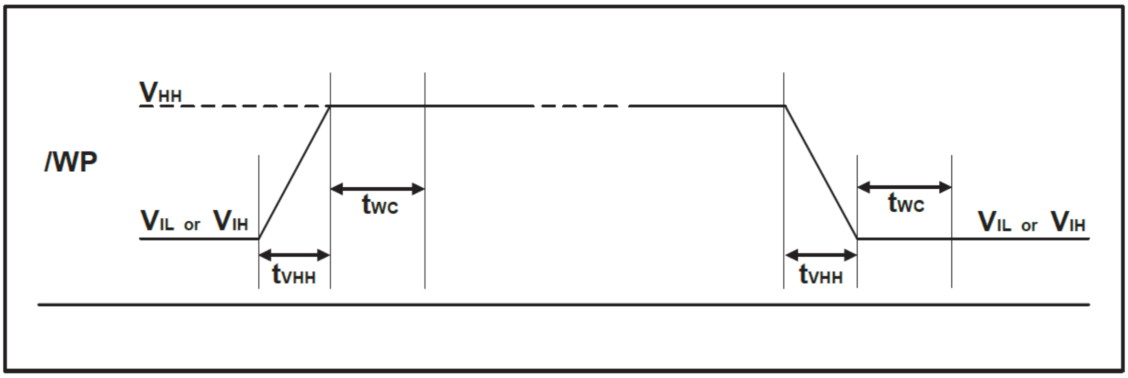


Figure 45. ACC Program acceleration Timing and Voltage Levels

9.5 DC Characteristics

Table 6. DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
CIN(1)	Input Capacitance	VIN = 0V(2)			6	pF
Cout(1)	Output Capacitance	VOUT = 0V(2)			8	pF
ILI	Input Leakage				±2	µA
ILO	I/O Leakage				±2	µA
ICC1	Standby Current	CS# = VCC, VIN = GND or VCC		10	50	µA
ICC2	Power-down Current	CS# = VCC, VIN = GND or VCC		2	20	µA
ICC3	Current Read Data / Dual Output Read 33MHz(2)	C = 0.1 VCC / 0.9 VCC IO = Open			15	mA
ICC3	Current Read Data / Dual Output Read 85MHz(2)	C = 0.1 VCC / 0.9 VCC IO = Open			20	mA
ICC3	Current Read Data / Dual/Quad Read 133MHz	C = 0.1 VCC / 0.9 VCC IO = Open			28	mA
ICC4	Current Page Program	CS# = VCC		15	25	mA
ICC5	Current Write Status Register	CS# = VCC		10	20	mA
ICC6	Current Sector/Block Erase	CS# = VCC		15	25	mA
ICC7	Current Chip Erase	CS# = VCC		15	25	mA
VIL	Input Low Voltage		–0.5		VCC x 0.2	V
VIH	Input High Voltage		VCC x0.7		VCC +0.4	V
VOL	Output Low Voltage	IOL = 100 µA			0.2	V
VOH	Output High Voltage	IOH = –100 µA	VCC –0.2			V

Notes:
1. Tested on sample basis and specified through design and characterization data. TA=25° C, VCC 1.8V.
2. Checker Board Pattern.

9.6 AC Measurement Conditions

Table 7, AC Measurement Conditions

Symbol	PARAMETER	Min.	Max.	Unit
CL	Load Capacitance		30	pF
TR, TF	Input Rise and Fall Times		5	ns
VIN	Input Pulse Voltages	0.2VCC to 0.8VCC		V
VtIN	Input Timing Reference Voltages	0.3VCC to 0.7VCC		V
VtON	Output Timing Reference Voltages	0.5 VCC to 0.5 VCC		V

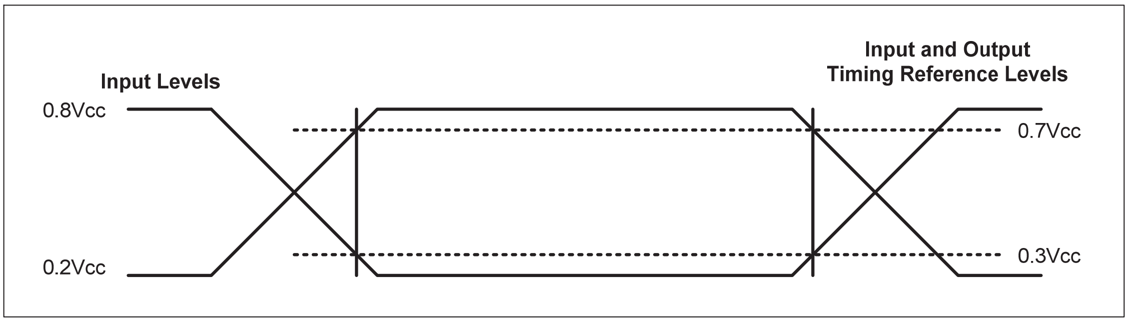


Figure 46, AC Measurement I/O Waveform

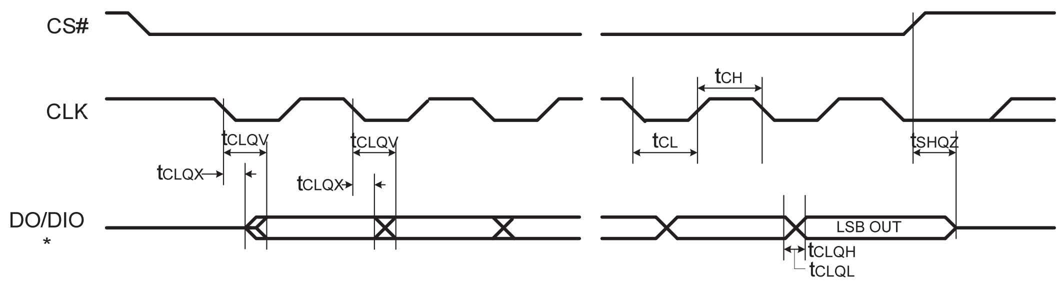
9.7 AC Electrical Characteristics

Table 8, AC Electrical Characteristics

SYMBOL	ALT	Parameter	SPEC			UNIT
			MIN	TYP	MAX	
FR	fC	Clock frequency For all instructions, except Read Data (03h) and Dual output(3bh) 1.65V-1.95V VCC & Industrial Temperature	D.C.		133	MHz
fR		Clock frequency for Read Data instruction (03h) Read ID (90h, 9Fh and ABh), Read Status Register (05h and 35h)	D.C.		50	MHz
tCLH, tCLL(1)		Clock High, Low Time for all instructions except Read Data (03h)	3.5			Ns
tCRLH, tCRLL(1)		Clock High, Low Time for Read Data (03h) instruction	8			Ns
tCLCH(2)		Clock Rise Time peak to peak	0.1			V/ns
tCHCL(2)		Clock Fall Time peak to peak	0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time relative to CLK	5			Ns
tCHSL		CS# Not Active Hold Time relative to CLK	5			Ns
tDVCH	tDSU	Data In Setup Time	2			Ns
tCHDX	tDH	Data In Hold Time	3			Ns
tCHSH		CS# Active Hold Time relative to CLK	5			Ns
tSHCH		CS# Not Active Setup Time relative to CLK	5			Ns
tSHSL	tCSH	CS# Deselect Time (for Array Read →Array Read / Erase or Program → Read Status Register)	30			Ns
tSHQZ(2)	tDIS	Output Disable Time			7	Ns
tCLQV	tV	Clock Low to Output Valid 2.7V-3.6V / 3.0V-3.6V			6	Ns
Tclqx	tHO	Output Hold Time	2			Ns
tHLCH		/HOLD Active Setup Time relative to CLK	5			Ns
tCHHH		/HOLD Active Hold Time relative to CLK	5			Ns
tHHCH		/HOLD Not Active Setup Time relative to CLK	5			Ns
tCHHL		/HOLD Not Active Hold Time relative to CLK	5			Ns
tHHQX(2)	tLZ	/HOLD to Output Low-Z			7	Ns
tHLQZ(2)	tHZ	/HOLD to Output High-Z			12	Ns
tWHSL(3)		Write Protect Setup Time Before CS# Low	20			Ns
tSHWL(3)		Write Protect Hold Time After CS# High	100			Ns
tDP(2)		CS# High to Power-down Mode			3	Us
tRES1(2)		CS# High to Standby Mode without Electronic Signature Read			3	Us
tRES2(2)		CS# High to Standby Mode with Electronic Signature Read			1.8	Us
tRST		CS# High To Next Command After Reset			30	Us
tRUS		/CS High to next Instruction after Suspend			30	Us
tW		Write Status Register Time		5	15	Ms
tPP		Page Program Time		0.5	5	Ms
tEP		Page Program Time(ACC=9V)		0.3	3	Ms
tSE		Sector Erase Time (4KB)		70	400	Ms
tBE1		Block Erase Time (32KB)		0.2	1.5	S
tBE2		Block Erase Time (64KB)		0.35	3	S
tCE		Chip Erase Time		30	150	S

Notes:
1, Clock high + Clock low must be less than or equal to 1/fC.
2, Value guaranteed by design and/or characterization, not 100% tested in production.
3, Only applicable as a constraint for a Write Status Register instruction when Sector Protect Bit is set to 1.

4, For multiple bytes after first byte within a page, tBPN = tBP1 + tBP2 * N (typical) and tBPN = tBP1 + tBP2 * N (max), where N = number of bytes programmed.



*DIO is an Output ONLY for the fast read dual output instructions(3Bh)

Figure 47, Serial Output Timing

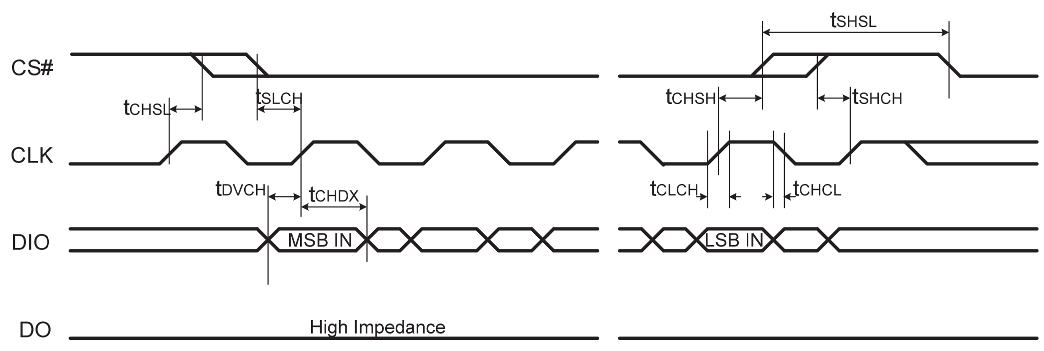


Figure 48, Input Timing

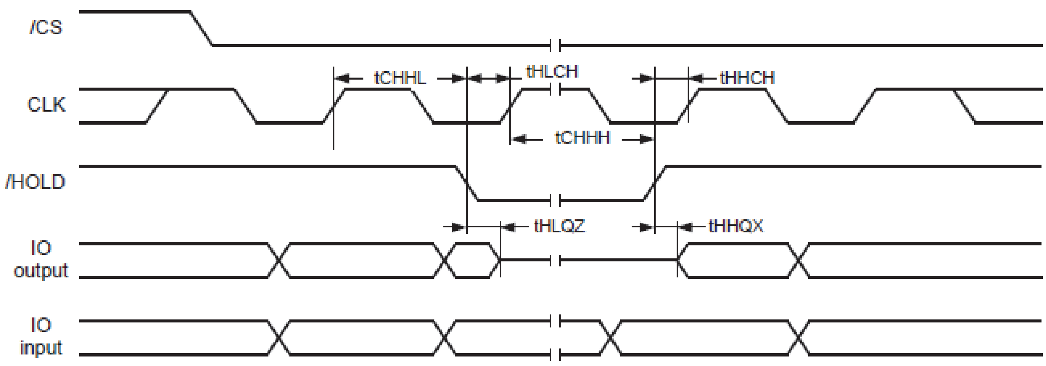
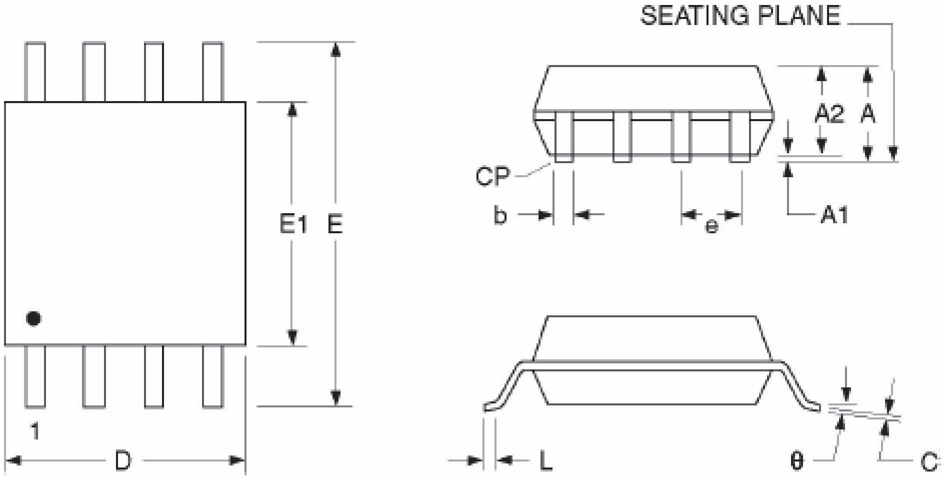


Figure 49, Hold Timing

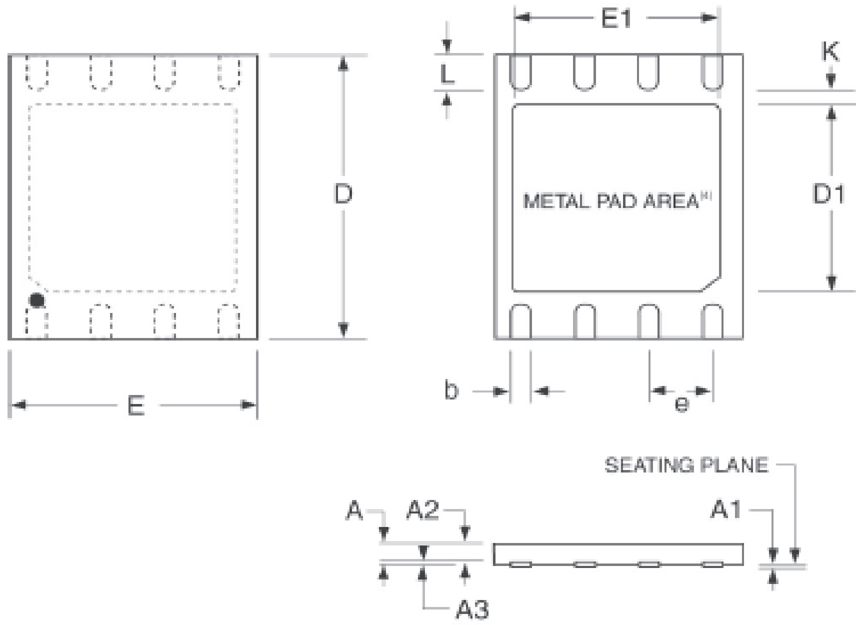
10 PACKAGE MECHANICAL

10.1 8-Pin SOIC 208-mil



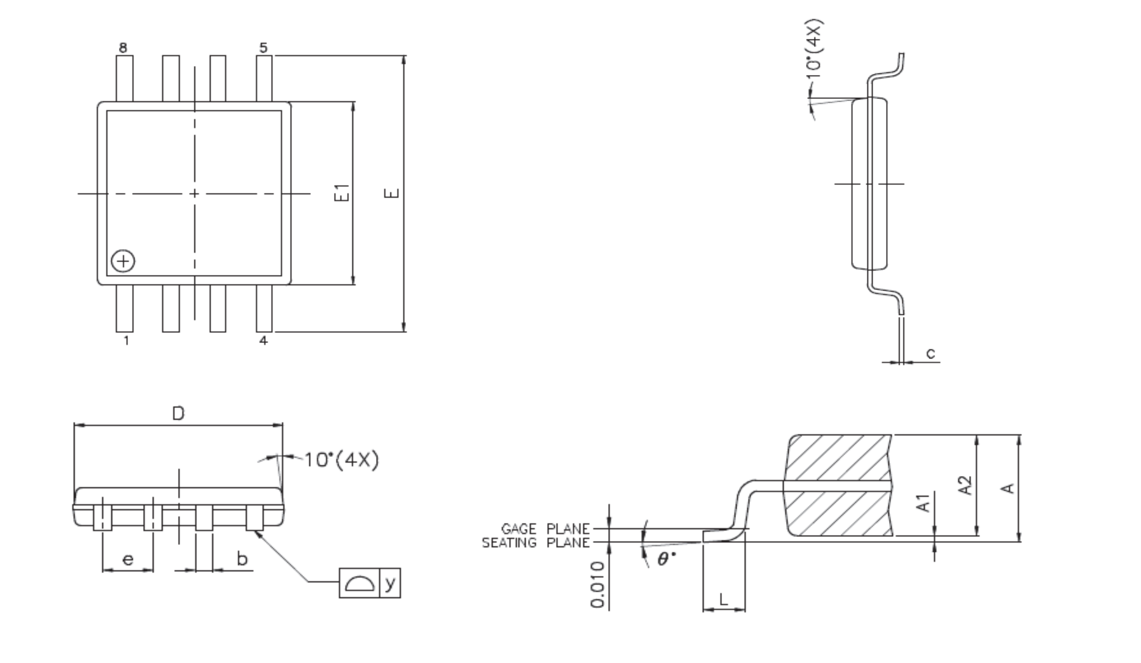
SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.75	2.16	0.069	0.085
A1	0.05	0.25	0.002	0.010
A2	1.70	1.91	0.067	0.075
b	0.35	0.48	0.014	0.019
C	0.19	0.25	0.007	0.010
D(3)	5.18	5.38	0.204	0.212
E	7.70	8.10	0.303	0.319
E1(3)	5.18	5.38	0.204	0.212
e(2)	1.27 BSC		0.050 BSC	
L	0.50	0.80	0.020	0.031
θ	0°	8°	0°	8°
y	---	0.10	---	0.004

10.2 8-Contact WSON (6x5mm)



SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP.	MAX	MIN	TYP.	MAX
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	0.02	0.05	0.0000	0.0008	0.0019
A2		0.55			0.0126	
A3	0.19	.0.20	0.25	0.0075	0.0080	0.0098
b	0.36	0.40	0.48	0.0138	0.0157	0.0190
D(3)	5.90	6.00	6.10	0.2320	0.2360	0.2400
D1	3.30	3.40	3.50	0.1299	0.1338	0.1377
E	4.90	5.00	5.10	0.1930	0.1970	0.2010
E1(3)	4.20	4.30	4.40	0.1653	0.1692	0.1732
e(2)	1.27 BSC			0.0500 BSC		
K	0.20			0.0080		
L	0.50	0.60	0.75	0.0197	0.0236	0.0295

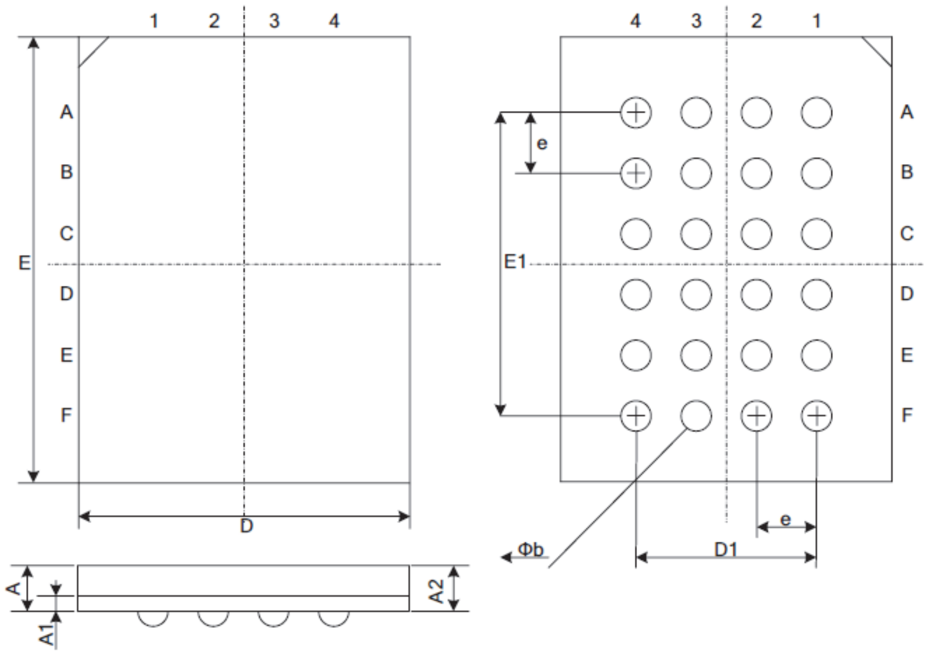
10.3 8-Pin VSOP 208-mil



SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A	---	---	1.00	---	---	0.039
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.75	0.80	0.85	0.030	0.031	0.033
b	0.35	0.42	0.48	0.014	0.017	0.019
c	0.127 REF.			0.005 REF.		
D	5.18	5.28	5.38	0.204	0.208	0.212
E	7.70	7.90	8.10	0.303	0.311	0.319
E1	5.18	5.28	5.38	0.204	0.208	0.212
e	---	1.27	---	---	0.050	---
L	0.50	0.65	0.80	0.020	0.026	0.031
y	---	---	0.10	---	---	0.004
θ	0 °	---	8 °	0 °	---	8 °

Notes:
1. JEDEC outline: N/A.
2. Dimension “D”, “D1” does not include mold flash, mold flash shall not exceed 0.006 [0.15mm] per end. Dimension “E”, “E1” does not include inter lead flash. Inter lead flash shall not exceed 0.010 [0.25mm] per side.
3. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.003 [0.08mm].

10.4 TFBGA-24BALL (6*4 ball array)

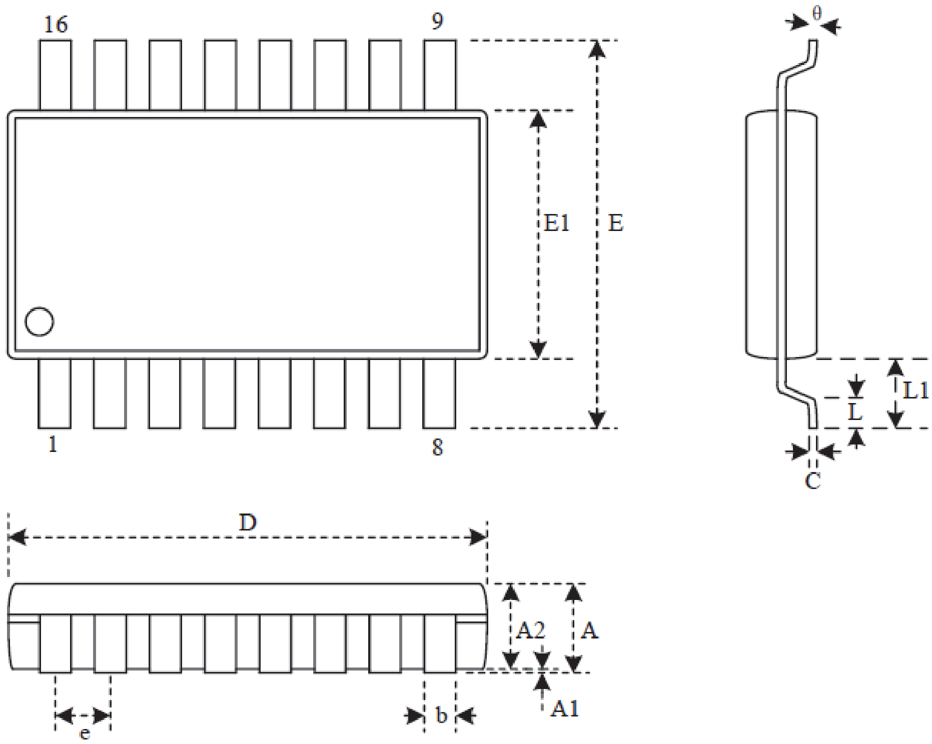


Dimensions

Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e
mm	Min		0.25		0.35	5.90		7.90		
	Nom		0.30	0.85	0.40	6.00	3.00	8.00	5.00	1.00
	Max	1.20	0.35		0.45	6.10		8.10		
Inch	Min		0.010		0.014	0.232		0.311		
	Nom		0.012	0.033	0.016	0.236	0.120	0.315	0.200	0.039
	Max	0.047	0.014		0.018	0.240		0.319		

Note：Both package length and width do not include mold flash.

10.5 SOP16 300mil



Dimensions

Symbol / Unit		A	A1	A2	b	C	D	E	E1	e	L	L1	θ
mm	Min	2.36	0.10	2.24	0.36	0.20	10.10	10.10	7.42		0.40	1.31	0
	Nom	2.55	0.20	2.34	0.41	0.25	10.30	10.35	7.52	1.27BSC	0.84	1.44	5
	Max	2.75	0.30	2.44	0.51	0.30	10.50	10.60	7.60		1.27	1.57	8
Inch	Min	0.093	0.004	0.088	0.014	0.008	0.397	0.397	0.292		0.016	0.052	0
	Nom	0.100	0.008	0.092	0.016	0.010	0.405	0.407	0.296	0.050BSC	0.033	0.057	5
	Max	0.108	0.012	0.096	0.020	0.012	0.413	0.417	0.299		0.050	0.062	8

Note:Both package length and width do not include mold flash.

11 REVISION LIST

Version No.	Description	Date
A	Initial Release	2018/7/14