

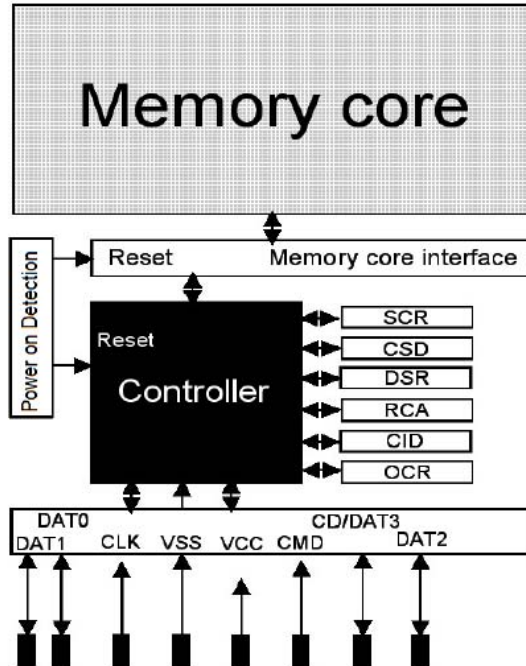
**ZDSD01G/02G/04G/08G/16G/32G/64G**

**SD NAND**

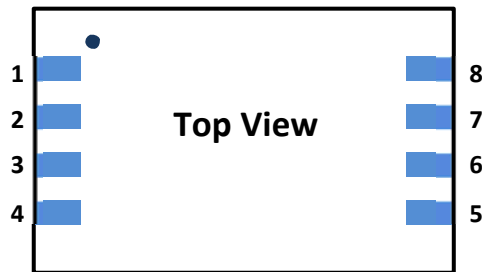
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### 4. Block Diagram



### 5. Pin Assignments



Pin No.	Pin name (SD mode)	Pin name (SPI mode)
1	SD2, I/O pin	NC, no connection
2	SD3, I/O pin	/CS, chip select
3	CLK, clock signal	CLK, clock signal
4	Vss, ground	Vss, ground
5	CMD, command signal	DI, data in
6	SD0, I/O pin	DO, data out
7	SD1, I/O pin	NC, no connection
8	Vdd, power supply	Vdd, power supply

## 6. Usage

### 6.1. Product Protocol

As SD NAND is the realize SD2.0 standard product, thus please refer to the SD2.0 related protocol: SD Physical Layer Specification Version 2.00.

### 6.2. DC Characteristics

Item	Symbol	MIN	MAX	Unit	Note	
Supply voltage	VDD	2.7	3.6	V		
Input voltage	High Level	V <sub>IH</sub>	VDD*0.625	VDD+0.3	V	
	Low Level	V <sub>IL</sub>	VSS-0.3	VDD*0.25	V	
Output voltage	High Level	V <sub>OH</sub>	VDD*0.75	--	V	I <sub>OH</sub> =-2mA, VDD=VDDmin
	Low Level	V <sub>CL</sub>	--	VDD*0.125	V	I <sub>OL</sub> =2ma, VDD=VDDmin
Standby Current(*)	I <sub>cc1</sub>	--	20*	mA	VDD=3.6V, clock 25MHz	
		--	0.2		VDD=3.0V, clock STOP, Ta=25° C	
Operation Current(*)	Write	I	--	25	mA	3.6V/25MHz,50MHz
	Read	I	--	25		
Input voltage setup Time	V <sub>rs</sub>	--	250	ms		

Note: Standby current max 20mA with CLOCK 25Mhz only based on 100 pcs samples

#### Peak Voltage and Leak Current

Item	Symbol	MIN	MAX	Unit	Note
Peak voltage on all lines		-0.3	VDD+0.3	V	
Input Leakage Current for all pins		-10	10	uA	
Output Leakage Current for all outputs		-10	10	uA	

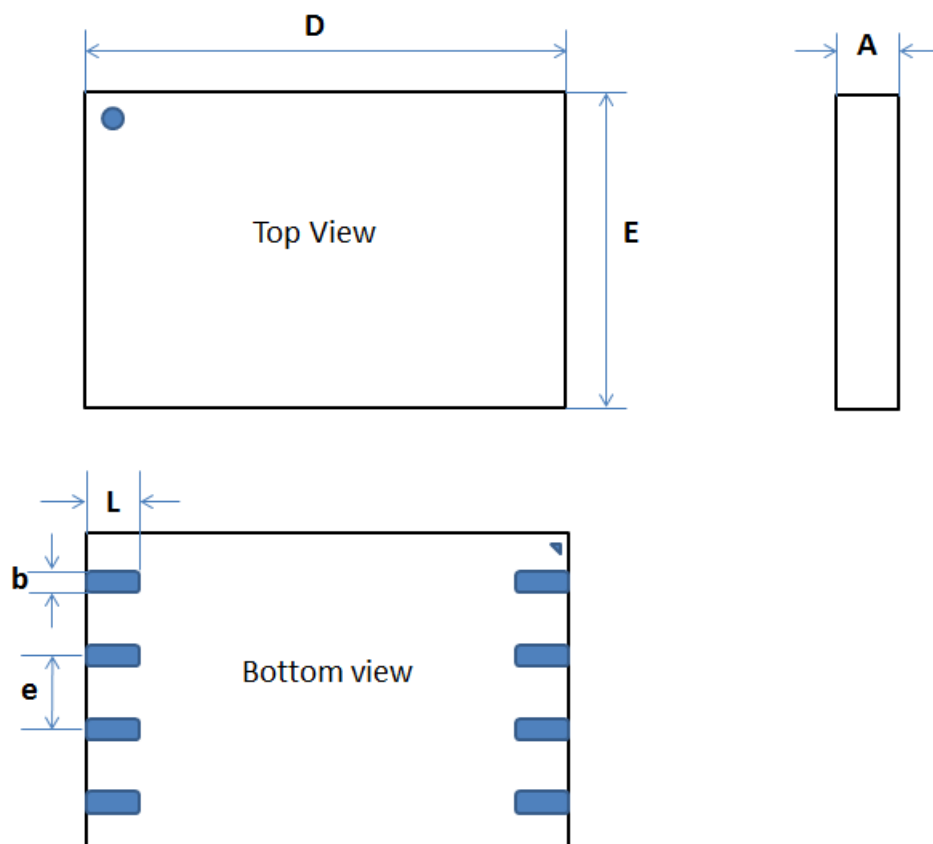
#### Signal Capacitance

Item	Symbol	MIN	MAX	Unit	Note
Pull up Resistance	R <sub>CMD</sub> /R <sub>DAT</sub>	10	100	k	
Total bus capacitance for each signal line	C <sub>L</sub>	-	40	pF	1 card C <sub>HOST</sub> +C <sub>BUS</sub> ≤ 30pF
Card Capacitance for signal pin	C <sub>CARD</sub>	-	10	pF	
Pull up Resistance inside card (pin1)	R <sub>DAT3</sub>	10	90	k	
Capacity Connected to Power line	C <sub>C</sub>	-	5	pF	

Note: WP pull-up (R<sub>wp</sub>) Value is depend on the Host Interface drive circuit.

## 7. Package Dimensions

### LGA8 (SLC 8x6mm/MLC 8x6.2mm) (Land Grid Array)

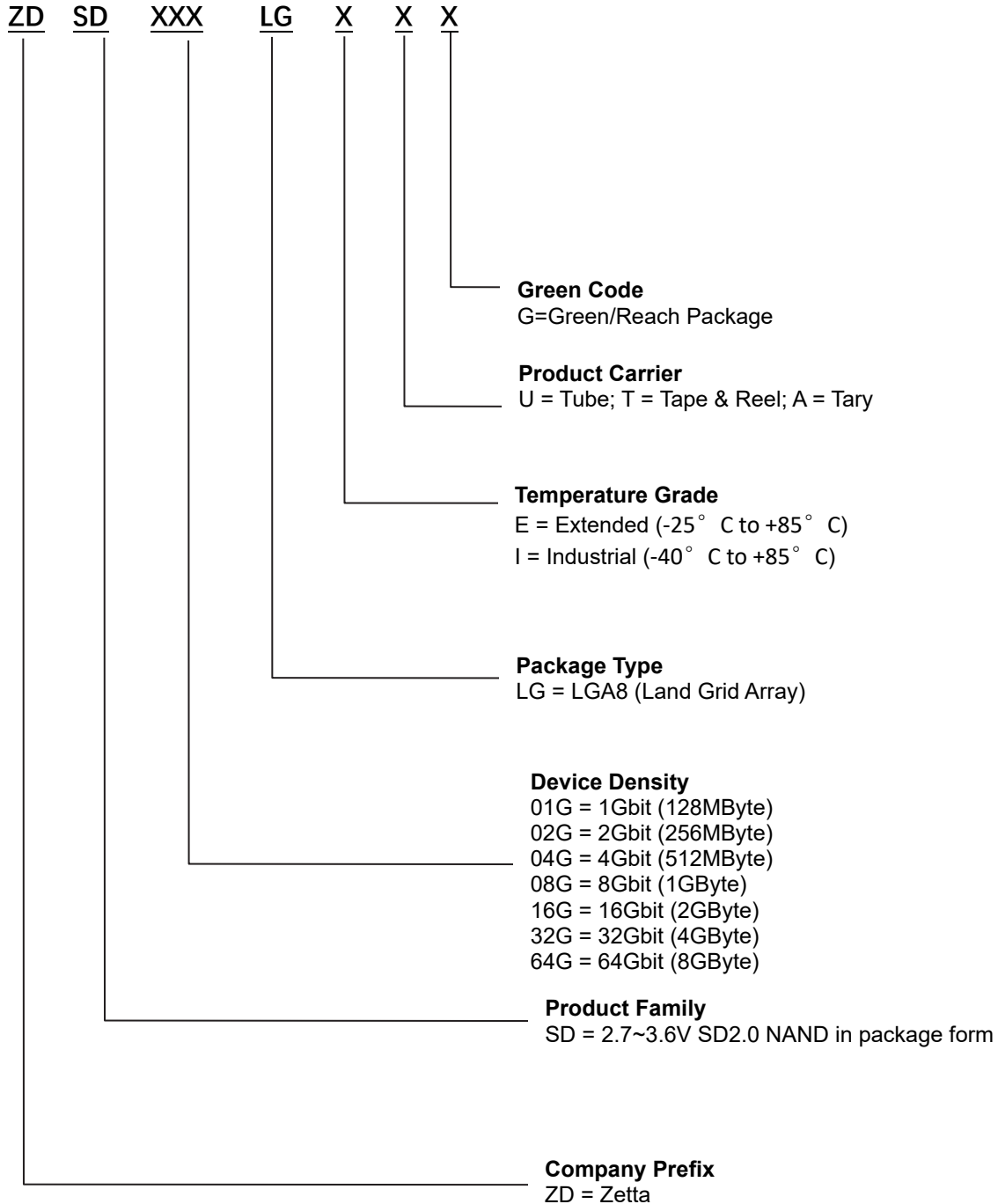


Dimensions:

Symbol		A	b	D	E-SLC	E-MLC	e	L
Unit								
Mm	Min	0.75	0.55	7.95	5.90	6.10		0.75
	Norm	0.80	0.60	8.00	6.00	6.20	1.27	0.80
	Max	0.85	0.65	8.05	6.10	6.30		0.85

## 8. Ordering Information

The ordering part number is formed by a valid combination of the following



## 9. Revision History

<b>Version No.</b>	<b>Change Description</b>	<b>Date</b>
V1.0	Initial release, part number is based on SLC Nand, LGA 8*6mm	2020/06/02
V1.1	Add MLC SD Nand and LGA 8*6.2mm package	2021/12/01
V1.2	Ordering Information Update	2022/2/20
V1.3	Add 64Gb MLC SD Nand	2022/10/08

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